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THD Analysis of a 13 Level Asymmetric Hybrid Cascaded Multilevel Inverter for Industrial Applications

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Abstract: This paper proposes asymmetric cascaded H-bridge multilevel inverter with reduced number of switches suitable for industrial applications and renewable energy too. Cascade Multilevel Inverters are very popular and have many applications in electric utility and for industrial drives. When these inverters are used for industrial drive directly, the THD contents in output voltage of inverters are very significant as the performance of drive depends very much on the quality of voltage applied to drive. There are two types of cascaded H-bridge inverter based on input voltage from different sources namely symmetric and asymmetric inverter.The proposed asymmetric cascaded H-bridge topology consists only one H-bridge(with 4 switches) and 3 more switches totally 7 switches for 13 level output voltage. The new topology is well suited for drives and renewable energy applications. THD depends on modulation index and the switching angles for different levels of multilevel inverters. Therefore, the switching angles are calculated first by using N-R (Newton Raphson) method where certain number of harmonic components has been eliminated. THD is reduced to 9.23% by using SPWM technique.THD analysis is carried out for each switch of firing angle calculated analytically as well as using MATLAB/SIMULINK. The proposed topology is verified with hardware prototype of single phase 13 level inverter using FPGA based Xilinx SPARTAN 3E processor. This processor provides appropriate gating signals for switches using SPWM where the modulation index can be varied manually and THD is observed. By using low pass filter with minimum value, further the THD is reduced to 1.08%.all the results are validated experimentally.

Key words: Multilevel inverter (MLI) · Field programmable gate array (FPGA) · Total harmonic distortion (THD) · SPWM (sinusoidal pulse width modulation).

INTRODUCTION

Nowadays, there has been an increase in the use of renewable energy due to growing concern for the shortage of conventional energy resources and environment pollution. Multilevel inverters are widely used for such renewable energy sources like solar energy generation systems consist of various photovoltaic generators [1]. There are mainly three topologies in multilevel inverter. These are Diode Clamped, Capacitor Clamped and Cascaded multilevel inverter [2]. Multilevel Inverter gives an AC voltage from several DC sources, that is, from the photovoltaic generators. Cascaded H-Bridge structure takes no dc to dc boost converter and takes no additional transformer connection. For that reason it is 25% cheaper in cost compared with transformer combined structure. There are many modulation techniques employed for multilevel inverters [3, 4] namely SPWM and SVM (space vector modulation).Among them, multicarrier SPWM technique is mostly used. Harmonic elimination methods applied in multilevel inverter reported in literature are Sine triangle PWM (SPWM), Optimal Minimization of Total Harmonic Distortion (OMTHD), Selective Harmonic Elimination Pulse Width Modulation (SHE-PWM) etc. Among them Selective Harmonic Elimination Pulse Width Modulation (SHE-PWM) offers a tight control of the harmonic spectrum of a given voltage waveform generated by a power electronic converter along with a low number of switching transitions [5, 6]. There are many optimization methods applied to minimize Total Harmonic Distortion (THD) like Particle Swarm optimization (PSO), Genetic

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algorithm (GA) [7, 8] and Harmony Search algorithm (HSA) [14] in literature. Optimum Switching angles are computed by Newton Raphson method.

There are various levels of H-bridge multi level inverter from 5th level. As the level increases THD reduces. Hence 11 level and 13 level inverters are optimum for attaining IEEE standard minimum THD suitable for various applications. Conventional H-bridge topology has more number of switches namely a single phase 11 level inverter has 5 bridges each H-bridge has 4 IGBT switches. But the proposed topology uses less number of switches.

Cascaded H-bridge inverter which requires several independent dc sources. Normally, each phase of a cascaded multilevel inverter requires 'n' dc sources for 2n+1 level. Based on the dc sources MLI is divided into symmetric and asymmetric cascade MLI that uses equal and unequal dc sources in each phase.asymmetric cascaded H-bridge MLI improves the reliability by reducing the number of dc sources when comparing symmetrical H-Bridge MLI. For the cascaded multilevel inverter there are several well known sinusoidal pulse width modulation strategies. Compared to the conventional triangular carrier based PWM, the inverted rectified sine carrier PWM has a better spectral quality and a higher fundamental output voltage without any pulse dropping [9]. However, the fixed frequency carrier based PWM affects the switch utilization in multilevel inverters.

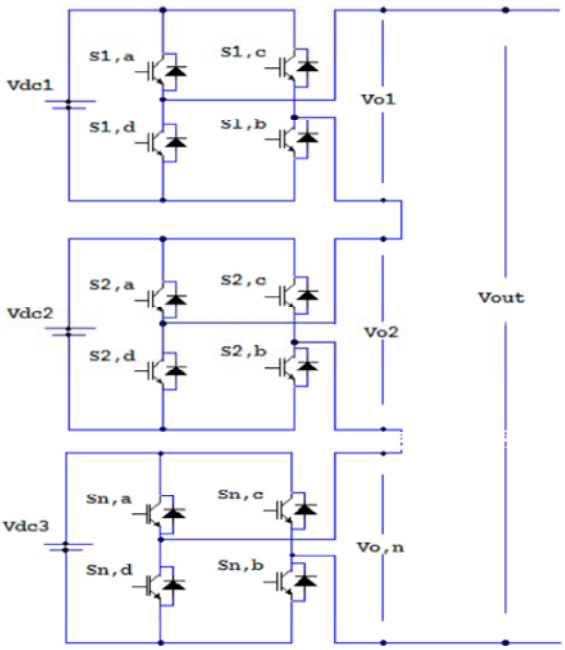

Fig. 1: Cascaded H-bridge multi level inverter-Symmetric

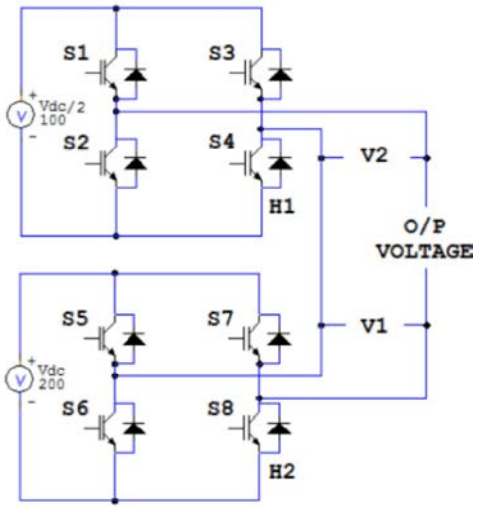

Fig. 2: Asymmetric seven level cascaded multilevel inverter

Symmetrical and Asymmetrical Cascade H-Bridge Inverter:

Configuration of Symmetrical Dc Link Voltage: Structure of symmetric single-phase cascade H-Bridge inverter is shown in Fig. 1 In conventional structure DC link voltage is shared equally among all the DC voltage sources should be regulated to the equal value at V/n if DC voltage across n voltage sources is boosted to Vdc. Each H-bridge has separate dc sources of equal magnitude.

Asymmetric Cascaded Multilevel Inverter: For many applications it is difficult to use separate dc sources and too many dc sources will require many long cables and could lead to voltage imbalance among the dc sources. To reduce the number of dc sources required for the cascaded H-bridge multilevel inverter, a scheme is proposed which uses lesser number of bridges. This scheme therefore provides the capability to produce higher voltages at higher speeds with low switching frequency which has inherent low switching losses and high converter efficiency. A seven-level asymmetric cascaded H-bridge multilevel inverter has two H-bridges for each phase are shown in Fig. 2, whereas the symmetric seven level H-bridge inverter uses three H- bridges.

Unequal dc sources are connected to the corresponding bridges. The DC source for the first H-bridge (H1) is a DC source with an output voltage of Vdc, while the DC source for the second bridge (H2) is a DC source with an output voltage of Vdc/2. The output voltage of the first H-bridge is denoted by v1 and the

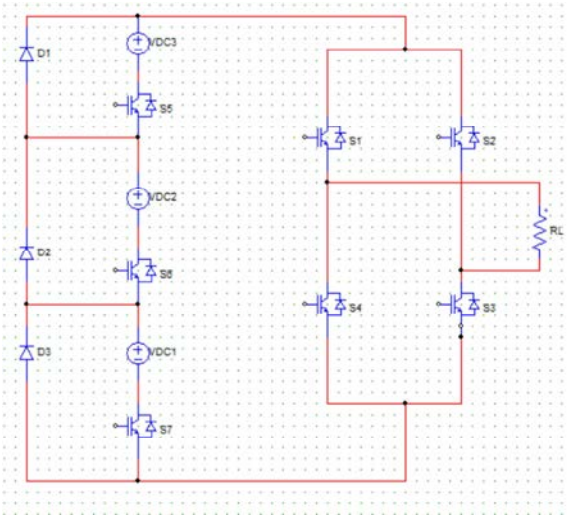

Fig. 3: Proposed asymmetric topology for 13 level cascaded MLI

output voltage of the second H-bridge is denoted by v2 so that the output of this two DC source cascaded multilevel inverter V (t) = V1 (t) + V2 (t).By appropriately opening and closing the switches of H1, the output voltage of H1 can be made equal to +Vdc, 0 and -Vdc.

Similarly the output voltage of H-Bridge-2 V2 (t) can be made equal to -Vdc/2, 0 or +Vdc/2 by opening and closing the switches of H2 [10]. Hence V (t) takes values -3/2Vdc, -Vdc, -1/2Vdc, 0, +1/2Vdc, +Vdc, +3/2Vdc as shown in the Fig. 3. The advantages of the topology are reduced number of dc sources, High speed capability, Low switching loss and High conversion efficiency.

The literature reports that the asymmetric inverter with dc voltage ratios 1 : 3 : 9 (power of 3) [11, 12], can provide an ac voltage of 3n levels with low harmonic content and hence low total harmonic distortion (THD). The asymmetric inverters can be used in different applications such as active filters [13], electric vehicles [14] and ac drives. In order to reduce the number of switches and THD we go for proposed topology of 13 levels cascaded MLI.

Proposed Topology: For multilevel inverter topologies, the required number of power devices depends on the output voltage level. However, increasing the number of power semiconductor switches also increases the inverter circuit size, cost, installation area and control complexity as well as output voltage levels. Higher voltage levels are needed to reduce THD in voltage without adding filters. Thus to provide a large number of output levels without increasing the number of bridges, a new power circuit

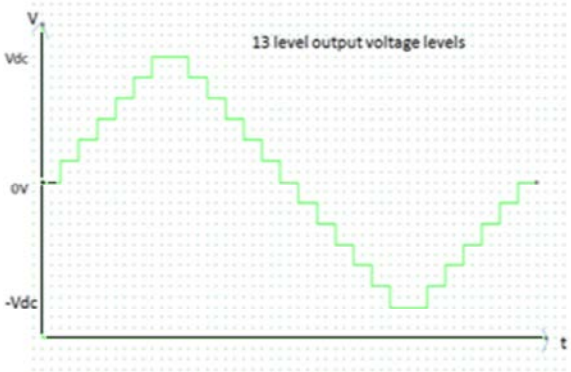

Fig. 4: output voltage levels for 13 level inverter

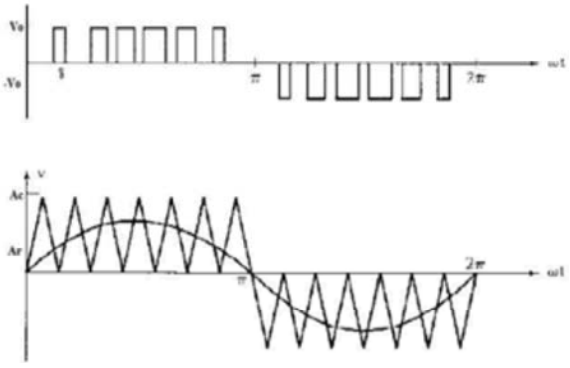

Fig. 5: Pulse with variation due to SPWM

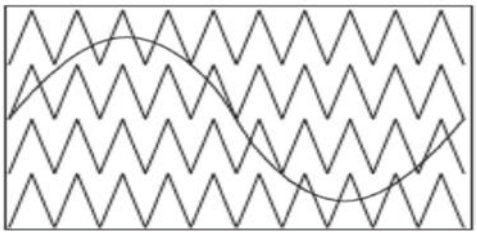

Fig. 6: Multilevel carrier SPWM

topology and a suitable method to determine the dc voltage sources level for symmetrical and asymmetrical multilevel inverter are proposed in this paper Fig. 4 shows the proposed basic unit for asymmetrical multilevel inverter. The output for 13-level topology is shown in Fig. 5 [15].

Control Techniques Of Multilevel Inverter: The magnitude of the AC output phase voltage is given by

$$V_{AN} = V_{A1} + V_{A2} + V_{A3} + V_{A4} + V_{A5} \quad (1)$$

In general, the Fourier series expansion of the staircase output voltage waveform as shown in Fig. 4. The output waveforms have a double symmetry compared to the quarter and the half-period thus the angles of conduction must satisfy the following condition:

$$(0 < \theta_1 < \theta_2 < \theta_3 < \theta_4 < \theta_5 < \frac{\pi}{2}) \quad (2)$$

The output voltage V_{DC} is given by the voltage steps waveform such as the one depicted in Fig. 4 with 5 steps, the Fourier transform for this waveform is as follows:

$$V_{AN}(\omega t) = 4E/\pi \sum [\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3) + \cos(n\theta_4) + \cos(n\theta_5)] x \sin(n\omega t)/n \quad (3)$$

For $(0 < \theta_1 < \theta_2 < \theta_3 < \theta_4 < \theta_5 < \frac{\pi}{2})$

Where n= 1,3,5,7 …

From (3), the magnitude of the Fourier coefficients when normalized with respect to E is as follows:

$$H(n) = \frac{4}{n\pi}[\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3) + \cos(n\theta_4) + \cos(n\theta_5)] \quad (4)$$

Where n is the harmonic order and $\theta 1$, θ_2 and θ_3 are independent switching angles. The coefficient $4E/\pi$ represent peak value of the maximum fundamental voltage $V_{H,max}$ of an H -bridge cell, which occurs when switching angle θ_1 of V_{H1} reduces to zero[16].

Modulation index is given by,

$$Ma = V_{AN1}/H x V_{H,max} = V_{AN1}/H x 4E/\pi \quad (5)$$

Where V_{AN1} is the peak value of the fundamental inverter phase voltage v_{AN1} and H is the number of H- bridge cells per phase.

For a seven level cascaded H-bridge inverter with 5^{TH} and 7^{th} harmonic elimination, the following equations can be formulated

$$\begin{aligned} &\cos(1_1) + \cos(1_2) + \ldots\ldots\ldots + \cos(1_6) = 6M \\ &\cos(3_1) + \cos(3_2) + \ldots\ldots\ldots + \cos(3_6) = 0 \\ &\cos(5_1) + \cos(5_2) + \ldots\ldots\ldots + \cos(5_6) = 0 \\ &\cos(7_1) + \cos(7_2) + \ldots\ldots\ldots + \cos(7_6) = 0 \end{aligned} \quad (6)$$

θ_1=57.106°, θ_2=28.717° and θ_3=11.504° for ma=0.8.

The waveform of V_{AN} does not contain the 5^{th} and 7^{th} harmonics and its THD is 12.5%.compared with carrier-based PWM schemes, the staircase modulation features low switching losses. Thus we used SPWM modulation technique in this paper [17].

Modulation Technique: A.SPWM (Sinusoidal Pulse Width Modulation)

In this modulation technique are multiple numbers of output pulse per half cycle and pulses are of different width. In this technique pulse magnitude will be constant and only pulse time (width) can be changed The width of each pulse is varying in proportion to the amplitude of a sine wave analyzed at the centre of the same pulse. The gating signals are generated by comparing a sinusoidal reference frequency (f) with a high frequency triangular carrier wave signal (f_c). The point of intersection of the two frequency points determines the switching angles for the MOSFET.

The rms ac output voltage is,

$$Vo = Vs \sqrt{p\delta/\pi} \quad (7)$$

Where, P= number of pulses, δ- pulse width.

This PWM technique involves generation of a digital waveform, for which the duty cycle can be modulated in such a way so that the average voltage waveform corresponds to a pure sine wave. The simplest way of producing the SPWM signal is through comparing a low power sine wave reference with a high frequency triangular wave. Through an LC filter, the output of Full Wave Bridge Inverter with SPWM signal will generate a wave approximately equal to a sine wave. This technique produces a much more similar AC waveform than that of others. The primary harmonic is still present and there is relatively high amount of higher level harmonics in the signal.

The sampling technique used here is natural sampling. By comparing sinusoidal reference signal with multi carrier triangular wave, the gating pulses are generated.

Multilevel SPWM is, numbers of carriers are used in multilevel SPWM. For ‘m’ level inverter ‘m-1’ carrier are used. Interaction of particular carrier and reference is used to generate gating signal for particular complementary pair

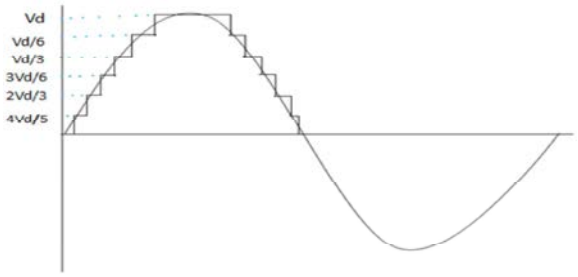

Fig. 7: Thirteen Level Output Waveform

of switches in diode clamped or capacitor-clamped inverter, or particular cell in multi-cell inverter. Here for seven switches six carriers are used [18].

Modes of Operation: There are seven MOSFET and 3 diodes. Four MOSFETS for H-bridge which conducts alternatively where H1, H2 conducts when H3, H4 is off.

H3, H4 conducts when H1,H2 is off.

Switching states of s1, s2 and s3 varies depending on intersection of modulating signal and carrier signal.

Modulation Index and Newton Raphson Method: There are various types of modulation phase shifted, level shifted and staircase modulation. Stair case modulation is well suited for cascade H-bridge inverter.THD indicates quantity of harmonics in output waveform. Modulation index is the difference between the ratio of peak magnitude of the modulating waveform and the carrier waveform. It is related to the inverter dc link voltage and the magnitude of pole voltage output by the inverter. Let $V_m \sin(\grave{u}t)$ is the modulating signal and let the magnitude of triangular carrier signal vary between peak magnitude of $+V_c$ and $-V_c$. Hence the ratio of peak magnitude of modulating wave (V_m) and the carrier wave (V_c) is called as modulation index (m).

So,

$$m = Vm / Vc \tag{8}$$

When modulation index decreases THD increases. The magnitude of modulation index is always limited below one (0<m<1).For modulation index near to 1 THD is smaller. Thus Optimum modulation index varies from 0.65 < m<0.85.

$$THD = \frac{\sqrt{\sum_{n=2}^{x} V_n^2}}{V_1} \tag{9}$$

$$\%\, THD = \frac{\left(VL^2 - VL1^2\right)^{1/2}}{VL_1} X100 \tag{10}$$

$$THD = \left(\sum_{n=2}^{\infty} Vn^2\right)^{1/2} / V1 \tag{11}$$

In general, the main disadvantage of Newton Raphson method is requirement of good initial guess which requires in the past. Knowledge about convergence and good initial guess is not possible always. Hence, in this paper that drawback is eliminated by developing the algorithm which can work with any random initial guess. For a proposed thirteen level inverter, it is required to compute three switching angles at each MI from 0 to 1 with an increment of 0.001.

RESULTS

Simulation of the proposed topology of thirteen level cascaded H-bridge inverter is done using MATLAB/Simulink R2009b and sim-power system in MATLAB. Here seven IGBT switches and 3 diodes are used with modulating voltage of 6v.The carrier wave of frequency 10kHz.Load resistance R= 100 ohms used for this single phase inverter shown in Fig. 9. Fig. 10 shows the same proposed circuit simulated with LC low pass filter at load, where L= 0.8mH and C=8µF.

Fig. 11 shows subsystem where SPWM signals are generated by comparing modulating signal and seven carrier signal and Fig. 15 shows the input signals for SPWM. Fig. 12 shows pulse generation for the IGBT switches from SPWM subsystem circuit where the width of the pulse varies depending on input. Fig. 13 and Fig. 14 shows the output of proposed circuit without and with filter respectively.

Fig. 16. shows the FFT analysis by with THD is found for the proposed circuit is 9.29%. Fig. 17 shows FFT window with THD reduced to 1.03% with LC filter of low cost and size.

Experimental Set up and Results: Hardware set up for the proposed topology has four blocks shown in Fig. 18. FPGA Spartan-3E controller for gating pulse generation, an Opto-coupler, driver circuit and 13 level inverter with load resister R_L. Spartan-3E FPGAs deliver up to 1.6

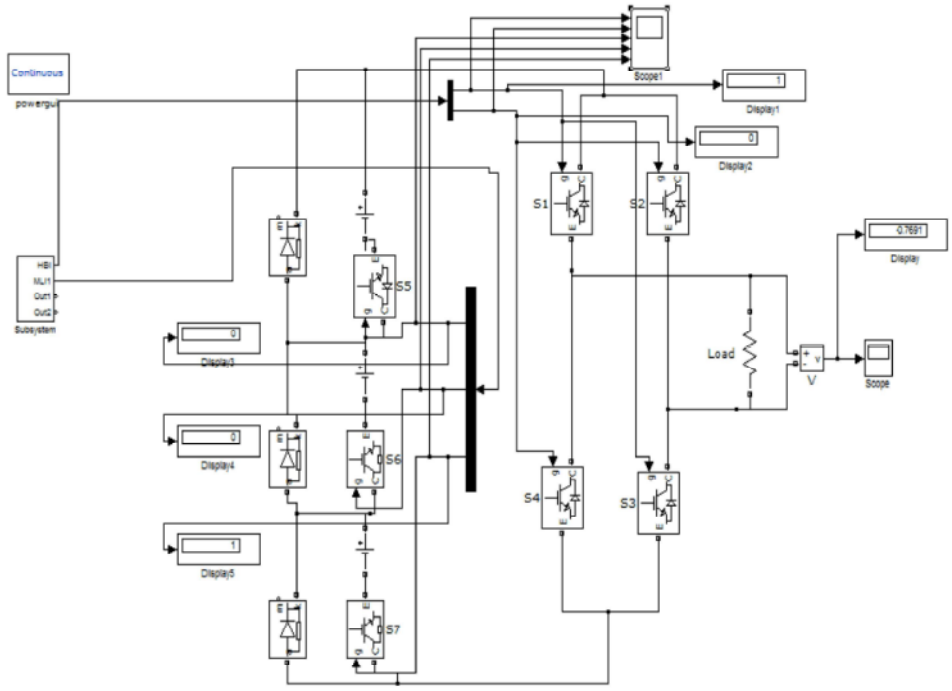

Fig. 8: 13 level cascaded H-bridge proposed inverter without filter

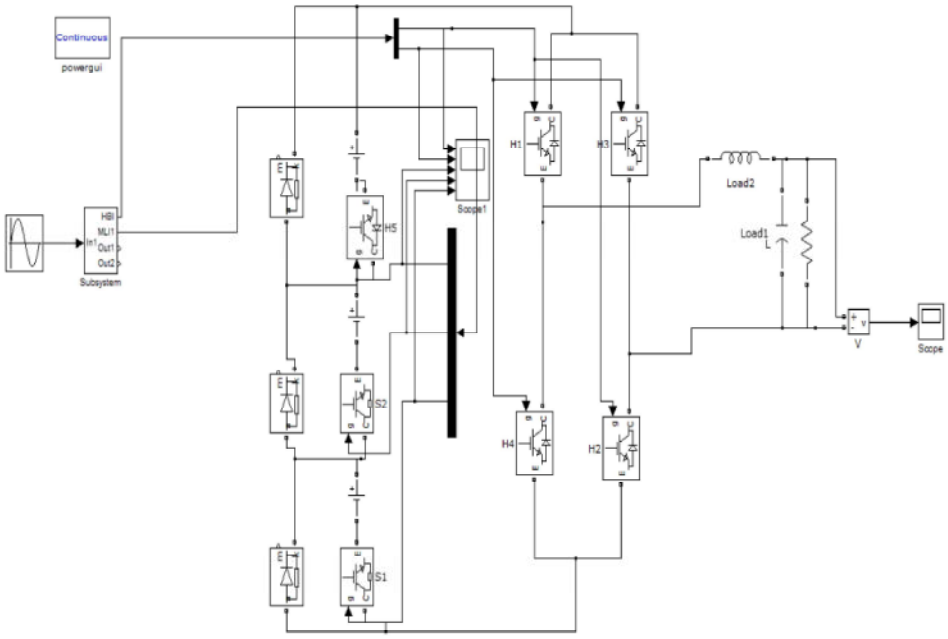

Fig. 9: Proposed 13 level cascaded h-bridge inverter with filter

million system gates, up to 376 I/Os and versatile platform FPGA architecture with the lowest cost per-logic in the industry. The features and capabilities of the Spartan-3E family are optimized for high-volume and low-cost applications and the Xilinx supply chain is ready to fulfill your production requirements. The Spartan-3E family reduces system cost by offering the lowest cost-per-logic of any FPGA family. The advantages of FPGA (Field Programmable Gate Arrays) are enhanced flexibility, reduced board space, power, cost and increased performance.

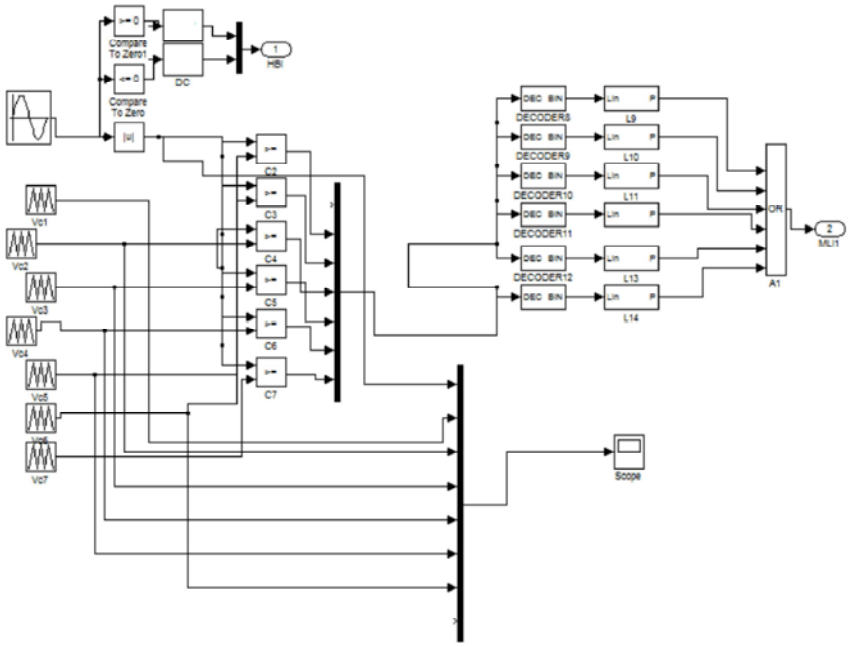

Fig. 10: SIM model of pulse generation for switches

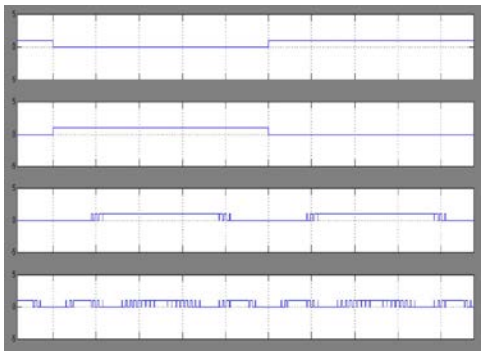

Fig. 11: Generated wave forms for switches

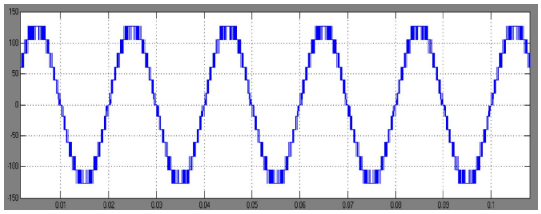

Fig. 12: Output voltage with 13 levels without filter

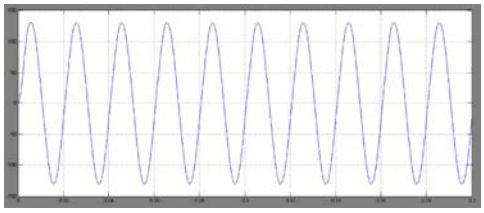

Fig. 14: Sine wave output voltage with Filter

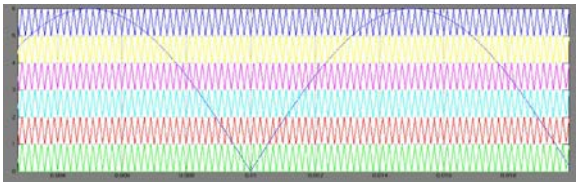

Fig. 15: SPWM

All FPGAs have basic logic cells, I/O logic cells, Programmable interconnect, Software to design and program the FPGA. The function of an Opto isolator is to isolate the control circuit from the power Circuit having LED and photodiode. The name of this Opto coupler IC is 6N137. Gate driver acts as high power buffer stage between the PWM control device and gates of the primary power switching Devices likes as MOSFET, IGBT. Fig. 19 shows the hardware prototype of proposed circuit. Hardware result is checked by observing the 13 level output in DSO with input 6V as shown in Fig. 20.

Modulation index is varied manually in the harware prototype and output voltages are observedas shown in Fig. 21 and Fig. 22. THD is also analysed using harmonic analyser for various modulation index and optimum THD is obtained around 0.80 to 0.95. Table 1 shows the modulation index and corresponding THD variation without using filters.Fig. 23 and Fig. 24 shows output voltage which is observed in DSO for modulation index 0.85 and 0.97.

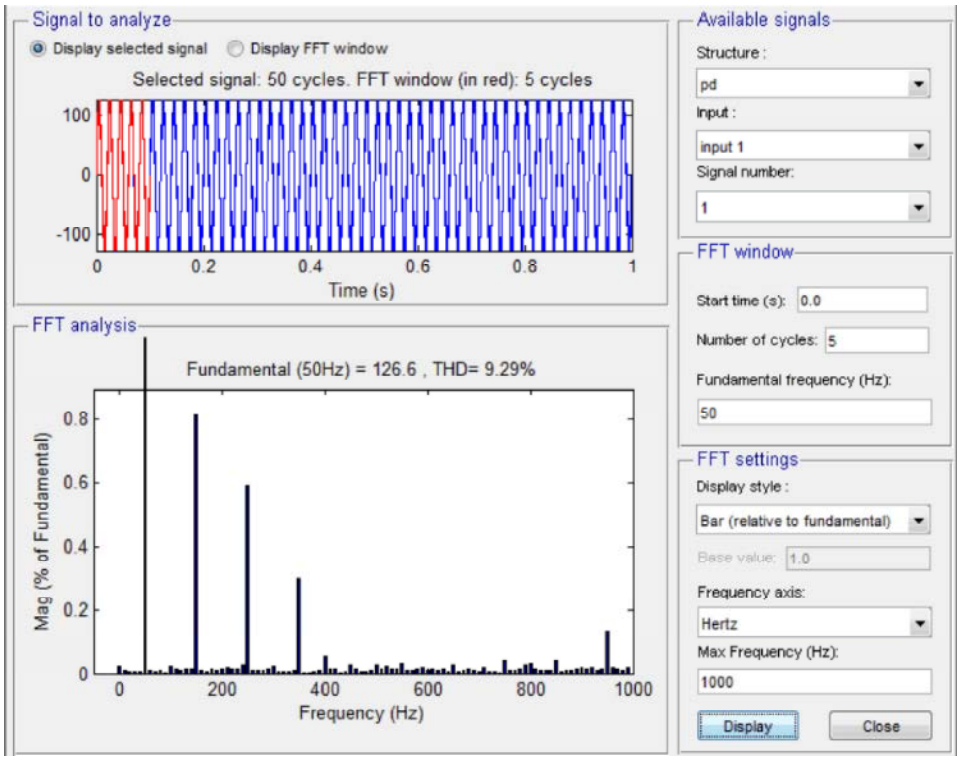

Fig. 16: THD analysis without filter for ma=0.3

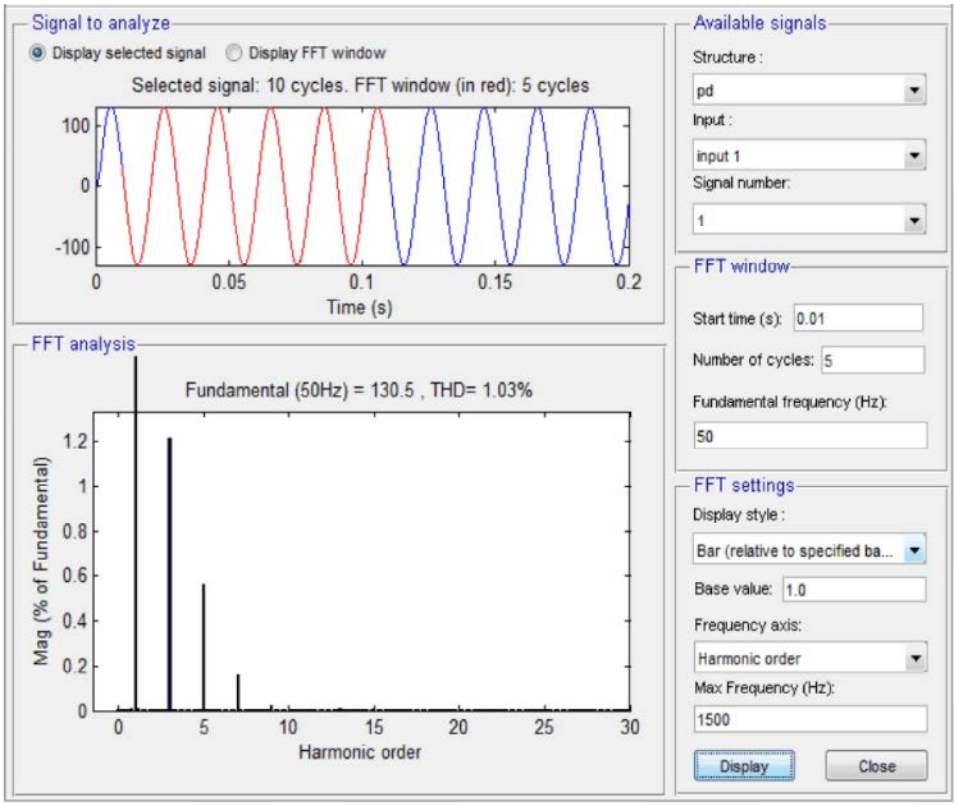

Fig. 17: THD Analysis with Filter

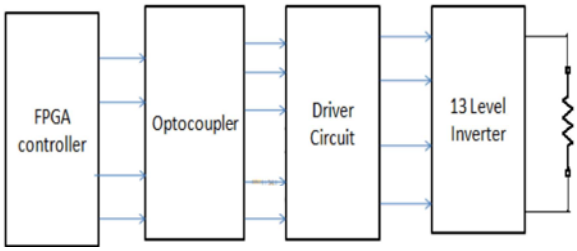

Fig. 18: Basic block diagram of asymmetric cascaded h-bridge 13 level inverter-hardware

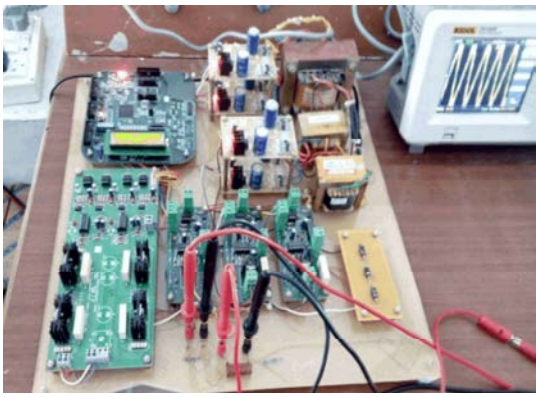

Fig. 19: A Prototype Experimental Setup

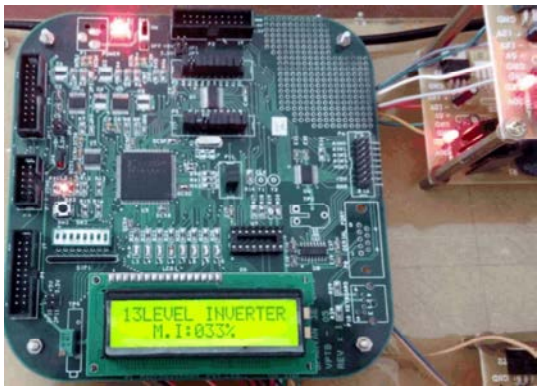

Fig. 20: Modulation Index variation of 33%

Fig. 21: Modulation Index of 100%

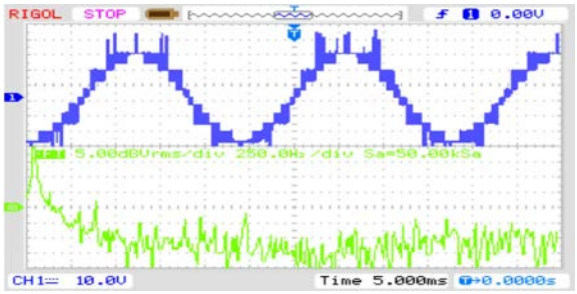

Fig. 22: Hardware output of staircase waveform of proposed 13-level inverter for Mi=0.85

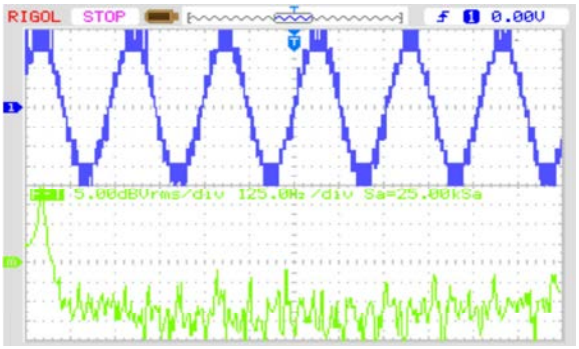

Fig. 24: Hardware output of staircase waveform of proposed 13-level inverter for Mi=0.97

Table 1: Switching Schemes of 13 Level Inverter

Sequence of Switches							Output Voltage
S5	S6	S7	S1	S2	S3	S4	V_d
0	0	1	1	0	1	0	$+V_d$
0	1	1	1	0	1	0	$+V_d/6$
0	1	1	1	0	1	0	$+V_d/3$
1	0	0	1	0	1	0	$+3\ V_d/6$
1	0	1	1	0	1	0	$+2\ V_d/3$
1	1	1	1	0	1	0	$+4\ V_d/5$
0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	$-V_d$
0	1	1	0	1	0	1	$-V_d/6$
0	1	1	0	1	0	1	$-V_d/3$
1	0	0	0	1	0	1	$-3\ V_d/6$
1	0	1	0	1	0	1	$-2\ V_d/3$
1	1	1	0	1	0	1	$-4\ V_d/5$

Table 2: Modulation Index vs Thd-harware Prototype

S.No	Modulation index	% of THD
1	0.33	9.23
2	0.85	8.59
3	0.97	6.19
4	1	4.10

CONCLUSION

From the experimental results observed in both simulation and hardware prototype it is clear that modulation index is near to 1 then THD is smaller. With small and low cost low pass LC filter pure sine wave is obtained in the output with THD 1.03 % which satisfies the IEEE 519-1992 standard.FPGA Xilinx's SPARTAN 3-E DSP controller is used to generate the required gate pulses for 13-level inverter. Less %THD value is obtained at MI of value 1.0 from experimental analysis and from simulation approach is 4.10%. Simulation results and hardware experimental results are compared which are almost similar.

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