

Al₂O₃ Potential as a Gate Dielectric of the Next Nano MISFET Transistor

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Abstract: The current gate dielectric thickness of MOSFET (metal–oxide–semiconductor–field–effect–transistor) is down to 1 nm which can not prevent boron diffusion from electrodes through the ultra thin gate oxide. Hence, the quest for new dielectric materials as alternatives to silicon dioxide is driving many efforts to grow new materials directly on silicon surfaces. We have thus tried to study a group of high-K dielectric materials, here Al₂O₃, for their potential as gate insulators in future generations of silicon based complementary metal–insulator–semiconductor (MIS) devices. In the present work we have grown Al₂O₃ on Si (100) substrate and studied with using surface sensitive techniques. The obtained results show a pure Al₂O₃ film formed on silicon substrate is amorphous and can be a good candidate of the next CMISFET devices.

Key words: Thin film • Nanostructure • Al₂O₃ and surface sensitive technique

INTRODUCTION

Characteristics of current density-voltage and capacitance-voltage were also investigated to evaluate the insulative and interface quality in a Al₂O₃/ SiO₂ metal-oxide-semiconductor structure. According to international technology roadmap for semiconductor (ITRS) anticipations, the CMOS scaling technology has been faced with several barriers and problems due to some issues: 1-Increasing leakage and tunneling current and 2-boron diffusion through the ultra thin gate oxide. These problems cause to deploy new technology and materials for providing additional functional in ICS. In fact, some new technology will be evolutionary additions to current CMOS processes. Others will be revolutionary and will go well beyond the theoretical limits of CMOS scaling.

Hence, the growth of high-K dielectric materials of only a few layers on silicon surfaces has become that the target for the development of industrial process towards the next generations of Si-based electronics. Obviously the processing and analysis of such films are very demanding. The analysis details of the reaction dynamics and structural properties of the Al₂O₃ films.

The present result can be used for studying the electrical properties of ultra thin Al₂O₃ gate dielectric for both n-and p-channel FETs. In fact, the use of Al₂O₃ to replace SiO₂ as gate dielectric can reduce the gate leakage current by several orders of magnitude while maintaining excellent interface quality.

Experimental Details: In this work, the silicon samples are 5 Ohm-Cm, 1 Cm by 1 Cm n- type (p-doped) Si, cut form a 2 mm thick silicon wafer. These samples were then cleaned by Dc-current heating samples at above 1000° C in the furnace without any other treatment. A powder of Al₂O₃ and the Al wire are used for this study. The silicon samples have been polished on one side as purchased and cleaned with acetone in an ultrasonic bath and then rinsed with distilled water. After transfer into the analysis chamber, they are sputtered with Ar⁺ until all carbon contamination in the spectra disappeared. An example of clean Si (100) is shown in Figure1. It is clear that there are no other elements like carbon and oxygen peaks, meaning our samples are definitely clean samples. In addition, we could remove native silicon dioxide from the silicon surfaces. Although Cuha [1] and Morgan [2] and some other researchers [3–6] have established the growth of device quality Al₂O₃ / Si interfaces using layer deposition of Al₂O₃ directly on top of Si (100) surfaces. Therefore, grow Al₂O₃ at high pressure and temperature in the furnace.

We have then evaporated Al wire by passing current through the wire for 10 min in the Ar and O₂ atmosphere inside the quartz tube. The Al₂O₃ could be formed as demonstrated in Figure 2. Of course a Si (100) 2 x 1 surface is covered partially by approximately 0.5 monolayer of Al and oxidized at about 10 min. It comprises from 1 cycle through 6 cycles, as shown in Figure 3.

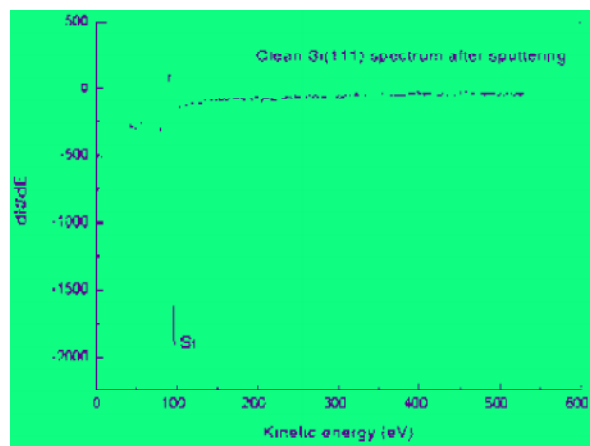


Fig. 1: AES of clean silicon samples

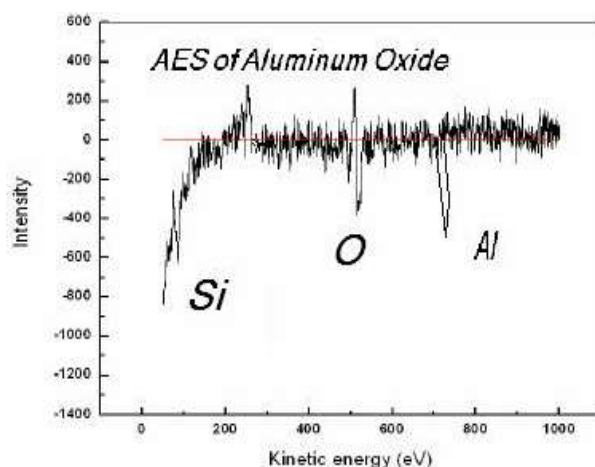
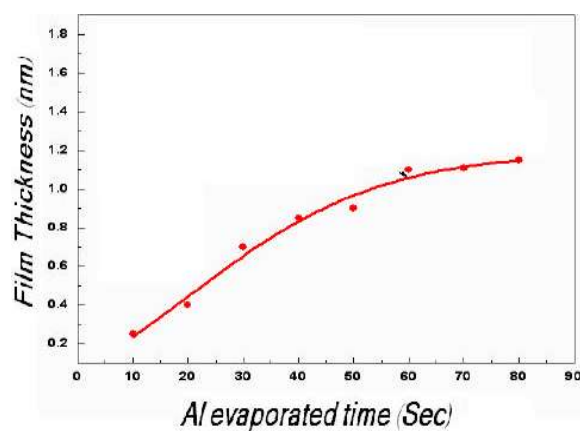
Fig. 2: AES of Al_2O_3 film. There are several peaks due to some significant transitions, which the huge peak has been usually considered in discussionsFig. 3: The self limiting growth of Al_2O_3

Figure 3 indicates that we are not be able to grow thicker than 1.2 nm with the above procedure.

DISCUSSION

As shown in Figure 1, we could clean the samples. After exposing oxygen and evaporating Al on the silicon surface, an ultra thin Al_2O_3 is formed in where after depositing Al-oxide, in the first cycle, some of the oxygen atoms are bounded to silicon atoms. Thickness diagram obtained by Auger electron spectroscopy (AES) indicates that a small amount of oxygen is incorporated into the film. It is accumulated slightly at the interface of the Si/ Al_2O_3 . Saturation of the growth rate with respect to both precursors is verified and the film thickness reveals the Boltzmann function dependency on the number of deposition cycles applied.

We believe that by continuing the aluminum and oxygen exposures on silicon substrate, a nearly thicker Al_2O_3 (up to maximum 3 nm) can be formed in where the all Al atoms made bonds with silicon and oxygen atoms as deposited in Figure 3. However, beyond this, the electrical properties due to band bending demonstrated that the charge and defect densities inside the film at the film-Si interface may stop the film growth. From the point of electrical view, means that a thin Al_2O_3 layer was subsequently deposited on the SiO_2 surface can reduce detrimental surface states indicating the good passivation effect of Al_2O_3 film.

CONCLUSIONS

High-k gate oxides such as Al_2O_3 are advantageous since they enable a reduction of leakage current through the ultra thin silicon oxide film. To address this issue, we focused on the interface between the gate dielectric and the active material and we explored the effects of functionalizing the Al_2O_3 surface by means of self-limiting growth.

However, surface passivity effects of the Al_2O_3 have been confirmed by self limiting growth behavior. We expect that the gate leakage current is several orders of magnitude lower than that of the reference high-electron mobility transistors at a positive gate bias. However, the barrier improvement observed for one $\text{Al}_2\text{O}_3/\text{SiO}_2$ bilayer and two $\text{Al}_2\text{O}_3/\text{SiO}_2$ bilayers could not be explained using present work and should be studied in the future.

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