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# Design of High Performance and Low Power Double Edge-Triggered Clocked Storage Element

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**Abstract:** Double Edge-Triggered Flip-Flop (DETFF) allows maintaining a constant throughput while operating at only half the clock frequency as compared to Single Edge-Triggered Flip-Flop. This paper proposes a high performance and low power dual edge triggered flip-flop. In this work four previously published dual edge triggered flip-flops (DETFFs) are compared with the proposed design for their power dissipation, performance and power-delay-product (PDP). All simulations are performed on TSpice using BSIM models in 130 nm process node. The simulation results show that the proposed design has an improvement in terms of power dissipation, delay and PDP without increasing silicon area. The proposed design is suitable for low power and high speed applications.

**Key words:** Clocked Storage Elements · Power Consumption · Speed · Transmission Gate · CMOS Technology

## INTRODUCTION

In recent years, with the raise in demand of electronic devices with longer battery life, low cost and high speed, there is a regular need of new circuits design to carry out these requirements. Since digital Very Large Scale Integration (VLSI) circuits are considered to be a combination of interconnected flip-flops and logic gates, choosing appropriate topology is of fundamental importance [1]. Sequential logic circuits such as registers, memory elements, counters etc. are heavily used in the implementation of VLSI. Moreover to sample and store the input data through flip-flops these systems use clock signals for synchronization of components, so power dissipation of VLSI chips is to be a progressively more crucial problem. Therefore improvement of such circuits, as reduction in power consumption without weakening other characteristics, is of prime importance to VLSI technology [2].

In synchronous systems, data arrangement and operation take place by a time relationship which is fixed and pre-determined. Flips-flops and latches are elementary building blocks of digital electronics systems used in computers, communications along with clock. The flip- flops and latches also controlled the timings of computations. Flip-flops and latches are clocked storage elements which stores value functional to their inputs [3, 4]. Storage elements commonly store its value as charges on a capacitor. Depending on how it maintains its values beside charge leakage CMOS flip-flop can be static or dynamic. A static flip-flop retains its value by means of positive feedback.

**Double Edge-triggered Flip-Flops:** Edge triggered flip-flop circuits may be classed into two types.

The first one latches data on either the positive or negative edge of a clock pulse that is called single edge triggered (SET) flip-flops [5]. Second is double edge triggered flip-flop (DETFF), which can trigger output at both the rising and falling edges of a clock [6]. A double edge triggered flip-flop has an upper path and a lower path between input data and an output node. The upper path includes a switch connection to a first data loop and the lower path includes a switch connected to a second data loop. The first data loop and second data loops share a forward path having data inverting circuit. In addition,

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there is a feedback path with each loop which includes only one element as a switch [2]. Compared to rising/falling edge-triggered flip-flop which process data only at the rising/falling transition of the clock, the DET flip-flop reduces the clock rate by half or doubles the rate of data processing thereby, either reducing power consumption or increasing the data throughout in the clock circuit respectively. Thus there are possible chances of reduced power and high-speed operation. However the implementation of conventional static DET needs many transistors and spends too much silicon area to make them an attractive design in VLSI circuits. Though many contributions have been given to the art of DET flip-flops, a need evidently occurs for a design that still further improves the relative power consumption of DET flip-flops.

Clock related power is one of the most important components of the dynamic power consumption. The total clock related power dissipation in synchronous VLSI circuits is classified into three major components [7, 8]:

- Power dissipation in the clock network
- Power dissipation in clock buffers
- Power dissipation in flip-flops.

The clock frequency is linearly proportional to the clock power dissipation. Although the clock frequency is calculated by the system specification, it can be shortened by using dual edge triggered flip-flops (DETFFs). As its name implied, DETFF responds to both rising and falling clock edges. Hence, it reduces the clock frequency by half while keeping the same data throughout. As a result, there is a reduction in power consumption of the clock distribution network, making DETFFs desirable for low power applications. The usage of DETFFs for high performance applications, offers certain benefits. Since the clock speed is reduced by a factor of two, one does not need to propagate a relatively high speed clock signal.

A classic DET flip-flop can be represented by Figure 1. In this classic configuration, two opposite polarity level-sensitive latches are connected in parallel; the output is then multiplexed at the output stage [9].

**Existing Double Edge Triggered Design:** Several DET flip-flop have been described by replicating the latch elements of a SET flip-flop and multiplexing the output. This paper compares four previously published DET flip-flops with a proposed design for their delay, PDP and power consumption.

The Double edge-triggered flip-flop shown in Figure 2 was proposed by R. Hossain [6]. The structure is based on master-slave pattern. It has two data path, an upper data path and a lower data path. The upper data path consists of MN1, INV2 and MN3; the lower data path consists of MN2, INV3 and MN4. The input data is in connection with MN1 and MN2 and output is taken from INV5 whose input in turn connected with MN3 and MN4. Each data path have loop within itself for retaining charge levels functionally static. The feedback path in each loop includes an inverter and a PMOS which is switched by clock. The loops are isolated from each other. When the clock pulse changes from low to high upper loop holds data and lower loop samples the data. But when clock pulse changes from high to low the upper loop switches to sample data and lower loops holds the data.

The Double edge-triggered flip-flop shown in Figure 3 was proposed by G.M. Blair [10]. The structure is based on master-slave pattern. It has two data path, an upper data path and a lower data path. The upper data path consists of TG1, INV2 and TG3; the lower data path consists of TG2, INV4 and TG4. The input data is in connection with TG1 and TG2 and output is taken from INV5 whose input in turn connected with TG3 and TG4. The Transmission gates used in both the data path are clocked such that upper data path works as negative edge triggered flip-flop and lower data path works as positive edge triggered flip-flop. Each data path have loop within itself for retaining charge levels functionally static. The feedback path in each loop includes an inverter and transmission gate.

The Double edge-triggered flip-flop shown in Figure 4 was proposed by Imran A. Khan [11]. The structure is based on master-slave pattern. It has two data path, an upper data path and a lower data path. The upper data path consists of TG1, INV1 and TG2; the lower data path consists of TG3, INV3 and TG4. The input data is in connection with TG1 and TG3 and output is taken from INV5 whose input in turn connected with TG2 and TG4. The Transmission gates used in both the data path are clocked such that upper data path works as positive edge triggered flip-flop and lower data path works as negative edge triggered flip-flop. Each data path have loop within itself for retaining charge levels functionally static. The feedback path in each loop includes an inverter and Pass Transistor P1 in upper data path loop and P2 on lower data path loop.

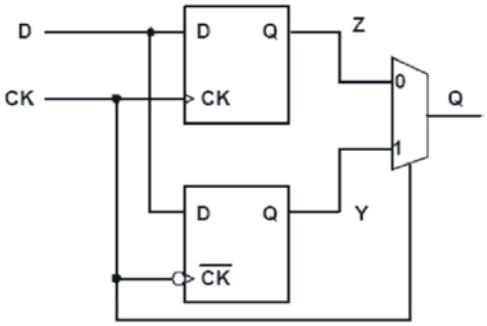


Fig. 1: Representation of DETFF

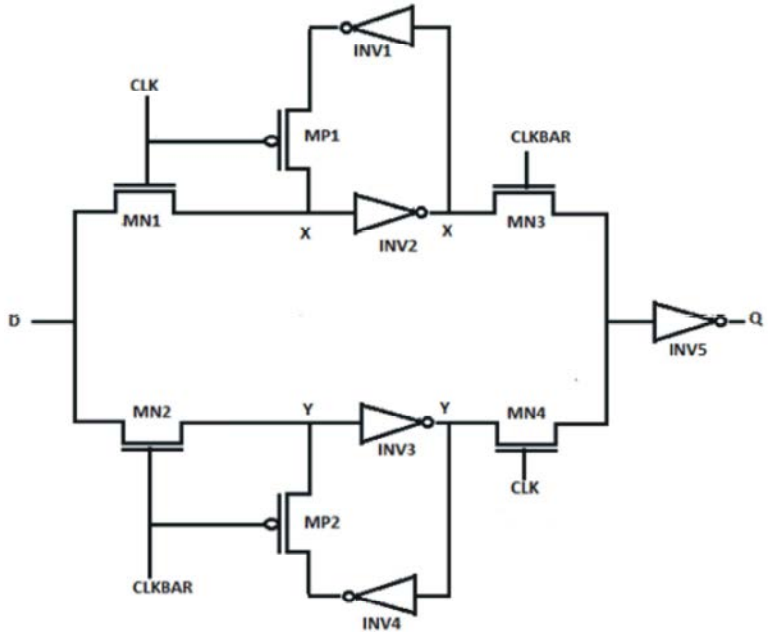


Fig. 2: DETFF proposed by Hossain

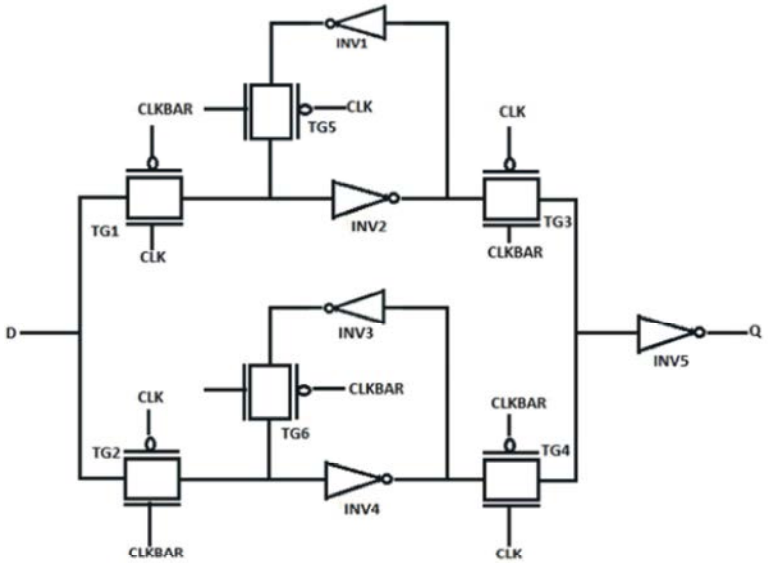


Fig. 3: DETFF proposed by G.M. Blair

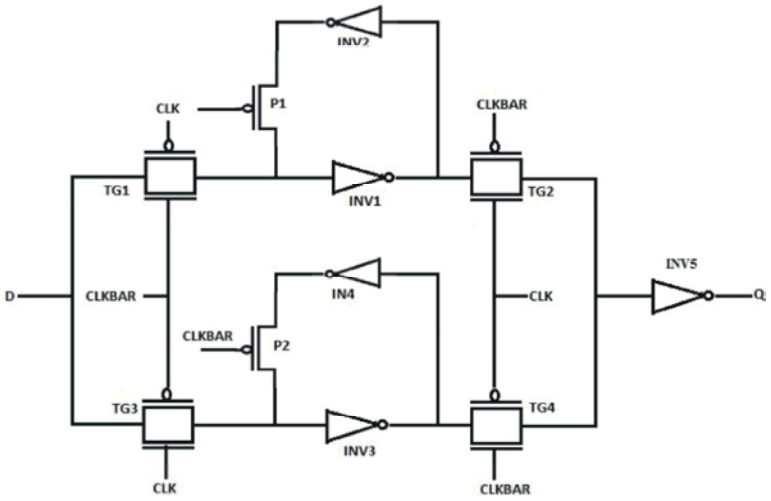


Fig. 4: DETFF proposed by Imran

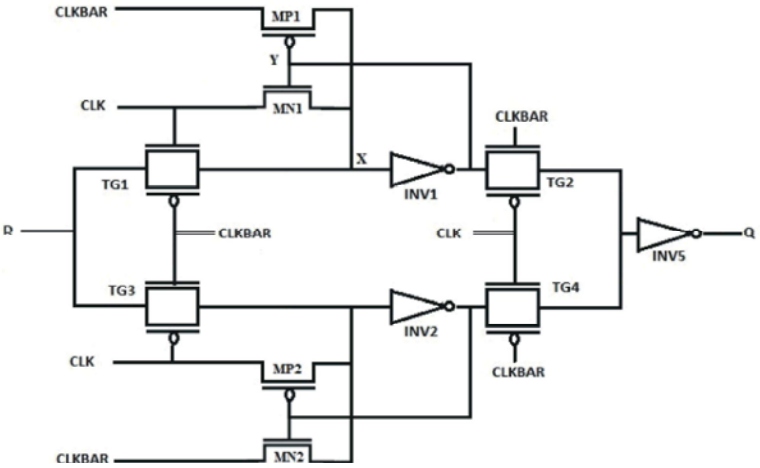


Fig. 5: DETFF proposed by M. Pedram

Table 1: CMOS Simulation parameter

| | |
|---|---|
| 130 nm CMOS Technology | |
| Min. Gate Width: | 0.26um |
| Max. Gate Width: | 1.04um |
| MOSFET Model: | BSIM3 |
| Nominal Conditions: | $V_{dd}$=1.6V |
| Duty Cycle | 50% |
| Clock Frequency | 400MHz |

The DET flip-flop shown in Fig. 5 is proposed by M. Pedram [12]. In this flip-flop the input data controls the passing of the clock signals in the feedback path of both latches used in the circuit. If clock = 1, TG1 turns on, when D = 0, Node X discharges to 0 and Node Y switches to 1 due to this MN1 turns on. As a result, MN1 and TG1 attempt to write 0 and 1(2 different voltages) simultaneously onto Node X. This voltage conflict is present until the clock =0. So this structure allows large current to flow at the input. Similarly in other cases power consumption is increased. Another problem with this circuit is reduction of noise margin. The degraded voltage level at Node X also causes a direct path current in the following inverters. This increases power consumption.

**Proposed Double Edge Triggered Flip-Flop:** The proposed design of double edge-triggered flip-flop is shown in Figure 6. The structure is based on master-slave pattern. It has two data path, an upper data path and a lower data path. The upper data path consists of pass transistor (MN1), INV1 and TG1; the lower data path consists of pass transistor (MN2), INV3 and TG2. The input data is in connection with pass transistor (MN1) and pass transistor (MN2) and output is taken from INV5 whose input in turn connected with TG1 and TG2. The Pass transistor and transmission gates used in both the data path are clocked such that upper data path works as positive edge triggered flip-flop and lower data path

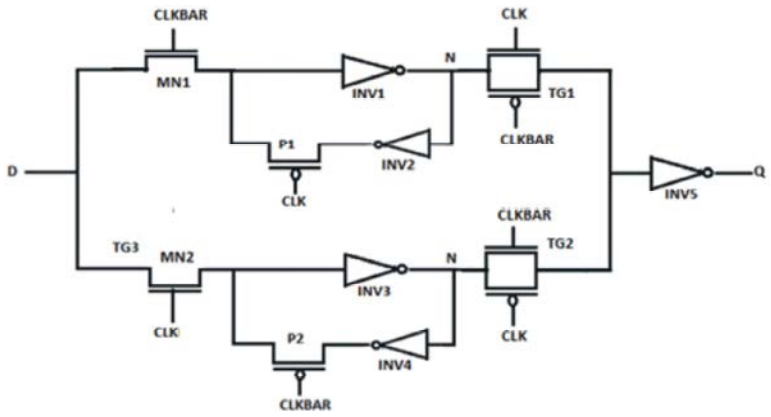


Fig. 6: Proposed DET flip-flop

works as negative edge triggered flip-flop. Each data path have loop within itself for retaining charge levels functionally static. The feedback path in each loop includes an inverter and pass transistor P1 in upper data path loop and P2 in lower data path loop. Proposed design is identical to Figure 4, except master part of the circuit in which the proposed flip-flip uses pass transistors (NMOS) instead of transmission gates. This improves the power efficiency of the flip-flop. So the main advantages of the proposed design are increase in performance and low power consumption with less transistor counts.

**Simulation**

**Analysis:** We can evaluate the flip-flops at different parameters. For example we can compare delay, power consumption, power delay product (PDP), energy delay product (EDP) of the flip-flops. In this paper, we compared delay, PDP and power consumption of the flip-flops.

**Optimization:** Power increases on optimizing a circuit for delay and vice versa. The design has been simulated to attain minimum power consumption. For fair comparison all the flip-flops have same aspect ratios of transistors. The transistors of all flip-flops, that are not located on critical path, are implemented with minimum size to reduce area overhead and to minimize power dissipation.

**Experimental Result Comparison:** To evaluate performance, different flip-flops have been analyzed and a new flip-flop is proposed in 130nm CMOS technology. All the simulations are carried out by varying clock frequency from 100 MHz to 1GHz and supply voltage from 1.2V to 2.0V. Table 2 shows power of various flip-flops with the variations in data pattern. For this table, the supply voltage is 1.6V and clock frequency is 400MHz. From this table it is clear that the proposed flip-flop has improvement in terms of average power consumption when compared with existing DETFF.

Table 3 shows power consumption of various flip-flops with the variations in clock frequency at 1.6V supply voltage and 50% data activity. Simulation result shows that DETFF-Hossain is failed at 1 GHz frequency. From this table it is clear that the proposed flip-flop has improvement in terms of average power consumption for all clock frequencies except 250MHz than existing DETFF. Table 4 shows power consumption of various flip-flops with the variations in supply voltage for 400MHz clock frequency and 50% data activity. Simulation result shows that DETFF-Hossain failed at 1.2V and 1.3V supply voltages. The proposed flip-flop has lowest power consumption for all supply voltages when compared with existing DETFFs.

Table 5 shows average delay of various flip-flops with the variations in supply voltage. For this table, the clock frequency is fixed at 400MHz and data pattern is 1111010110010000. Simulation result shows that DETFF-Hossain failed at 1.2V and 1.3V supply voltages. From this table it is clear that the proposed flip-flop has improvement in terms of average delay than existing DETFFs except DETFF-Blair and DETFF-Pedram at 1.3V supply voltage and DETFF- Imran at 1.8V supply voltage. Table 6 shows Set-up time and Hold time of various flip-flops. For these tables, the clock frequency is fixed at 400MHz, data pattern is 1111010110010000 and supply voltage is 1.6V. Figure 7 shows PDP with supply voltage variation for 400MHz clock frequency and 50% data activity. Figure shows that DETFF-Hossain failed at 1.2V and 1.3V supply voltages and the proposed DETFF has the lowest PDP for all supply voltages than existing DETFFs except one condition; at 1.3V supply voltage DETFF-Blair has lesser PDP than the proposed DETFF. So, the proposed DETFF is best suitable for low power and high performance applications.

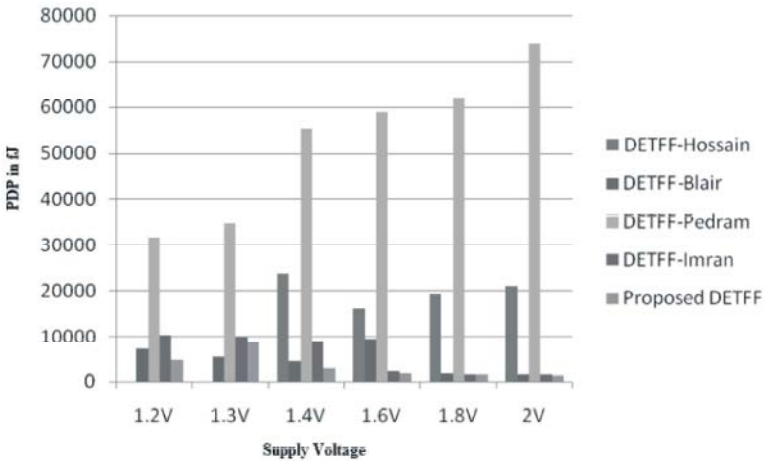


Fig. 7: PDP with supply voltage variation

Table 2: a) Power consumption in µW for different data pattern

| Data Pattern | DETFF-Hossain | DETFF-Blair | DETFF-Imran | DETFF- Pedram | PROPOSED DETFF |
|---|---|---|---|---|---|
| 11111111 | 42.1 | 38.6 | 35.3 | 217.4 | 32.5 |
| 11111111 | | | | | |
| 00000000 | 45.8 | 38.4 | 42.5 | 386.4 | 37.4 |
| 00000000 | | | | | |
| 11110101 | 64.1 | 49.0 | 49.1 | 307.4 | 45.4 |
| 10010000 | | | | | |
| 11001100 | 64.5 | 48.0 | 49.1 | 303.4 | 46.0 |
| 11001100 | | | | | |
| 10101010 | 85.7 | 59.5 | 61.6 | 313.2 | 59.1 |
| 10101010 | | | | | |
| 01000000 | 51.4 | 41.0 | 44.9 | 377.0 | 39.9 |
| 00000000 | | | | | |

Table 2: b) Improvement in power consumption of proposed FF over existing flip-flops

| Data Pattern | Improvement over DETFF- Hossain | Improvement over DETFF- Blair | Improvement over DETFF- Imran | Improvement over DETFF- Pedram |
|---|---|---|---|---|
| 11111111 | 22.80% | 15.80% | 7.93% | 85.05% |
| 11111111 | | | | |
| 00000000 | 18.34% | 2.60% | 12.00% | 90.32% |
| 00000000 | | | | |
| 11110101 | 29.17% | 7.35% | 7.54% | 85.23% |
| 10010000 | | | | |
| 11001100 | 28.68% | 4.17% | 6.31% | 84.84% |
| 11001100 | | | | |
| 10101010 | 31.04% | 0.67% | 4.06% | 81.13% |
| 10101010 | | | | |
| 01000000 | 22.37% | 2.68% | 11.14% | 89.42% |
| 00000000 | | | | |

Table 3: a) Power consumption in µW with clock frequency variation

| Clock Frequency | DETFF-Hossain | DETFF-Blair | DETFF-Imran | DETFF-Pedram | PROPOSED DETFF |
|---|---|---|---|---|---|
| 100MHz | 34.7 | 30.6 | 20.9 | 279.04 | 20.2 |
| 200MHz | 45.4 | 29.1 | 29.5 | 287.91 | 28.5 |
| 250MHz | 27.7 | 35.5 | 37.8 | 294.59 | 39.0 |
| 400MHz | 64.1 | 49.0 | 49.1 | 307.4 | 45.4 |
| 1GHz | Failed | 105.1 | 105.5 | 360.4 | 99.9 |

Table 3: b) Improvement in power consumption of proposed FF over existing FFs

| Clock Frequency | Improvement over DETFF- Hossain | Improvement over DETFF-Blair | Improvement over DETFF- Imran | Improvement over DETFF- Pedram |
|---|---|---|---|---|
| 100MHz | 41.79% | 33.99% | 3.35% | 92.76% |
| 200MHz | 37.22% | 2.06% | 3.39% | 90.10% |
| 250MHz | -28.97% | -8.97% | -3.08% | 86.76% |
| 400MHz | 29.17% | 7.35% | 7.54% | 85.23% |
| 1GHz | ---------- | 4.95% | 5.31% | 72.28% |

Table 4: a) Power consumption in µW with supply voltage variation

| Supply Voltage | DETFF-Hossain | DETFF-Blair | DETFF-Imran | DETFF- Pedram | PROPOSED DETFF |
|---|---|---|---|---|---|
| 1.2V | Failed | 28.3 | 26.6 | 108.0 | 25.4 |
| 1.3V | Failed | 33.8 | 31.3 | 146.6 | 29.0 |
| 1.4V | 44.6 | 37.7 | 35.8 | 192.0 | 32.6 |
| 1.6V | 64.11 | 49.0 | 49.1 | 307.4 | 45.4 |
| 1.8V | 96.0 | 61.7 | 61.9 | 465.9 | 60.6 |
| 2.0V | 125.83 | 75.6 | 77.7 | 667.6 | 75.0 |

Table 4: b) Improvement in power consumption of proposed FF over existing FFs

| Supply Voltage | Improvement over DETFF- Hossain | Improvement over DETFF-Blair | Improvement over DETFF- Imran | Improvement over DETFF- Pedram |
|---|---|---|---|---|
| 1.2V | ------ | 10.25% | 4.51% | 76.48% |
| 1.3V | ------ | 14.20% | 7.35% | 80.22% |
| 1.4V | 26.91% | 13.53% | 8.94% | 83.02% |
| 1.6V | 29.18% | 7.35% | 7.54% | 85.23% |
| 1.8V | 36.88% | 1.78% | 2.10% | 86.99% |
| 2.0V | 40.40% | 0.79% | 3.47% | 88.77% |

Table 5: a) Delay (in picoseconds) with the variation in supply voltage

| Supply Voltage | DETFFHossain | DETFF-Blair | DETFF-Imran | DETFF- Pedram | PROPOSED DET FF |
|---|---|---|---|---|---|
| 1.2V | ------ | 254.07 | 388.23 | 292.81 | 187.87 |
| 1.3V | ------ | 155.22 | 315.44 | 237.32 | 296.31 |
| 1.4V | 529.71 | 118.55 | 249.14 | 288.15 | 92.08 |
| 1.6V | 250.44 | 190.17 | 46.35 | 191.17 | 39.62 |
| 1.8V | 199.91 | 29.4 | 25.16 | 133.48 | 25.56 |
| 2.0V | 166.41 | 20.82 | 19.05 | 110.84 | 18.76 |

Table 5: b) Improvement in delay of proposed FF over existing FFs

| Supply Voltage | Improvement over DETFF- Hossain | Improvement over DETFF-Blair | Improvement over DETFF- Imran | Improvement over DETFF- Pedram |
|---|---|---|---|---|
| 1.2V | ----- | 26.06% | 51.61% | 35.84% |
| 1.3V | ------ | -47.62% | 6.06% | -19.91% |
| 1.4V | 82.62% | 22.33% | 63.04% | 68.04% |
| 1.6V | 84.18% | 79.17% | 14.52% | 79.27% |
| 1.8V | 87.21% | 13.06% | -1.56% | 80.85% |
| 2.0V | 88.73% | 9.89% | 1.52% | 83.07% |

Table 6: a) Set-up time and hold time CLK=0-1, INPUT=1-0

| Time (pS) | DETFF-Hossain | DETFF-Blair | DETFF-Imran | DETFF- Pedram | PROPOSED DETFF |
|---|---|---|---|---|---|
| Set-up time | 12.10 | 9.84 | 14.48 | 8.88 | 14.44 |
| Hold time | 26.83 | 19.69 | 14.48 | 6.51 | 7.22 |

Table 6: b) Set-up time and hold time CLK=0-1, INPUT=0-1

| Time (pS) | DETFF-Hossain | DETFF-Blair | DETFF-Imran | DETFF- Pedram | PROPOSED DETFF |
|---|---|---|---|---|---|
| Set-up time | 3.05 | 1.54 | 2.26 | 2.77 | 2.03 |
| Hold time | 21.20 | 14.57 | 7.22 | 14.34 | 15.90 |

Table 6: c) Set-up time and hold time CLK=1-0, INPUT=1-0

| Time (pS) | DETFF-Hossain | DETFF-Blair | DETFF-Imran | DETFF- Pedram | PROPOSED DETFF |
|---|---|---|---|---|---|
| Set-up time | 14.44 | 7.29 | 14.44 | 4.78 | 10.60 |
| Hold time | 16.01 | 8.96 | 16.01 | 9.56 | 4.75 |

Table 6: d) Set-up time and hold time CLK=1-0, INPUT=0-1

| Time (pS) | DETFF-Hossain | DETFF-Blair | DETFF-Imran | DETFF-Pedram | PROPOSED DETFF |
|---|---|---|---|---|---|
| Set-up time | 7.22 | 14.57 | 9.22 | 9.56 | 10.60 |
| Hold time | 7.22 | 14.57 | 8.01 | 4.78 | 11.75 |

## DISCUSSION AND CONCLUSION

The paper proposed a new design of static master slave double edge-triggered flip-flop in 130nm CMOS Technology. The proposed design is compared with the existing double edge-triggered flip-flop designs. Power outcome interpret that proposed flip-flop has improvement in terms of total power dissipation when compared with existing designs. The proposed DET flip-flop consumes up to 92.76% (13.81 times) lesser power than the existing DET flip-flops. The proposed design also illustrates considerable improvement in terms of propagation delay and PDP as compared to existing designs. The simulation results show that the proposed DET flip-flop has up to 88.73% (8.87 times) shorter delay and up to 98.10% (52.59 times) lesser PDP as compared to the existing DET flip-flops. The proposed design is suitable for low power and high speeds applications.

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