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Design of Fully Differential CMOS Amplifier For Clipping Control Circuit

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Abstract: This paper describes the design of a fully differential CMOS amplifier for clipping control circuit. The amplifier with specification of low settling time less than 5ns, high dynamic range above 90dB and low power supply of 3 volt is designed and realized in a 0.35 μm CMOS process with 3 volt power supply. Simulation confirm the presented design.

Key words: Differential amplifier .dynamic range . settling time

INTRODUCTION

The importance of analog circuits using low supply voltage is enormously increasing in recent past [1-3]. Specially large component densities demands lower power consumption. The power consumption can be minimized either by reducing the supply voltage or current. Since transistor noise is dependent on current, therefore, for high performance analog circuit, reduction in current beyond certain limit is not recommended and therefore reasonable method for power consumption is to reduce power supply. A transconductance amplifier for A/D converters has been designed [4]. In this paper, differential CMOS amplifier for clipping control circuit with low Settling time, low power supply and high dynamic rang is designed.

The paper is organized as follows. First, the considerations about topology, second the design analysis for topology are presented. Finally, simulation results is presented which verify that our design meets the required specifications.

SELECTION OF TOPOLOGY

In choosing a topology [4], the following points should be taken into account.

High dynamic range requirements of the amplifier which dictates that a relatively large compensation must be used to keep the total output noise at a minimum level.

- Fast settling, implies that the amplifier must be able to source large currents to charge capacitor to avoid slew limitations [4].

The comparison of performance of various op-amp topologies [5] is shown in Table 1.

Because of the high gain requirement, at least two stage amplifier is required. Since we need high gain and high swing for clipping control circuit thereby stage 1 and stage 2 should have high gain and high swing respectively [5]. Therefore first stage will be selected as Telescopic amplifier and second stage, class AB Amplifier as shown in Fig. 1.

Main circuit: To maintain stability in a two-stage amplifier, some form of compensation must be applied inside the feedback loop. One may choose to employ standard Miller compensation, which places a pole-splitting capacitor between the output of the first stage and the output of the second stage. We employ cascode compensation [6, 7], which places the compensation capacitor between the first cascode node in the first stage and the output of the second stage as shown in Fig. 2.

Biasing network: In order to maximize the performance, a robust biasing circuit must be employed. We use the high-swing cascaded current mirror to maximize robustness over process and supply voltage variation while also providing excellent current mirroring as shown in Fig. 3.

Common mode feedback: For proper operation of a fully differential amplifier, common mode feedback (CMFB) is required to fix the voltages at high

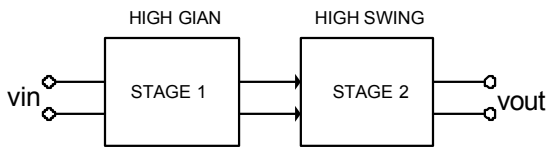

Fig. 1: Two stage topology

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Table 1: The comparison of performance of various op-amp topologies

Amplifier type	Gain	Swing	Speed	Power	Noise
Telescopic	Medium	Medium	Highest	Low	Low
Folded-cascode	Medium	Medium	High	Medium	Medium
Two-stage	High	Highest	Low	Medium	Low
Gain-Boosted	High	Medium	Medium	High	Medium

Table 2: Transistor specifications

	W/L (um um^{-1})	Id (mA)	Vdsat (mV)	Gm (mS)	ro (kO)	Cg (pF)	Cd (pF)
M1	2145/0.5	3.9868	93.5	67.85	2.50	5.0778	2.3852
M2	2145/0.5	3.9868	93.5	67.85	2.50	5.0778	2.3852
M3	1095/1	3.9868	351.0	20.03	2.70	4.9253	1.8654
M4	1095/1	3.9868	351.0	20.03	2.70	4.9253	1.8654
M5	1095/1	3.9868	371.0	17.65	0.36	4.8870	1.7386
M6	1095/1	3.9868	371.0	17.65	0.36	4.8870	1.7386
M7	2145/0.5	3.9868	96.24	69.06	2.02	5.0072	2.1828
M8	2145/0.5	3.9868	96.24	69.06	2.02	5.0072	2.1828
M9	1.1/0.35	0.2028	351.0	1.0213	126.81	0.2440	0.0930
M70	3637.5/0.5	5.5999	150.8	63.90	0.98	8.8734	5.4020
M73	3637.5/0.5	5.2248	138.9	58.00	3.81	2.3056	0.99338
M80	890/0.5	5.5988	150.8	63.90	0.98	8.8734	5.40200
0M83	890/0.5	5.2215	138.9	58.00	3.81	2.3056	0.99338

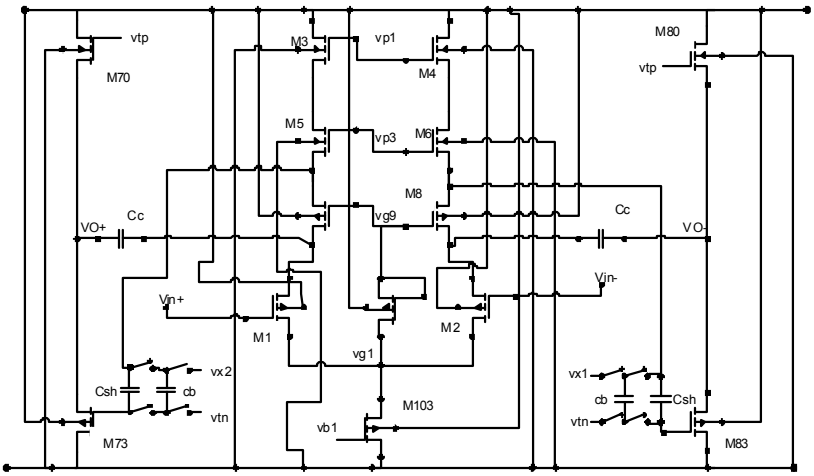

Fig. 2: Operational amplifier with class AB output stage

impedance nodes in the circuit to their desired values. Since we employ a two stage design with two inversions, the CMFB also must be inverting. This is accomplished by a switched-capacitor circuit and PMOS differential pair which adjusts the common mode level of the first stage by either injecting current into or leaking current from the input terminals as needed. The common mode output of the first stage is set to the point which minimizes the quiescent current in the second stage. The common mode voltage of the second stage is also dynamically adjusted using the transistors MF1 and MF2. These transistors help to correct the inherent imbalance in pulling between NMOS in PMOS in a class AB stage during switching. This Circuit is shown in Fig. 4. The transistor Specifications is shown in Table 2.

DESIGN ANALYSIS

Dynamic range: First we determined the maximum total output noise that we could tolerate for a given output swing. This has direct effect on determining the size of the compensation capacitor and feedback capacitor to give the desired dynamic range. We

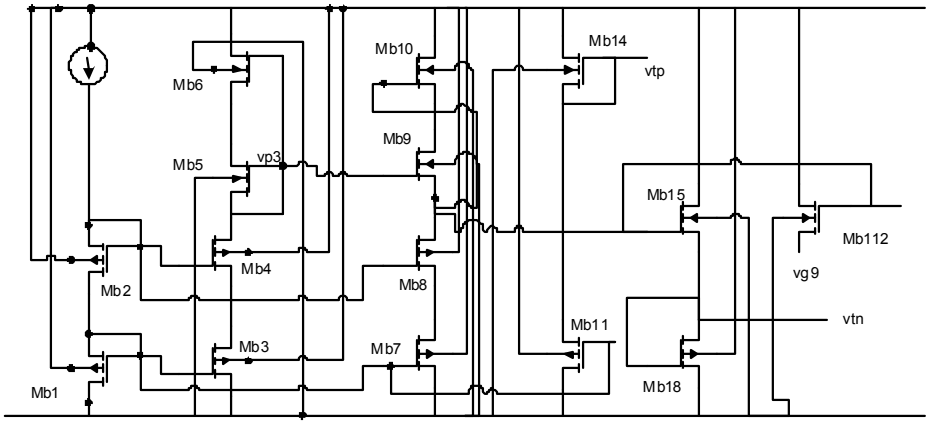

Fig. 3: Bias circuit

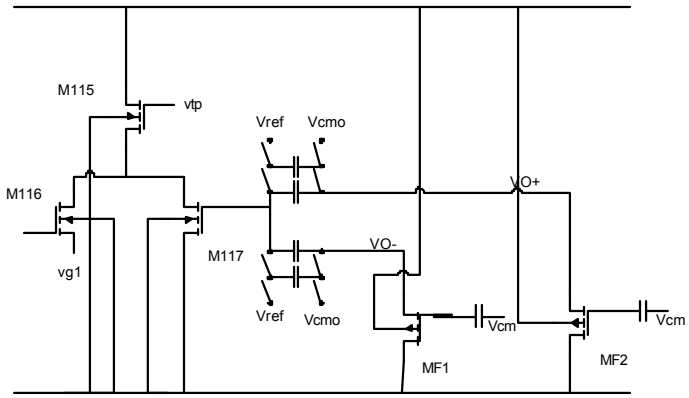

Fig. 4: Common mode feedback circuit

initially assume that have a single-ended output swing of 2.5V, which corresponds to a differential swing of 5V peak-to-peak. The Dynamic Range (DR) is defined as:

$$DR = 10\log\left[\frac{P_{peak}}{P_{noise}}\right] = 10\log\left[\frac{\frac{1}{8}v_{omax}^{2}}{\overline{v_n}}\right] \geq 90db$$

$$P_{peak\_signal} = \frac{1}{8}V_{omax} \quad (1)$$

$$= \frac{1}{2}\left(V_{DD} - V_{D(73,83)}^{sat} - V_{D(70,80)}^{sat}\right)$$

Using Eq. 1 and a 5V p-p output swing, we find that we need to keep the total integrated output noise voltage below 3.125 nV2 in order to meet 90dB of dynamic range.

$$P_{noise} = 2\cdot\frac{2}{3}\cdot\frac{k\cdot T}{C_C}\cdot\frac{1}{f}\cdot n_f = V_{noise}^2 \quad (2)$$

$$F = \frac{C_s}{3C_s + C_{g,M1}} \quad (3)$$

$$n_f = 1 + \frac{g_{m3}}{g_{m1}}$$

As a conservative starting point, we assume that F = 1/4 and nf = 2. Solving for Cc, we obtain Cc = 14pF. Remember that, we neglected the noise of the 6 cascode transistors, which contribute approximately 50% more noise than input transistors alone. Correspondingly, we increase the capacitance and begin with Cc = 25pF.

Settling time: The settling time is combination of two parts i.e., 'linear' and 'slewing' settling times. During slewing, the maximum amount of current is drawn from the amplifier to charge the capacitor. Since we are using a class AB output stage, the second stage does not experience "slewing". For the first stage, the slew rate is given by:

$$SR = \frac{I_1}{C_c} \quad (4)$$

$$t_s = t_{slew} + t_{lin} \leq 5ns \quad (5)$$

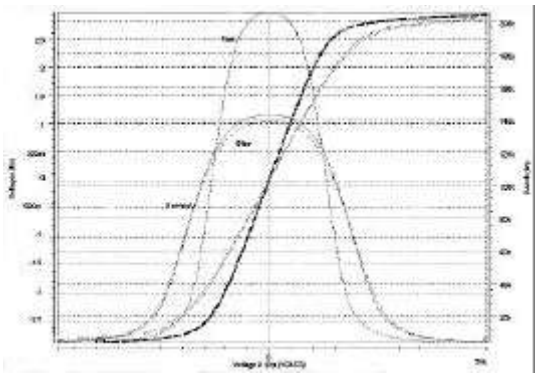

Fig. 5: DC gain and output voltage swing

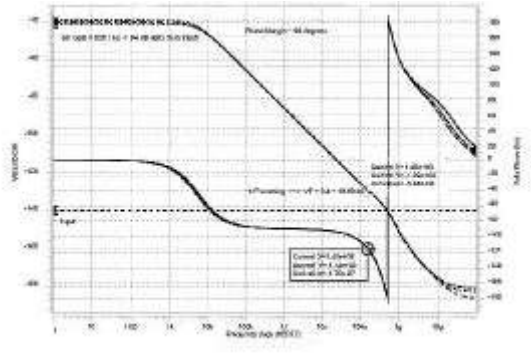

Fig. 6: Open loop frequency response

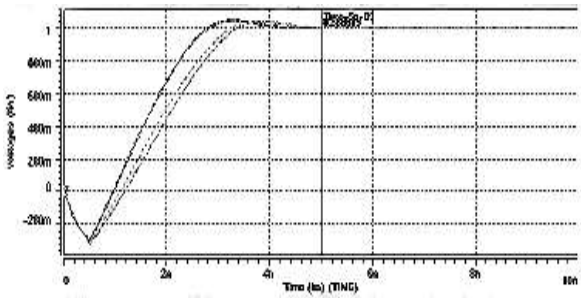

Fig. 7: Transient response showing settling

Combining (4) and (5) we get:

$$t_s = \left(V_{o,step} - \frac{V_{dsat,1}}{F} \right) \frac{1}{SR} - \frac{1}{F\omega_u} \ln\left(\varepsilon \frac{FV_{o,step}}{V_{dsat,1}} \right) \quad (6)$$

$$\omega_u = \frac{g_{m1}}{C_c} = \frac{2I_1}{C_c V_{dsat,1}} \quad (7)$$

Finally, using a V_{DSAT} of 200mV:

$$t_S = \frac{25pF}{I_1} = \left[(2.5V - 4\times 0.2V) - \frac{4\times 0.2V}{2} \ln\left(0.00005 \frac{2.5V}{4\times 0.2V} \right) \right] \leq 5ns$$

First, both slewing and exponential settling times are proportional to C_c/I_1. In order to minimize power while meeting the settling requirement, we needed to use C_c as small as possible limited by the dynamic range requirement. Second, if we select f, about 1/3 and $V_{o,step}$, about 2.5 V, for fixed value of C_c/I_1, the total settling time decreases as $V_d{}^{sat}{}_1$ decreases. But we did not want to put M1 and M2 in weak inversion, since otherwise, matching would be terrible. So the size of the input device was chosen and made sure that for worst process case, $V_d{}^{sat}{}_1$ is still greater than $2nV_t$, which is about 60mW for the technology we are using (n = 1.2). Third, as we mentioned earlier, C_s should not be too small, otherwise, f would become smaller and thus the exponential settling time increases.

SIMULATION RESULT

The simulation results related to gain and output voltage swing is shown in Fig. 5. Also Fig. 6 and 7 shows the frequency response and settling time respectively. It is observed that all goals in the designed are obtained.

CONCLUSION

We have presented the design of a two-stage fully differential CMOS amplifier with a telescopic input stage and a class AB output stage for clipping control circuit. It operate on a 3V power supply, has dynamic rang of 90dB and settling time of less than 5ns. The power consumption of the biasing network, of course, could be greatly reduced through device scaling.

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