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Reliable and Higher Throughput Anti-Collision Technique for RFID UHF Tag

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Abstract: This paper presents a proposed Reliable and Higher Throughput Anti-collision technique (RHTACT) for Radio Frequency Identification (RFID) Class 0 UHF tag. The RHTACT architecture consists of two main subsystems; Pre RHTACT and Post RHTACT. The Pre RHTACT subsystem is to detect any error in the incoming messages. Then the identification bit (ID) of the no error packet will be fed to the next subsystem. The Post RHTACT subsystem is to identify the tag by using the proposed Lookup Table. The proposed system is designed using Verilog HDL. The system is simulated using Modelsim and synthesized using Xilinix Synthesis Technology. The system has been successfully implemented in hardware using Field Programmable Grid Array (FPGA) Virtex II. The output waveforms from the FPGA have been tested on the Tektronix Logic Analyzer for real time verification. Finally the RHTACT architecture is resynthesized using Application Specific Integrated Circuit (ASIC) technology for on-chip implementation. This technology consists of 0.18 µm Library, Synopsys Compiler and tools. From the hardware verification results, it shows that the proposed RHTACT system enables to identify the tags without error at the maximum operating frequency of 80 MHz. The system consumes 13.13mW powers, occupies 11,531 gates and 0.06870 mm^2 area with Data arrival time of 2.72 ns.

Key words: Class 0 tag · Hardware implementation · Real time verification · Power · Area · Gates

INTRODUCTION

In the data management system a significant role of the Data link layer is to convert the unreliable physical link between reader and tag into a reliable link. Therefore, the RFID system employs the *Cyclic Redundancy Check* (CRC) as an error detection scheme. The CRC calculation consists of an iterative process involving Exclusive-ORs and shift register which is executed much faster in hardware compare in software [1].

In addition for reader to communicate with the multiple tags, an anti-collision technique is required. The technique is to coordinate the communication between the reader and the tags. These anti-collision techniques are classified into two; the deterministic and the stochastic/probability techniques.The common deterministic techniques are based on the Tree algorithm such as the Binary Tree and the Query Tree algorithms [2-5]. The common stochastic techniques are based on the Aloha algorithm such as the Aloha, the slotted Aloha and the frame slotted Aloha [6-8]. In the Binary Tree algorithm, the identification process will first search the smallest tag's ID until the largest one follows the Binary Tree sequence. Since this algorithm is a deterministic anti-collision technique, the reader will control the communication between the Tags. Therefore enable production of tag with simple, small, low cost and low power features. However this technique has longer identification time which dependents on the number of existing tags and the identification bit (ID) length.

RHTACT Methodology: In our proposed RHTACT the frame consists of slots and each slot (column) is divided into minislots (rows). The RHTACT architecture identifies eight tags per Read cycle using the proposed Lookup table. The uniqueness of this proposed technique is reducing the tag identification time in the Binary Tree. The existing tags are divided into

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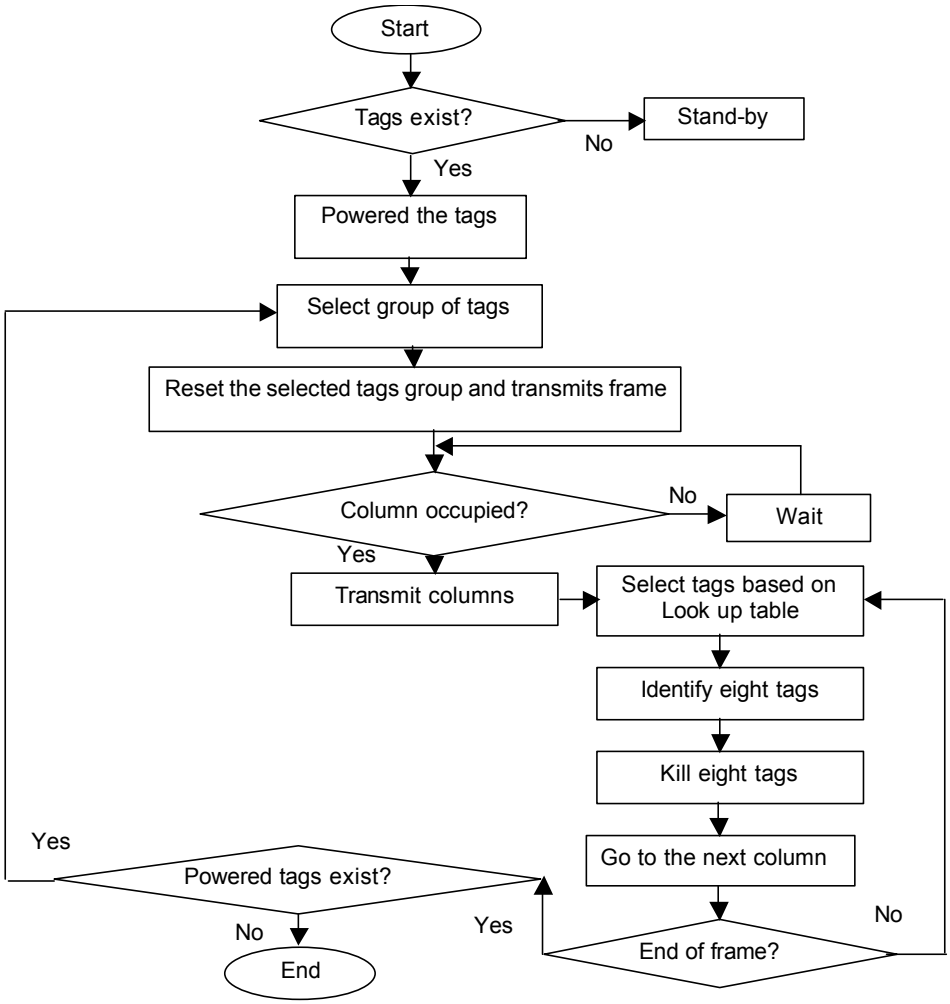
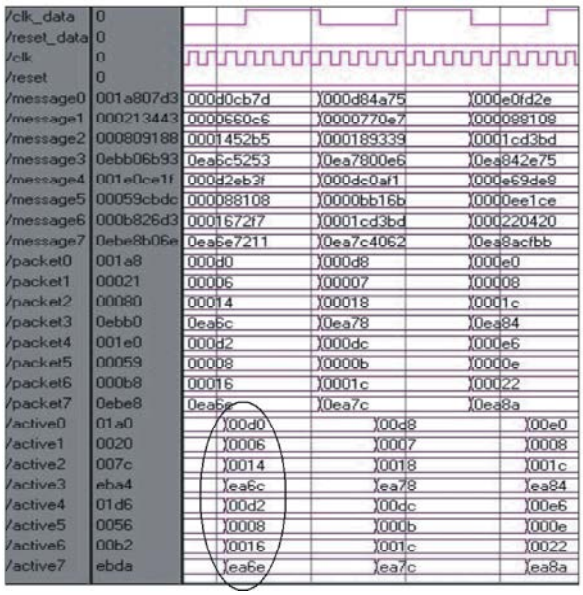


Fig. 1: RHTACT identification Methodology

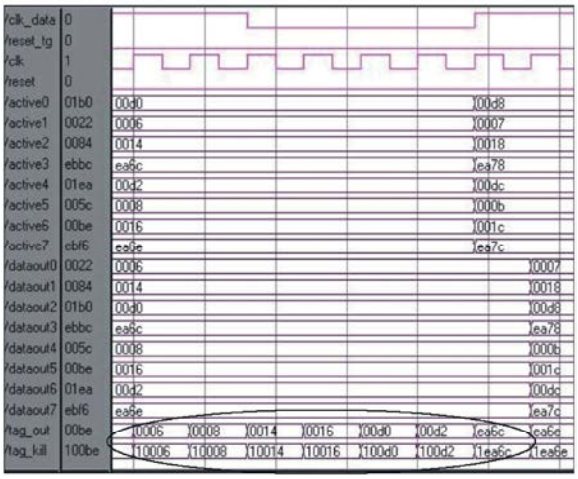
eight in each Read cycle to reduce the required iterations and thus faster the tag identification. This proposed technique does not require the tag to remember the instructions from the reader during the identification process. Thus the tag is treated as an address carrying device only and memory-less tag can be designed which requires very low power. The RHTACT identification methodology is shown in Fig. 1. In RHTACT, bidirectional communications are involved, from the reader to the tag (Downlink) and from the tag to the reader (Uplink). When the reader detects there are tags exist in its interrogation zone, it will power these tags. Then the reader sends the Select-group command based on the tag Prefix or Object Class (OC). The selected tags group will move to the Ready state. Next the Reader transmits Reset signals and its frame. After that the frame is transmitted back to the reader, column by column starting with the first column. This compensates the time required for transmitting the packet to the reader. Therefore for every Read cycle, there are always available packets at the reader waiting for identification.

At the reader, the incoming packets for each link sequentially enter the RHTACT system. The reader selects the incoming packets (IDs) using the proposed Fast-search Lookup table, and then the selected ID will be identified. Based on this proposed Lookup table, the eight IDs will be identified from the smallest value to the largest one in one Read cycle. Then the tag that has been successfully identified will be acknowledged by sending the Kill-tag.

RHTACT Architecture: The RHTACT architecture consists of two subsystem; Pre RHTACT and Post RHTACT (Fig. 4). In the Pre RHTACT, the received messages are fed into the CRC-remover module.



(a) PreRHTACT modules output



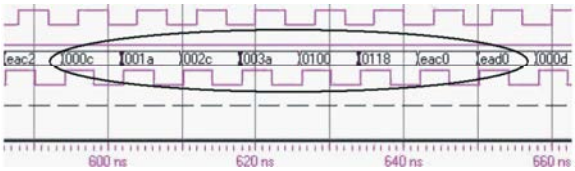
(b) PostRHTACT modules output

Fig. 2 The Behavioral simulation of RHTACT

These received messages will be separated into two; the received packet and the received CRC. These packet and CRC are sent to the CRC-checker module for verification process. The CRC-checker module recalculated the CRC of the received packet. Then, this calculated CRC is compared with the received CRC. If the values are same, means no error, the statusbit is set to its original value i.e. zero. Otherwise or there are errors in the packet, the statusbit is set to two. After that, this updated statusbit is appended to its respective packet.

Finally, the packet with the updated status-bit is fed to the Status-checker module. The Status-checker module will check any errors in the incoming packets.

(a) RHTACT FPGA outpu



(b) RHTACT Place and Route simulation output

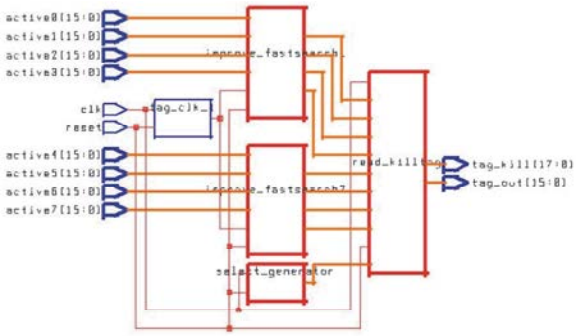
Fig. 3 RHTACT output at 45 MHz

If there are errors, then reset the slot of the respective packet to zero value. Otherwise, fill the slot of the packet with its respective ID. The status-bit is removed from its packet and only the tag's ID will be output to the PostRHTACT [9].

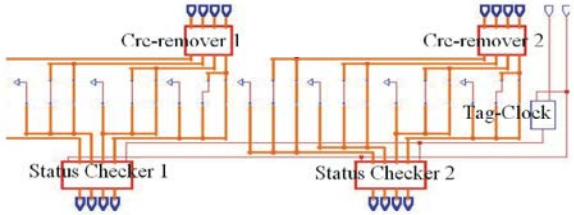
In the PostRHTACT, the active tags are divided into a group of eight for every Read cycle in order to reduce the number of iterations in the identification process. The PostRHTACT reads all the ID bits at once regardless of its length. This is performed by using the word-by-word multiplexing. During the identification process, the Fast-search modules identify the eight tag's IDs simultaneously in one Read cycle which equal to a Tag clock cycle. The module firstly identifies the smallest ID bits and lastly the largest one follows the Binary Tree with a maximum number of eight leaves.

Simulation Results: Verilog HDL codes for the RHTACT architecture have been successfully simulated and verified using the ModelSim XE II/Starter 5.7g tool. The following will discuss the Behavioral simulation waveforms for the selected ports in the RHTACT system as shown in Fig. 2.

At the first Read cycle, for the received messages of $000D0CB7D_{16}$, $0000660C6_{16}$, $0001452B5_{16}$, $0EA6C5253_{16}$, $000D2EB3F_{16}$, 000088108_{16}, $0001672F7_{16}$, and $0EA6E7211_{16}$, their recalculated CRC are $CB7D_{16}$, $60C6_{16}$, $52B5_{16}$, 5253_{16}, $EB3F_{16}$, 8108_{16}, $72F7_{16}$ and 7211_{16} respectively.



(a) PreRHTACT block diagram



(b) PostRHTACT block diagram

Fig. 4: Synthesized block diagram of RHTACT

As a result, the calculated CRCs are equal to the received CRCs which are represented by the four bit of the least significant bit (LSB) of the messages. Since there are no errors in the received messages, the Statusbit of the packets are set to zero, which are represented by the MSB of the packets; $000D0_{16}$, 00006_{16}, 00014_{16}, $0EA6C_{16}$ $000D2_{16}$, 00008_{16}, 00016_{16} and $0EA6E_{16}$ respectively. Finally, the ID of these packets will be fed simultaneously to the Post RHTACT subsystem.

In the Post RHTACT subsystem, two Fast-search modules identify the eight active tags simultaneously starting from the smallest value to the largest one. For examples, for the eight input tag's ID of $00D0_{16}$, 0006_{16}, 0014_{16}, $EA6C_{16}$, $00D2_{16}$, 0008_{16}, 0016_{16} and $EA6E_{16}$ will be identified as 0006_{16}, 0008_{16}, 0014_{16}, 0016_{16}, $00D0_{16}$, $00D2_{16}$, $EA6C_{16}$ and $EA6E_{16}$ respectively. Then these tags are fed simultaneously to the Read-killtag module at the Tag clock negative edge. Finally, the Read-killtag Module will output these eight tags serially, one tag at every system clock cycle starting from the smallest tag's ID to the largest one. Moreover, at the same clock cycle, the identified tag will be killed.

Implementation and Verification: The RHTACT architecture has been implemented in hardware using the Field Programmable Grid Array (FPGA) model Virtex II Xc2v250. The output waveforms from the FPGA have been displayed using the Tektronix Logic Analyzer model TLA 5201 for real time verification. From the result, it shows that the system still enables to identify the tags without errors at the operating frequency of 80 MHz. Fig. 3 shows the FPGA output and its equivalent place and route simulation result at 45 MHz. For examples for the first Read cycle the identified tags are $000C_{16}$, $001A_{16}$, $002C_{16}$, $003A_{16}$, 0100_{16}, 0118_{16}, $EAC0_{16}$ and $EAD0_{16}$ as marked by a circle.

Table 1: Synthesized Output Parameters

Xilinix Parameters	ASIC Parameters
Max. Frequency = 253MHz	Cell area = 0.06870 mm^2
Total gate count = 11 531	Power = 13.133 mW
Connection Delay = 1.16ns	Arrival time = 2.72 ns
Max. pin Delay = 3.96ns	Slack = 0.23 ns

The RHTACT system has been successfully implemented in hardware using FPGA with desired performances. Then the system is implemented on chip using ASIC approach. In this approach the system is resynthesized using 0.18 µm Library, Synopsys Compiler and tools. Table 1 shows the output parameters using two synthesis technology; Xilinix and ASIC.

From the synthesis results, it shows the RHTACT architecture has the maximum operating frequency of 253MHz and the total gates of 11,531. The average connection delay is 1.16 ns and the maximum pin delay is 3.96 ns. Moreover, the RHTACT occupies 0.06870 mm^2 cell area and consumes 13.133 mW powers. The data required time and the data arrival time are 2.72 ns and 2.19 ns respectively.

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