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Design and Optimization of Nanometric Reversible 4 Bit Numerical Comparator

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Abstract: Nowadays reversible logic plays an important role in improving technologies like CMOS design, quantum computing and nanotechnology. In this paper we propose a 4-bit nanometric reversible numerical comparator circuit, which makes our proposed design more efficient and optimal. The major constraint in designing the reversible logic circuit is reducing the number of gates, Garbage outputs and quantum cost. Therefore, we have tried to reduce these parameters to have the most optimal circuit. Compared to its counterpart, our proposed circuit can be reported as improved and well-designed.

Key words: Reversible logic gates · Reversible logic circuit · Comparator · Quantum computing · Nanometric

INTRODUCTION

Power dissipation is an important factor in VLSI design. Combinational logic circuit dissipates heat in an order of KTln 2 joules. For every bit information that is lost. Where K is the Boltzmann constant and T is the operating temperature [1]. Information is lost when the input vector cannot be uniquely recovered from its output vectors. Reversible logic circuit naturally takes care of heating since in a reversible logic every input vector can be uniquely recovered from its output vectors. Therefore, no information is lost. According to [2], zero energy dissipation would be possible only if the network consists of reversible gates. Thus, reversibility will become an essential property in future circuit design. Synthesis of reversible logic circuit differs from the combinational one in many ways [3]:

Firstly, in reversible circuit there should be no fan-out, that is, each output will be used only once.

Secondly for each input pattern there should be unique output pattern. Finally, the resulting circuit must be acyclic. Any reversible circuit design includes only the gates that are reversible. In reversible circuit the main ideal is minimizing the number of gates, quantum cost and the number of garbage outputs.

In reversible circuit, the outputs that are not used as primary outputs are called garbage's. In the input lines that are set to constant are termed as constant input. An efficient design should keep all of them to minimum.

MATERIALS AND METHODS

Reversible Logic Gates: It is an n-input n-output logic function in which there is a one-to-one correspondence between the input and the output. Because of this directive mapping the input vector can be uniquely determined from the output vector. This prevents the loss of information which is the root cause of power dissipation in irreversible logic circuits.

The reversible logic circuit must be constructed under three main constant,

- Fan-out is not permitted
- Loop or feedback is not permitted. Recently, researchers illustrated that feedback is allowed in reversible computing while designing the sequential circuits [4].
- Permutation of connection between gates is permitted

In the proposed design these three constraints along with other parameters are optimized effectively.

The simplest reversible gate is NOT gate and is 1*1 gates. The reversible 1*1, NOT gate with zero quantum cost is as shown in Fig. 1.

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Fig. 1: not gate

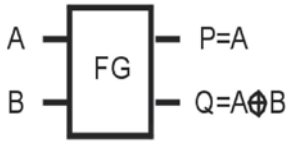

Fig.2: Feyman gate- 2*2 gate

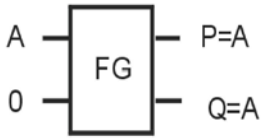

Fig.3: Feyman gate as a copying gate

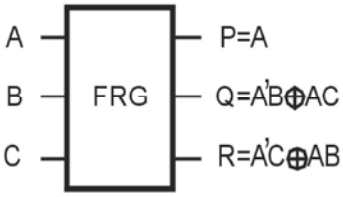

Fig.4: Fred kin gate -3*3 gates

The important basic reversible logic is,Feyman gate [5] which is the only 2*2 reversible gate with quantum cost one (QC=1) which is as shown in Fig. 2 and it is used most popularly by the designer for fan-out purpose (Fig. 3). There are also a Fredkin gate [6], Toffili gate [7], New gate [8] and Peres gate [9] all of which can be used to realize important combination function and all are 3*3 reversible gates as shown in fig. 4 to fig. 6. The figures also showed the switching function for terminals.

There are other 4*4 gates some of which are specially designed for the realization of important combinational circuit function in addition to some basic functions.

Some of the important 4*4 gates are MKG gate [10]. TSG gate [11], HNG gate [12] etc. HNG gate is very useful for the construction of reversible adders. They are also technology independent as quantum logic and optical logic are all still in the initial implementation stages and the technology is not defined properly. However, the design methods using existing reversible logic gates and new reversible logic gates are not only very important and useful for building future computation circuit but also for the design of ultra low power integrated circuits. They are classified circuits. They are classified as important theoretical computational circuits. A 4*4 HNG gate is depicted in fig.7.

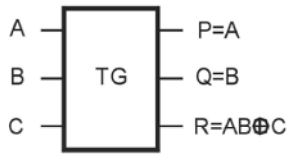

Fig. 5: Toffoli gate -3*3 gates

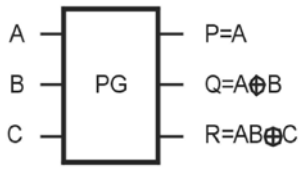

Fig. 6: Peres gate -3*3 gates.

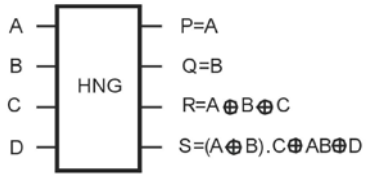

Fig. 7: Reversible HNG gate -4*4 gate

We use HNG gate in our proposed comparator as a full adder. For more information about reversible logic please see [13-16]

Optimization Parameters: The important parameters which play a major role in the design of an optimized reversible logic circuit are:

Constants Inputs: This refers to the number of inputs to be maintained constant at either 0 or 1 in order to synthesize the given logic function.

Garbage Outputs: This refers to the number of outputs which are not used in the synthesis of a given function. These are very essential.

Gate Count: The number of reversible gates used to realize the function.

Quantum Cost: This refers to the cost of the circuit in terms of primitive gate. It is calculated by knowing the number of primitive reversible logic gaiter (1*1or 2*2) required to realize the circuit.

Our Proposed Four Bit Reversible Numerical Comparator: The comparator is a synthetic circuit that compares two n-bit numbers and determines larger than, equal to, or less than the other. Two numbers comparing are signed or unsigned, there for have deferent synthetic circuit.

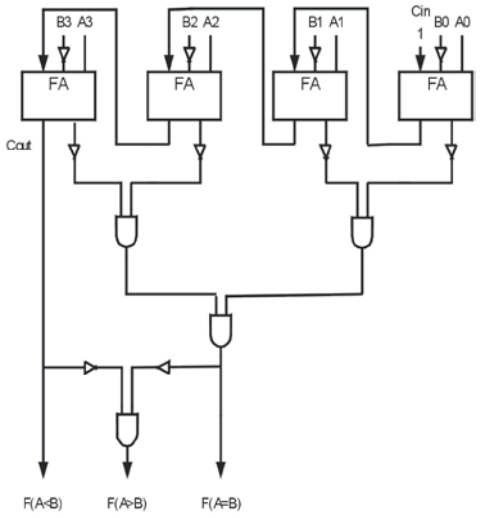

Fig. 8: Block diagram of conventional irreversible numerical comparator [17]

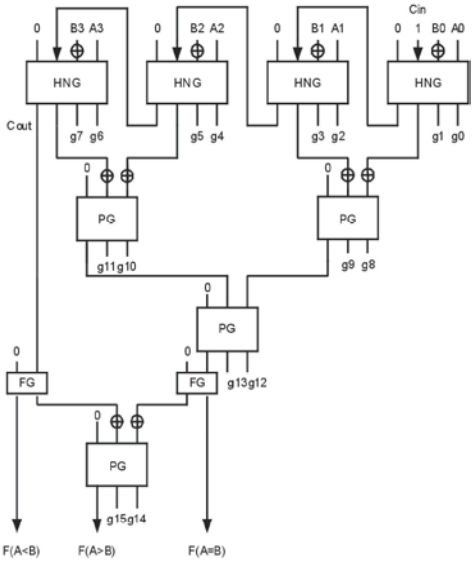

Fig. 9: Proposed reversible numerical comparator

According to the conventional numerical comparator, we propose our reversible numerical comparator. We have used the 4-bit adder in our comparator. We have transformed a-b to a+b'+l. if carry is produced then a>b, if carry isn't produced then a<b, and if the result to be zero tow number will be equal. The conventional of 4-bit irreversible numerical comparator which consist of 4 full adder and 4 NOR is shown in fig. 8. Our proposed 4-bit reversible numerical comparator mainly contains 4 HNG gate as full adder , and 4 three input PG and two FG for fan-out and some not gate. It can compare the value of two binary numbers A and B by using A-B. We have shown our proposal in fig. 9.

Table 1: Comparative analysis of different reversible comparator

	Number of gates	Number of garbage	Number of constant	Quantum coast (QC)
This work	10	15	11	42
Existing circuit [18]	25	23	17	Un known

RESULT AND DISCUSSION

Evaluation of the Proposed Numerical Reversible Comparator: the comparison of the proposed reversible comparator to the existing in terms of the number of gates, Garbage inputs/outputs and Quantum cost of the logics is shown in the table 1.

It is observed that this work has better performance compared to the existing circuit. In the implementation of [18] a total of 25 gates are used which produce 23 garbage outputs , with 17 constant inputs. In the present paper the design is such that these parameters are kept to the minimum value. The proposed circuit uses a total number of 10 reversible gates consisting of four HNG gates , four Peres gates for fan-out.

This is less than the number of gates implement in [18]. Our propos one circuit produces a total number of 15 garbage outputs with 11 constant inputs. This is less than the number of garbage outputs and constant inputs implemented in [18]. The quantum cost in this study is 42. This is less that of the existing circuit.

CONCLUSION

In this paper an optimized reversible numerical comparator is presented. The design is very useful for the future computing techniques like ultra low power digital circuits and quantum computers. It is shown that the proposed circuit is highly optimized in terms of number of reversible logic gates. Number of garbage and quantum cost. From table 1 it is observed that the presented circuit uses least number of gates, producing least number of garbage outputs and quantum cost. The design method is definitely useful for the construction of future computer and other computational structures in nanometric fashion.

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