Middle-East Journal of Scientific Research 24 (Techniques and Algorithms in Emerging Technologies): 532-537, 2016
ISSN 1990-9233;

DOI: 10.5829/idosi.mejsr.2016.24.TAET23635

Super Threshold FinFET Circuits Based on Pass Transistor Adiabatic Logic-2N Operating Region

V.M. Senthil Kumar[1], S. Saravanan[2], S. Priyanka[3] and P. Deepa[4]

[1]Associate Professor, Department of ECE,
Vivekanandha College of Engineering for Women, Tiruchengode, Tamil Nadu, India
[2]Professor and Head, Department of ECE Muthyammal Engineering College,
Rasipuram, Tamil Nadu, India
[3]PG student, Department of ECE Vivekanandha College of Engineering for Women,
Tiruchengode, Tamil Nadu, India
[4]PG student, Department of ECE Vivekanandha College of Engineering for Women,
Tiruchengode, Tamil Nadu, India

Abstract: Scaling of device technology the leakage power has become the main part of power consumption and seriously reduces the energy recovery efficiency of adiabatic logic. The adiabatic flip-flops that operate on medium-voltage region can not only keep reasonable speed but also reduce greatly energy consumptions. The main motivation of the work is adiabatic Fin-FET circuit reduces the power by working in lower voltages levels for supply in the voltage range 0.5 to 0.9 V. In recent times the consumer products are designed to operate in lesser power. To reduce energy consumption, voltage scaling techniques have proved a popular technique with sub threshold design representing the endpoint of voltage scaling. since FinFET devices can provide better drive strength than bulk CMOS ones. The leakage current is less than in Fin-FET compared to CMOS below 45nm technology. All circuits are simulated with LTSPICE at a PTM (Predictive Technology Model) 32nm Fin-FET technology.

Key words: FinFET · Adiabatic logic · Power reduction · Energy consumption

INTRODUCTION

In modern CMOS ICs, technology scaling increases the density and performance of a single chip, resulting in large energy consumptions [1, 2]. IC designers have been working on high operating speed with low energy dissipations. The total energy consumptions in a CMOS circuit mostly include two parts: static energy dissipation caused by leakage currents of MOS devices, dynamic energy dissipations caused by charging and discharging nodes of circuits [3, 4]. This seriously reduces the energy recovery efficiency of adiabatic logic. Unlike traditional CMOS circuits, which dissipate energy during switching, adiabatic circuits reduce dissipation by following two key rules: Never turn on a transistor when there is a voltage potential between the source and drain. Never turn off a transistor when current is flowing through it. FinFET has a three-dimensional structure. It consists of a thin silicon body, which is formed perpendicularly to the plane of the wafer. The current flows parallelly to the wafer plane. The word adiabatic comes from a Greek word that describes thermodynamic processes which exchange no energy with the environment and therefore, no Energy loss in the form of dissipated heat.

This is because that the delay of CMOS circuits increases exponentially as the supply voltage scales down. Therefore, sub-threshold computing for CMOS circuits only fits some ultra-low-speed applications. The supply voltage of near-threshold CMOS circuits is slightly above the threshold voltage of the MOS transistors [5]. The near-threshold CMOS circuits can retain much of the energy savings of sub-threshold circuits Compared with sub-threshold circuits, the near

Corresponding Author: V.M. Senthil Kumar, Associate professor, Department of ECE, Vivekanandha College of Engineering for Women, Tiruchengode, Tamil Nadu, India.

threshold CMOS circuits can obtain good performance due to large turn-on currents. However, the near-threshold CMOS circuits are only suitable for mid-speed applications, since their MOS devices operate on medium weak inversion.

Adiabatic logic is a good selection in the circuit level. We extract charge from the supply at the lowest feasible voltage and return it at the highest feasible voltage. Adiabatic logic utilizes AC power-clock to recover effectively the charge delivered by the clock instead of being dissipated to the ground [6]. Adiabatic computation has been widely accepted as a low-power design techniques. IC power dissipation consists of different components depending on the circuit operating mode [1].

Because of the reversibility requirements for a system to be fully adiabatic, most of these synonyms actually refer to and can be used inter-changeably, to describe the quasi-adiabatic systems. Since tunnelling probability of an electron through a potential barrier does not depend directly on temperature, the gate and the junction is expected to be less sensitive to temperature variations.

Cmos Adiabatic Logic

CMOS PAL-2N Inverter: The typical time sequence of the PAL-2N inverter logic is divided into four-phase operations. They are

- Wait: The power supply stays zero, the inputs become valid and the evaluation logic generates pre-evaluated result and the outputs keep low voltage.
- Evaluate: The power supply rises from zero to VDD gradually and inputs remain stable. According to the result of pre-evaluation, output follows the power supply to become valid.
- Hold: The power supply stays high to keep the output valid, providing the constant input signal for the next stage in the adiabatic pipeline. The inputs return to zero.
- Recover: The power supply climbs down to zero. The remaining zero voltage inputs shut down the current access to the ground; thus the charge stored in the node capacitance can flow back to the power supply through the cross-coupled P-MOSFETs.

In the Fig. 1 CMOS PAL-2N logic, the load driven circuit consists of a pair of p-type MOS transistor for recovering energy into power clock.

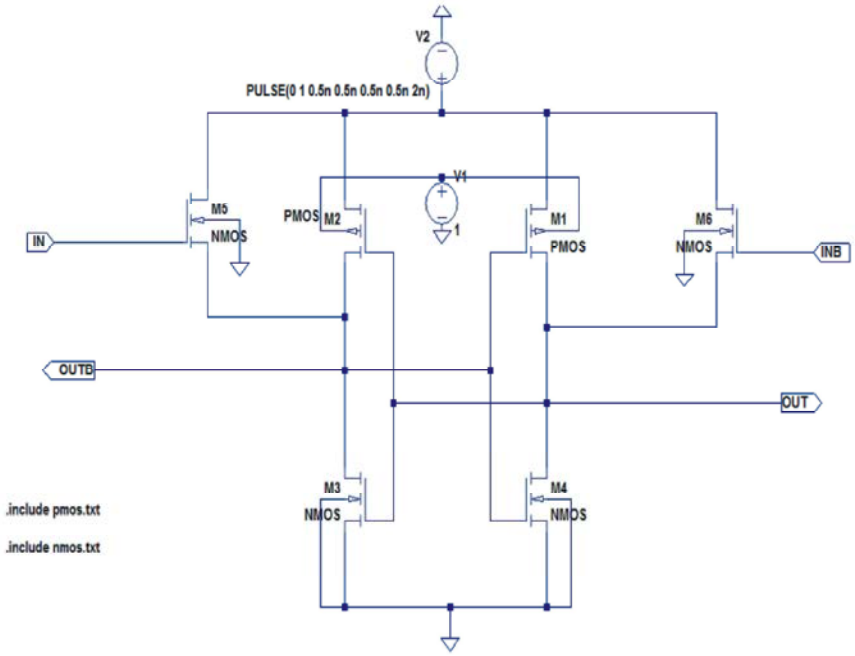

Fig. 1: CMOS PAL-2N inverter

CMOS PAL-2N Flip-Flop: The below Fig. 2 is a 4 stage CMOS PAL-2N inverter based flip-flop. The output of each stage is fed as input to the next stage. While the charge storage on the capacitor is subjected to an charge leakage that exist in CMOS Circuits.

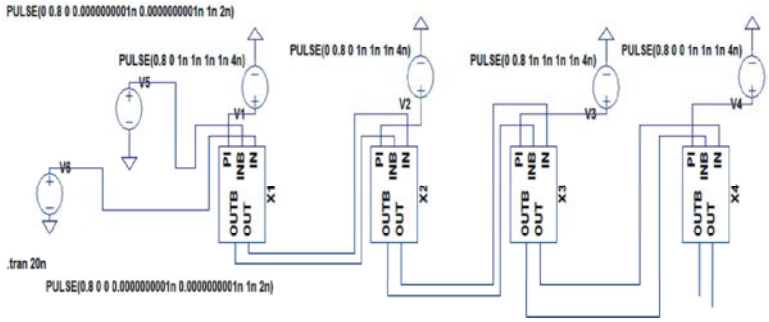

Fig. 2: CMOS PAL-2N flip-flop

The circuit can be modified to an static clocked design inverter in between the stage and using feedback control circuits. Flip-flops are essential element of digital sequential circuits [2].

FinFETS Adiabatic Logic

FinFET PAL-2N Inverter: The circuit of one stage FinFET PAL- 2N Inverter circuit is given below Fig. 3. It is composed of three main parts: the evaluation circuit consists of DPGMOS transistors trees implementing logic function. The load driven circuit consists of a pair of DGPMOS transistors for recovering energy into power clock [7]. The two NMOS transistor circuits can be ignored into particular PMOS circuits of recovering energy performances into power dissipation.

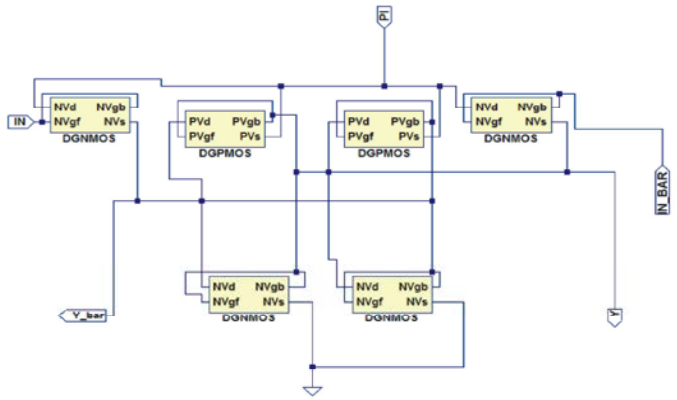

Fig. 3: FINFET PAL-2N inverter

FinFET PAL-2N Flip-flop: Flip-flops are critical components in digital circuits and thus the power consumed by flip-flops has a very important role for the total power of sequential logic circuit [3, 8]. In Fig. 4 there are three important timing parameters associated with flip-flop: setup time, hold time and propagation delay. The output of each stage is fed as input to the next stage. The input pulse can be given into the feedback control circuits while using the logic function of driven circuits in transmission gate.

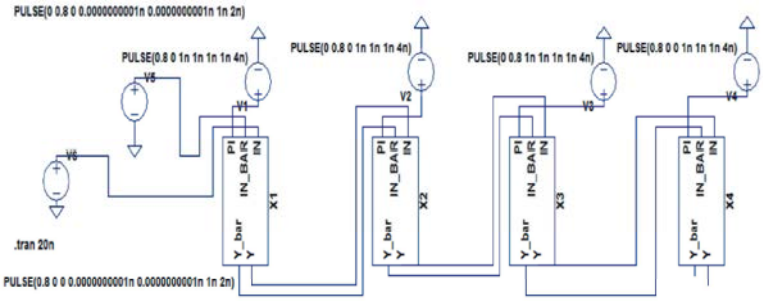

Fig. 4: FINFET PAL-2N flip-flop

The internal nodes can be eliminated other flip-flop designs exist and they are important components in digital design flip-flop.

PAL- 2N based Flip-Flop Operating in Medium Strong Inversion Region: FinFET logic circuits operating on medium inversion regions and strong inversion regions can obtain more favorable performance than conventional bulk CMOS. In this fig.5 super-threshold FinFET logic circuits operating on medium strong inversion regions can obtain faster speed than near-threshold ones operating on medium inversion regions. The FinFET device has larger sub-threshold slope than conventional MOS transistors due to strong gate control over the channel. Compared with bulk MOS transistors, the leakage of the FinFET ones is reduced significantly.

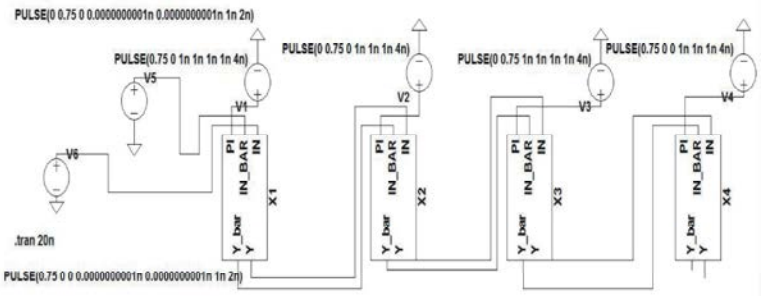

Fig. 5: PAL-2N based flip-flop operating in medium strong inversion region

RESULT AND DISSCUSION

The performances of the PAN-2N circuits based on FinFET in sub-threshold, near-threshold and super-threshold regions, the output waveform fig.6 PAL-2N FinFET flip flop are simulated with different peak-to-peak voltages of the power clocks ranging from 0.2V to 1.0V with 0.1V step using the 32nm FinFET PTM technology. The energy consumption saving of the FinFET Counter based on PAL-2N operating frequency respectively. The power consumption can be reduced at voltage time.

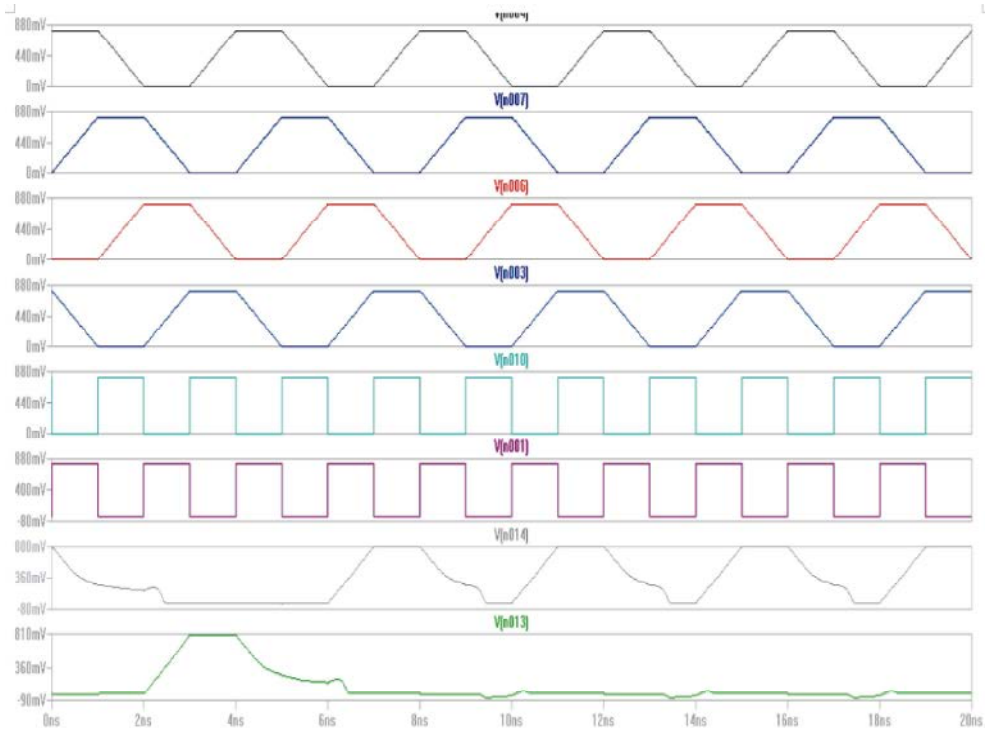

Fig. 6: Output waveform of CMOSPAL-2N flip-flop

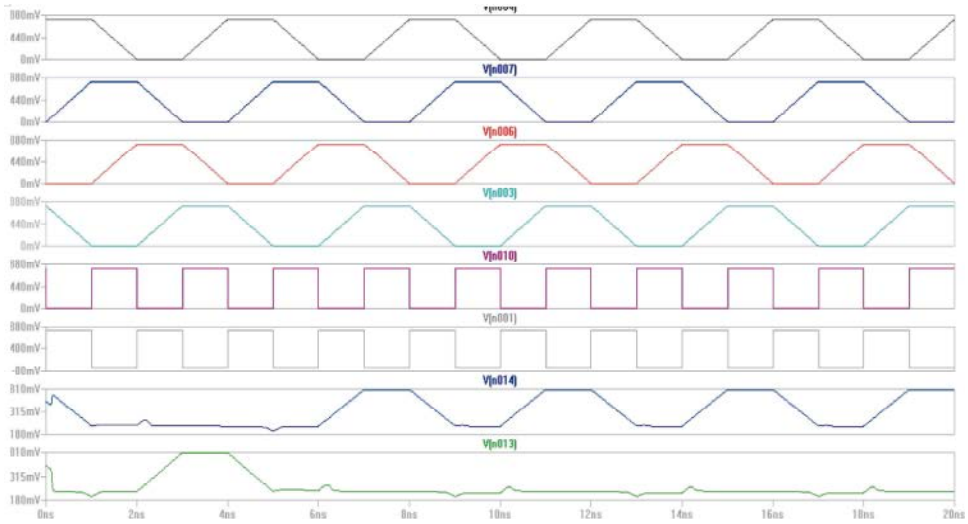

Fig. 7: Output waveform of FINFET PAL-2N flip-flop

However, the near-threshold CMOS circuits are only suitable for mid-speed applications [9, 10], since their MOS devices operate on medium weak inversion. The super-threshold adiabatic FinFET circuits based on PAL-2N operating on medium strong inversion regions are addressed in terms of energy consumption and operating frequency.

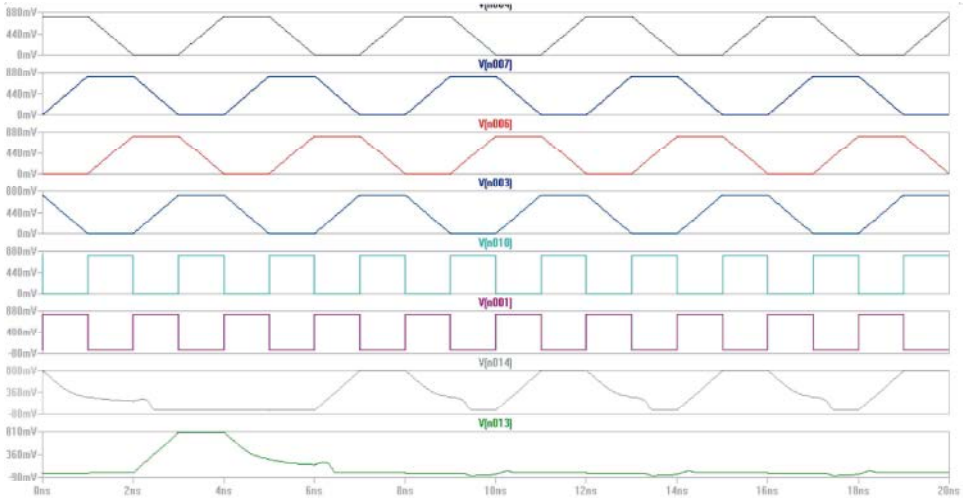

Fig. 8: Output waveform of PAL-2N based flip-flop operating in medium strong inversion region

Table I: Comparison of Cmos and Finfet Based on Pal-2n Flip-flop

	PAL-2N Flip-Flop				
Device	Stage1	Stage2	Stage3	Stage4	Total power
CMOS	9.63084 μW	2.1112 μW	34.7032 μW	10.4414 μW	56.8864 μW
FinFET	550.968 μW	975.252 μW	1.78329 μW	75.6631 μW	3.351731 μW

Total power in CMOS circuits can achieve maximum to minimum peak voltages and the FinFET PAL-2N Flip-Flop devices can ignore the lowering standard supply voltages.

CONCLUSIONS

The work is done on adiabatic finFET circuit which operates in lower operating supply voltage. The work will reduce the power which suits well for consumer products. The effectiveness of FinFET towards lower leakage current below 45nmTechnology is utilized and the results prove the same. The super-threshold adiabatic FinFET inverter and flip-flop circuits based on PAL-2N operating on medium strong inversion regions is designed and simulated. The CMOS based inverter and Flip Flop is also

designed and simulated and the performance is observed to compare with the different method. The power consumption of the devices is compared and found that the FinFET based devices consume less power.

REFERENCES

1. Fallah, F. and M. Pedram, 2005. Standby and active leakage current control and minimization in CMOS VLSI circuits, IEICE Transactions on Electronics, vol. E88-C, 4: 509-519, April 2005.
2. Borkar, S. and A.A. Chien, 2011. The future of microprocessors", Communications of the ACM, 54(5): 67-77.
3. Hisamoto, D., W.C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kua, E. Anderson, T.J. King, J. Bokor and C. Hu, 2000. FinFET – A self-aligned double gate MOSFET scalable to 20nm, IEEE Transaxtions on Electron Devices, 47(12): 2320-2325.
4. Wu, AY. and J. Hu, 2011. Near-threshold computing of clocked adiabatic logic with complementary pass-transistor logic circuits, Journal of Low Power Electronics, 7(3): 393-402.
5. Hu, J. and X. Yu, 2010. Near-threshold adiabatic flip-flops based on PAL-2N circuits in nanometer CMOS processes, In: Proceedings of Pacific-Asia Conference on Circuits, Communications and System, 1: 446-449.
6. Liu, F. and K.T. Lau, 1988. Pass-transistor adiabatic logic with NMOS pull-down con Fig..uration, Electronics Letters, 34(8): 739-741.
7. Hwang, Y.T., J.F. Lin and M.H. Sheu, 2012. IEEE Trans. On Very Large Scale Integration (VLSI) Systems, 20(2): 361-366.
8. Xiayu, L., J. Song, L. Limin and W. Yuan, 2012. IEICE Trans. On Electronics, vol. E9SC, 6: 1 12S-1 127.
9. Yejoong, K., J. Wanyeong, L. Inhee, O. Qing, *et al*., 2014. Proceedings of IEEE ISSCC 2014, San Francisco, Feb. 9-13, pp: 86-87.
10. Kawai, N., S. Takayama, J. Masumi, N. Kikuchi, *et al*., 2013. Proceedings ofIEEEA-SSCC 2013, Singapore, Nov. 11-13, pp: 117-120.