Middle-East Journal of Scientific Research 24 (Techniques and Algorithms in Emerging Technologies): 515-523, 2016
ISSN 1990-9233;

DOI: 10.5829/idosi.mejsr.2016.24.TAET23633

Design and Implementation of Low Power Finfets Using Adiabatic Logic

[1]V.M. Senthil Kumar, [2]S. Saravanan, [3]P. Deepa and [4]S. Priyanka

[1]Associate Professor, Department of ECE,
Vivekanandha College of Engineering for Women, Tiruchengode, Tamil Nadu, India
[2]Professor and Head, Department of ECE Muthyammal Engineering College,
Rasipuram, Tamil Nadu, India
[3]PG student, Department of ECE Vivekanandha college of Engineering for Women,
Tiruchengode, Tamil Nadu, India
[4]PG student, Department of ECE Vivekanandha College of Engineering for Women,
Tiruchengode, Tamil Nadu, India

Abstract: Scaling of device technology, CMOS (Complementary metal oxide semiconductor field effect transistor) circuits has lead to a stunning enhancement of leakage currents. The leakage current has become the main part of power consumption. So the continuous scaling with power reduction in future technology will cause leakage current in becoming an increasingly outsized component of total power dissipation. The continuous increasing power has become the primary barrier against further development of VLSI (Very large scale integration) circuit design. Therefore always it requires new techniques for providing low power circuit operation with high performance. Adiabatic logic style is an attractive solution for low power digital design. In this paper, a novel low-power adiabatic logic based on FinFETs (Fin-type Field-Effect Transistors) devices has been proposed. Due to the lower leakage current, higher on-state current and design flexibility of FinFETs. FinFETs have been proposed as a promising alternative for future technologies because of their better gate control of the channel with that of conventional bulk MOSFET (metal oxide semiconductor field effect transistor). The proposed adiabatic logic shows considerable power reduction, performance improvement and area saving compared with CMOS adiabatic. In this paper, we use 32nm predictive Technology model.

Key words: Adiabatic logic · FinFET · Leakage current · Power consumption · VLSI

INTRODUCTION

Power dissipation becomes a major part of concern in VLSI design as the feature size decreases and the corresponding chip density increases. In conventional static CMOS, the energy dissipation is caused primarily by the dissipative charge and discharge of the node capacitances in the circuit. Power consumption is composed of two parts: dynamic power and static power [1]. The dynamic power is due to the switching activities during charging and discharging process, while static power is caused by the inherent device leakage when the circuit is in the off state. Which seriously reduces the energy recovery efficiency of adiabatic logic [2]. The adiabatic charge recovery circuits achieve low energy consumption by restricting the currents to flow across devices using ramp like clock signals and by recycling the energy stored in their node capacitors using an ac power supply rather than dc. Adiabatic Circuits are low power circuitry which use "reversible logic" to conserve energy. The word adiabatic comes from a Greek word that describes thermodynamic processes which exchange no energy with the environment and therefore, no Energy loss in the form of dissipated heat [3].

Adiabatic logic is a low power digital circuit design technique. In static CMOS logic during the switching process the output node capacitances are charged and discharged from 0V to VDD by a step

Corresponding Author: V.M. Senthil Kumar, Associate professor, Department of ECE,
Vivekanandha College of Engineering for Women, Tiruchengode, Tamil Nadu, India.

voltage of very short rise and fall time. During the switching process energy dissipated in switching transistor is given by ½CLVDD2, where CL is load capacitance and VDD is constant voltage supply. We can say ½CLVDD2 is the lower limit for switching power dissipation in CMOS logic, but adiabatic logic can lower this limit further.

Adiabatic circuits employ AC power source (clock) rather than the DC supply and therefore can recover the energy stored in capacitance back to the power source and completely avoid the dynamic power dissipation theoretically. There are a number of synonyms that have been used by other authors to refer to adiabatic logic type systems, these include: Charge recovery logic, Charge recycling logic?, Clock-powered logic, Energy recovery logic and Energy recycling logic. Because of the reversibility requirements for a system to be fully adiabatic, most of these synonyms actually refer to and can be used inter-changeably, to describe quasi-adiabatic systems.

Types of Adiabatic Logic: Adiabatic logics are of two main types. They are:

- Partially adiabatic logic.
- Fully adiabatic logic.

Now, partially adiabatic logic is a logic having non-adiabatic loss present i.e. there is non -zero VDS across transistor when it is being turned ON. It doesn't depend upon frequency. It can be further classified as:

- Efficient charge recovery logic (ECRL).
- 2N-2N 2P logic.
- Positive feedback adiabatic logic (PFAL).
- NMOS energy recovery logic (NERL).
- Clocked adiabatic logic (CAL).

Fully adiabatic logic is a logic having non -adiabatic loss absent. It depends upon frequency. It can be classified as:

- Improved Pass transistor adiabatic logic(IPAL).
- Split rail charge recovery logic (SCRL).

Finfet Device: FinFET has a three-dimensional structure. It consists of a thin silicon body, which is formed perpendicularly to the plane of the wafer. The current flows parallelly to the wafer plane. The channel is wrapped by the gate electrodes in three directions. Fig. 1 (a) and (b) illustrate the three-dimension structure and cross-section diagram of a FinFET device. (c) three working modes for FinFET

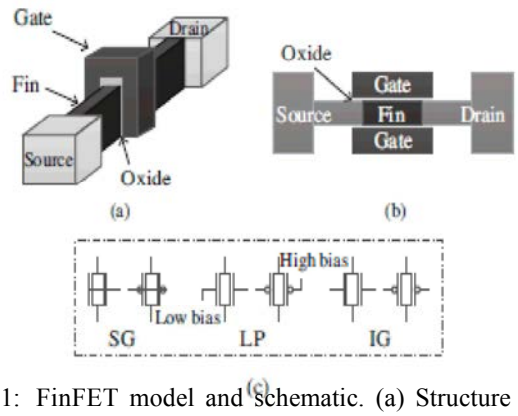

Fig. 1: FinFET model and schematic. (a) Structure (b) cross-section diagram(c) three working modes for FinFET.

With the continuing scaling of CMOS processes, leakage energy dissipations are becoming the main source of energy consumptions. In order to cope with this problem, several novel devices have been developed. FinFET devices show excellent performance with low-power characteristic in the novel devices. The recently reported researches have shown that FinFET is a promising alternative for the CMOS processes to realize continued scaling. FinFET has a three dimensional structure. It consists of a thin silicon body, which is formed perpendicularly to the plane of the wafer. The current flows parallelly to the wafer plane. The channel is wrapped by the gate electrodes in three directions.

FinFET can provide stronger control over the channel and suppress the SCEs [13], threshold current and gate-dielectric leakage current more effectively than MOSFET, resulting in higher on-state current, lower leakage and faster switching speed. FinFET is operated at three modes, namely Short-Gate mode(SG), Independent-Gate mode(IG)[12] and Low-Power mode(LP)[4].In shorted gate mode of operation the back gate is tied to the front gate to improve the drive strength and control of the channel. However in the independent gate mode back gate have a different voltages from front gate. in this mode has more flexibility in circuit design. in low power mode the threshold of front gate is altered with the bias on back gate thereby providing a method to reduce the leakage current.

Existing Method: In adiabatic logic, the node voltage changes synchronously with the supply voltage (sine wave); thus the energy released from the power supply is just 0.5 CV^2_{DD}, which could be stored in the load capacitance. Moreover, when the supply voltage falls

down to the ground level, the energy stored in the capacitance could flow back to the power supply[5]. The time sequence of the adiabatic logic is divided into four-phase operations. They are

Charge Sharing: The discharge signal increases at a rate twice that of the input signal. In this phase, the power-clock voltage (Vpc) is stable at a low level and the evaluation path signal which is established by cells, increases simultaneously and slowly. The total internal node capacitances are discharged to ground before the logic function is evaluated to prevent the circuit from depending on previous input data.

Evaluation: In the Evaluation phase, the Discharge signal is already stable at a low level, which turns on transistor so that the supply current can flow into the logic circuit. The output wires are evaluated through one of the active input cells and the Cx transistors already at a high level.

Hold: During the hold phase, the current active input and Evaluation signals slowly decrease to a low level; however, the outputs signals remain stable because these are controlled by the cross-coupled NMOSs.

Recovery: The power clock voltage (Vpc) steadily decreases to a low level and the current active output discharges to a low level via the active PMOS transistor because the Discharge signal is still low. Charge recovery occurs for every power-clock cycle to minimize the energy lost during charging or discharging.

Cmos 2N2N2P Inverter: The simplest adiabatic buffer with 2N2P structure, which contains two cross-coupled P-MOSFETs and two difierential input N-MOSFETs [6, 7]. In Fig.2 the 2N2N2P logic, the two more N-MOSFETs with P-MOSFETs make up two inverters to cross-couple, which increases the stability of the outputs.

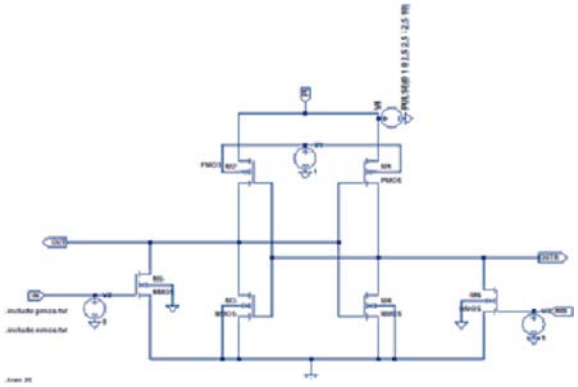

Fig. 2: CMOS 2n2n2p inverter

Cmos Ipal Inverter: The most widely used adiabatic logics include 2N2N2P, IPAL, PFAL,DCPAL. Above four types adiabatic buffers are shown in Fig. 2. They have similar operations with 2N2P logic but also have some differences. In the 2N2N2P logic, the two more N-MOSFETs with P-MOSFETs make up two inverters to cross-couple, which increases the stability of the outputs [8, 9]. In Fig.3 shows IPAL logic folds the evaluation logic upward to pull up blocks to form two charging paths with a pair of cross coupled P-MOSFET.

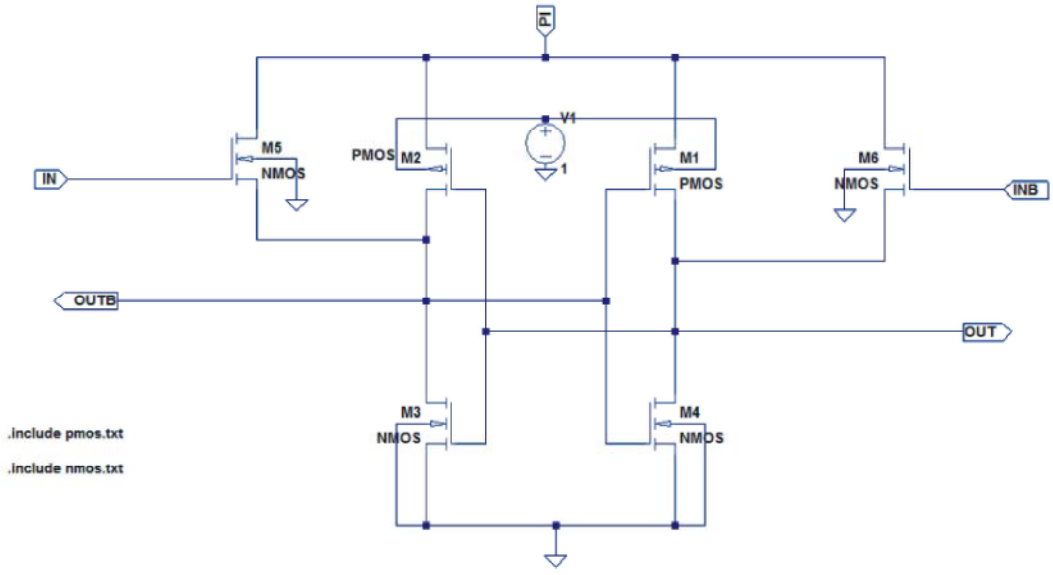

Fig. 3: CMOS IPAL inverter

Cmos Dcpal Inverter: DCPAL is a hold logic, which reduces the time taken of hold state and also reduces leakage current. DCPAL inverter eliminates the charge stored in the output node after the recovery phase, which can provide complete charge recovery is shown in Fig. 4.

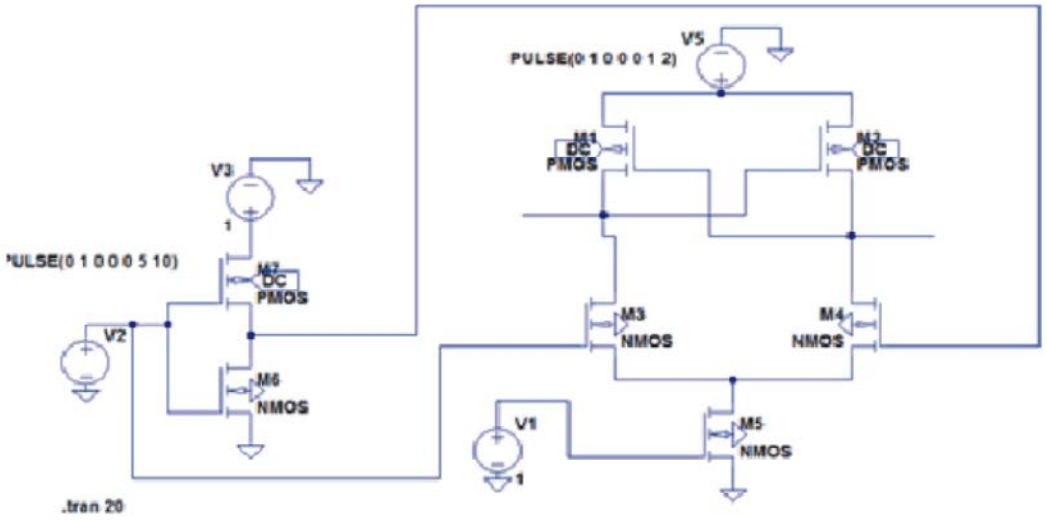

Fig. 4: CMOS DCPAL inverter

Cmos Pfal Inverter: Based on the IPAL logic, In Fig. 5. The PFAL logic adds a pair of feedback N-MOSFETs and the feedback signal comes from the next stage's outputs.

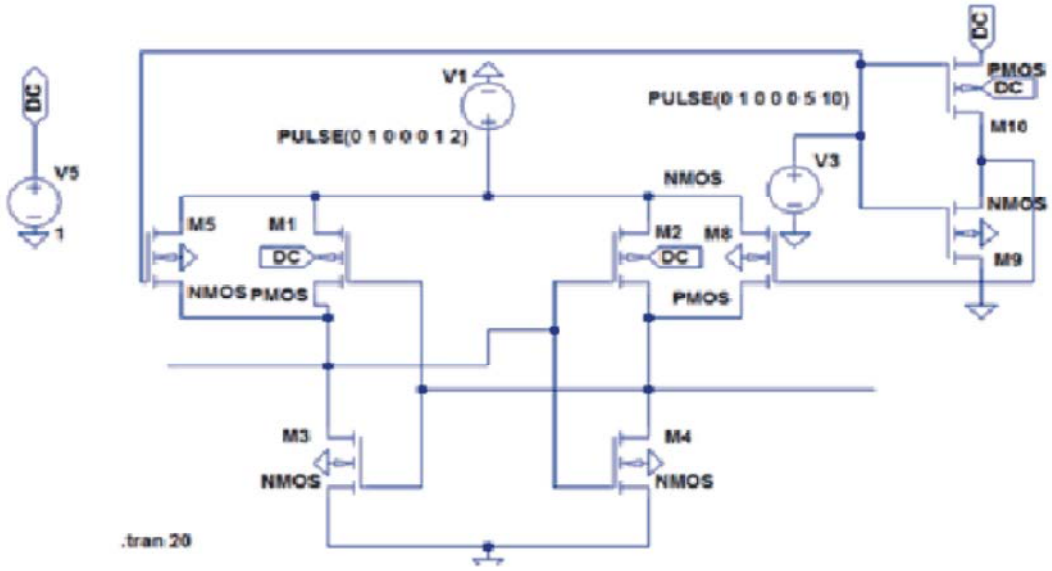

Fig. 5: CMOS PFAL inverter

Proposed Method

Finfet 2n2n2p Inverter: Compared to MOSFETs, FinFETs demonstrate low-power characteristic, excellent performance and flexible working modes. Based on these advantages, our research successfully proposed some novel adiabatic logics based on FinFETs to further improve the power consumption and performance.

In Fig. 6 shows that 2n2np inverters two PMOS transistors are cross coupled with the NMOS transistor, which increases stability of outputs. it have similar operation of 2n2p adiabatic logic.

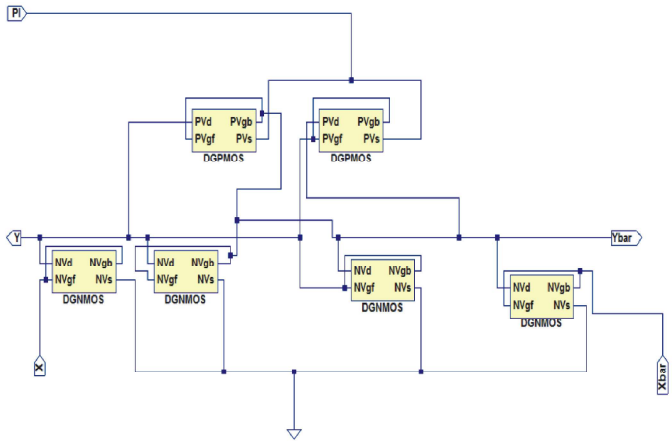

Fig. 6: FINFET 2n2n2p inverter

Finfet Ipal Inverter: The IPAL gate is based on the 2N-2P gate. It requires differential control in the charge phase of the clock and thus obtaining a differential output voltage is shown in Fig. 7.

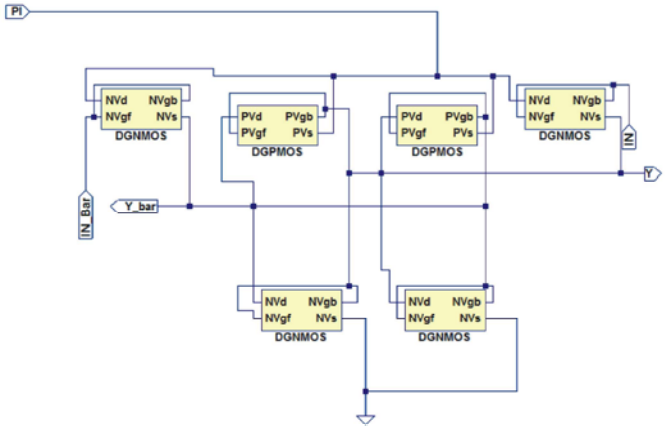

Fig. 7: FINFET IPAL inverter

Finfet Dcpal Inverter: DCPAL is a hold logic, which reduces the time taken of hold state and also reduces leakage current is shown in Fig. 8.

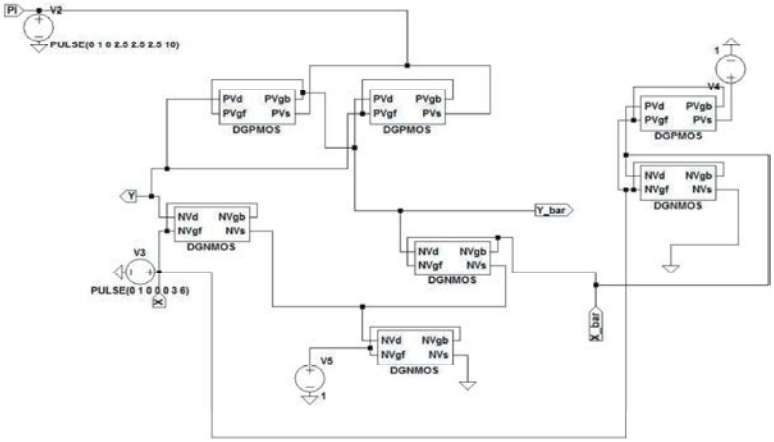

Fig. 8: FINFET DCPAL inverter

Finfet Pfal Inverter: Based on the IPAL logic, In the Fig.9 PFAL logic adds a pair of feedback N-MOSFETs and the feedback signal comes from the next stage's outputs [10]. This structure effectively eliminates the charge stored in the output node after the recovery phase, which can provide current.

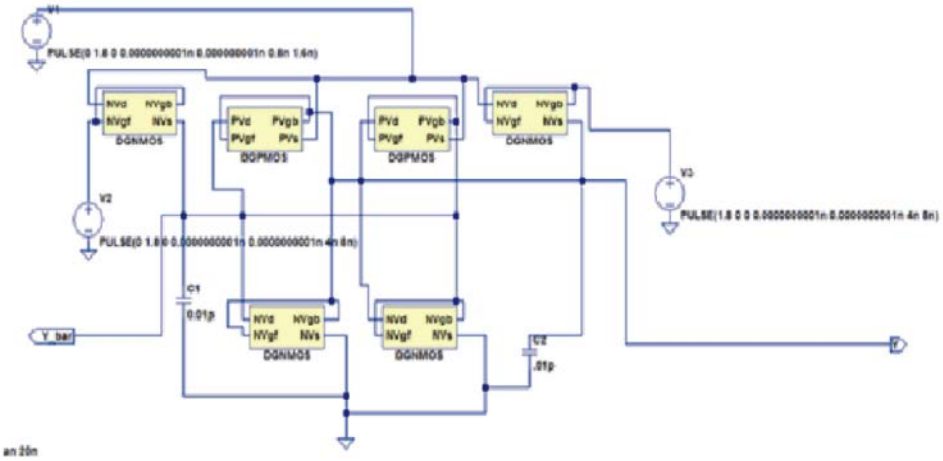

Fig. 9: FINFET PFAL inverter

RESULTS AND DISCUSSION

The SG mode FinFET circuit has lower off-state current and higher switching speed than MOSFET; thus it can effectively reduce the leakage current in every phase especially in the hold phase and it greatly raises the limiting frequency.

Finfet 2n2n2p Inverter:

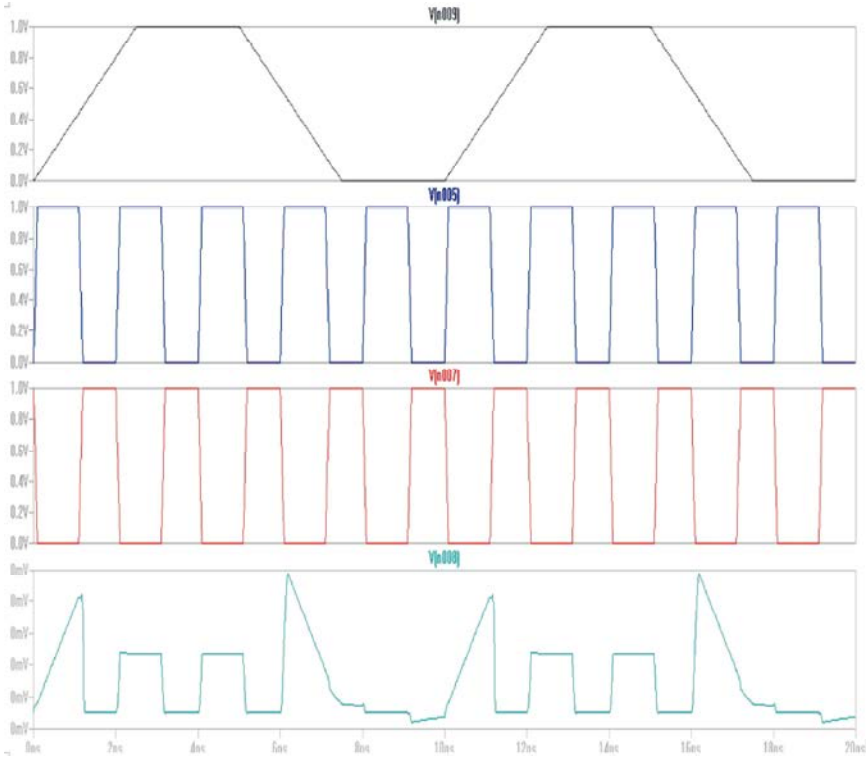

Fig. 10: FINFET 2n2n2p inverter

For the operation of adiabatic logic, the charging and discharging processes merely depend on the pull-up transistors, while the pull-down transistors primarily serve to accelerate the cross-coupling and maintain the certain nodes at zero voltage is shown in Fig. 10 and 11. Therefore the working speed of adiabatic circuits is determined by the pull-up transistors, independently of the pull-down parts.

Finfet Ipal Inverter:

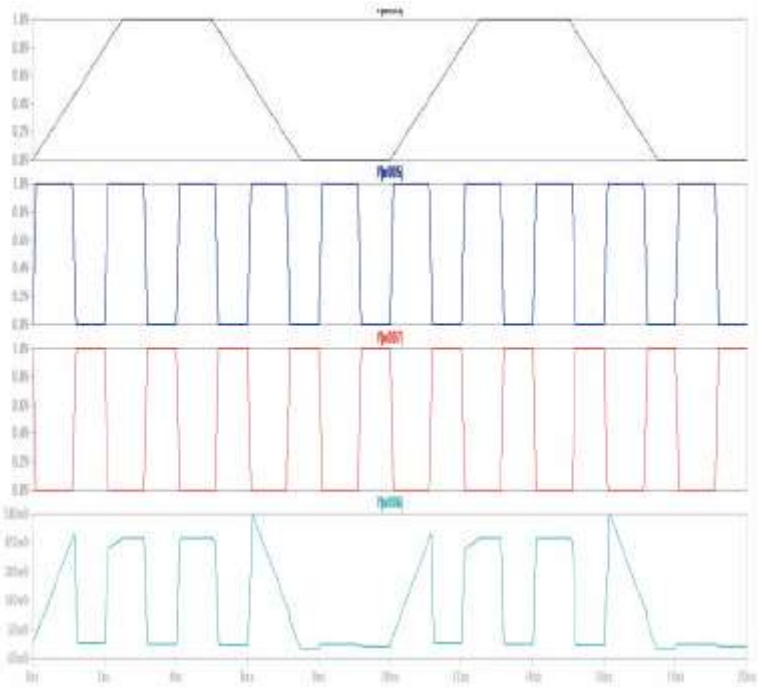

Fig. 11: FINFET IPAL inverter

Finfet Dcpal Inverter: The DCPAL [9, 10] operation consists of 4 states is shown in Fig 12.

- The pre-resolving phase, when the inputs are preresolved
- The Evaluate phase, when PC raises and evaluates Using the pre-resolved circuit states
- Hold phase
- Recovery phase

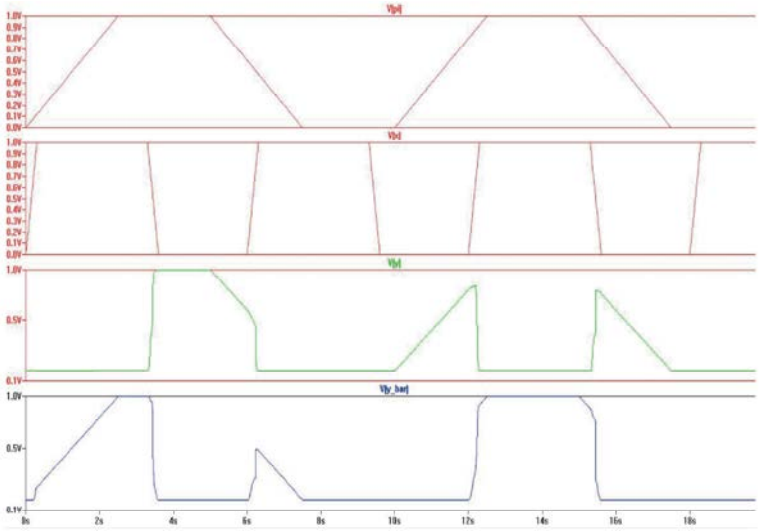

Fig. 12: FINFET DCPAL inverter

Finfet Pfal Inverter: PFAL logic adds a pair of feedback N-MOSFETs and the feedback signal comes from the next stage's outputs. For PFAL, considerable power savings are also realized by the FinFETs is shown in Fig. 13.

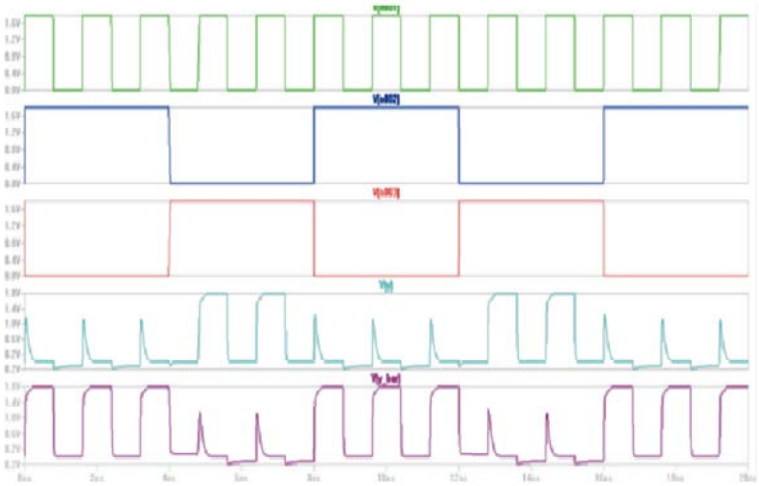

Fig. 13: FINFET PFAL inverter

CONCLUSION

In this paper presents the novel adiabatic logic based on FinFETs. Four types of adiabatic logic, namely 2N2N2P, IPAL, DCPAL, PFAL are rebuilt by SG mode FinFET. Compared with the CMOS adiabatic logic, the proposed logic effectively reduces the power consumption and improves the performance. Implementing of FinFET further improves the limiting frequency of adiabatic circuit. Therefore, the low-power and high-performance FinFET adiabatic logic will be a competing structure in the future IC design.

REFERENCES

1. Yang, B. and L. Kim, 2005. A low-power SRAM using hierarchical bit line and local sense amplifiers, IEEE J. Solid-State Circuits, 40(6): 1366-1376.
2. Moon, Y. and D.K. Jeong, 1996. An efficient charge recovery logic circuit. IEEE J. Solid-State Circuits, 31: 514-522.
3. Chanda, M., A. Dandapat and H. Rahaman, 2009. Low-power sequential circuit using single phase adiabatic dynamic logic. In:2009 International Conference on Computers and Devices for Communication, Kolkata, pp: 1-4.
4. Jafari, F., M. Mosaffa and S. Mohammadi, 2011. Designing robust asynchronous circuits based on FinFET technology. In: 2011 14th Euromicro Conference on Digital System Design, Oulu, pp: 401-408.
5. Bai, X.F., L. Huang, Y.F. Wang, *et al*., 2010. Evaluation of DPA attack resistance of transistor-based adiabatic logic styles. In: 2nd International Conference on e-Business and Information System Security, Wuhan, pp; 1-3.
6. Kramer, J.S., B. Denker and J. Flower, 1995. Moroney: 2nd Order Adiabatic Computation with 2N-2P and 2N-2N2P logic circuits", Int. Symposium on Low Power Design, pp: 191-196.
7. Moon, Y. and D. Jeong, 1996. An Efficient Charge Recovery Logic Circuit, IEEE Journ. Solid-state Circuits, 31(4): 514-522.
8. Varga, L., F. Kovacs and G. Hosszu, 2001. An improved pass-gate adiabatic logic. In: 14th Annual IEEE International ASIC/SOC Conference, Arlington, pp: 208-211.
9. Vetuli S.D. Pascoli and L.M. Reyneri, 1996. Positive feedback in adiabatic logic, Electronics Letters, 32(20): 1867-1869.
10. Kanchana Bhaaskaran, S. and J.P. Raina, 2008. Differential Cascode Adiabatic Logic Structure for Low Power, Jl. of Low Power Electronics, 4(2): 178-191.
11. Zhao, W. andY. Cao, 2007. Predictive technology model for nano-CMOS design exploration. ACM J. Emerg Technol Comput Syst, 3: 1.
12. Hsieh, C.Y., M.L. Fan, V.P.H. Hu, *et al*., 2012. Independently-controlled-gate FinFET Schmitt trigger sub-threshold SRAMs. IEEE Trans Very Large Scale Integr Syst, 20: 1201-1210.

13. Trivedi, V.P., J.G. Fossum and W.M. Zhang, 2007. Threshold voltage and bulk inversion effects in nonclassical CMOS devices with undoped ultra-thin bodies. Solid-State Electron, 1: 170-178.
14. Hisamoto, D., W.C. Lee, J. Kedzierski, *et al*., 2000. FinFETA self-aligned double gate MOSFET scalable to 20 nm. IEEE Trans Electron Dev, 47: 2320-2325.
15. Samson, M. and S. Mandavalli, 2011. Adiabatic 5T SRAM. In: 2011 International Symposium on Electronic System Design, Kochi, pp: 267-272.