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Low Power High Speed Performance of Multiplexer Using Reversible Logic

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Abstract: Reversible logic could be a common idea in economical energy computations and this may be the demand for forthcoming future computing technologies. Reversible logic is rising as a crucial analysis space and it'll be having wide applications in several fields like optical informatics, quantum computing and Low power CMOS style. The most purpose of planning reversible logic is to decrease the quantum value, depth of the circuits and a number of garbage outputs. Reversible square measure circuits (gates) that have one to 1 mapping between vectors of inputs and outputs; so the vector of input states are often continually reconstructed from the vector of output states. Reversible logic is enjoying a big role in quantum computing as quantum operations square measure unitary in nature. Quantum laptop performs computation at associate atomic level; thereby doing high-performance computations on the far side the boundaries of the standard computing systems. Reversible arithmetic units like adders, subtractors, multipliers kind the essential element of a quantum system. Among the adder styles, carry look-ahead is wide employed in high- performance computing owing to its O (log n) depth. During this work, we tend to gift improved styles of each in-place and out-of-place reversible carry look-ahead adder planned. The planned styles utilize the properties of the Reversible Peres gate square measure optimize the logic depth, quantum value gate count compared to the prevailing styles planned to each the improved styles assume no input carry (C0=0). Whereas the primary approach makes use of ancilla bits to store the add outputs, the second approach stores the add outputs in one in every of the input locations.

Key words: Reversible logic gates · Reduced garbage output · Quantum cost · Low power design · Carry look-ahead adder · Fredkin gate · Ancilla bits

INTRODUCTION

The demand for implementing ultra-low power digital systems in many fashionable applications, like mobile systems, sensing element networks and planted medicine systems, has augmented the importance of planning logic circuits [1] in subthreshold regime. These rising applications have low energy because the primary concern rather than performance, with the ultimate goal of gather energy from the surroundings.

The heat dissipated within the circuit can step by step decrease the performance and conjointly life of the circuit or device. So as to beat these forms of issues, we have a tendency to need low power consumption and fewer dissipation elements within the circuit. He planned two conditions of changeableness. First condition: For any device to be reversible if its input and output are unambiguously recoverable from one another known as logical changeableness. Ordinal condition: a tool will run really backward then it's known as physically reversible.

The reversible circuits area unit those within which reversible logic gates [2] area unit basic building blocks and there's no energy loss. The reversible logic gates [3] are having n-input and the n-output i.e. equal variety of input and an equal variety of output and conjointly with matched mapping i.e. inputs is unambiguously recovered from the outputs. Reversible logic supports the method of running the system each forward and backward.

Reversible Logic: The reversible rationale door will create one of a kind yield vector from extraordinary data vector or bad habit verse. In reversible rationale, Input vector is Iv= (I1,I2,I3… In) and Output vector is Ov = (O1,O2,O3… … On), For every specific vector j Iv ↔ Ov.

Figure: 1 demonstrates a generally reversible door; the entryway will have k inputs and k yields and it is called ak*k reversible entryway. In reversible doors, fan-out are not allowed. No input ways are permitted i.e. circuit is non-cyclic. Some critical elements are Garbage yield, consistent information and so on. Refuse yield is

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the un-used yield from the reversible entryway, all that much key to accomplishing reversibility and it must be not utilized for further calculation. Steady inputs are those that will be added to k*k capacity to make it reversible. For an enhanced reversible circuit, the quantity of trash yields, the quantity of consistent inputs and the quantity of reversible entryways utilized ought to be least.

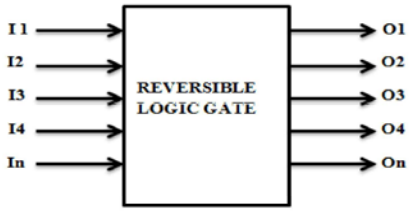

Fig.1: Generally reversible gate

In the design of reversible logic circuits, the following points must be considered to achieve an optimized circuit. They are:

- Fan-out isn't allowed.
- Loop or feedback isn't permissible.
- Garbage outputs ought to be minimum.
- Minimum path delay.
- Minimum quantum price.

Fredkin Gate (FRG): The input vector is I (A,B,C) and therefore the output vector is O (P,Q,R). The output is outlined by P=A, Q=A'B ^ AC and R=A'C ^ AB. The Quantum value of a Friedkin gate is five

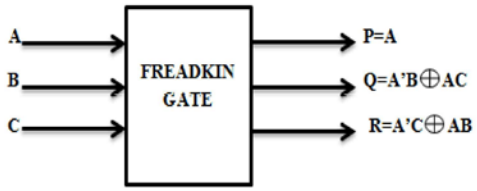

Fig. 2: 3*3 Fredkin gate.

Truth table of parity preserving Fredkin gate [4]:

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

New Fault Tolerant Gate (NFT): The NFT gate could be a 3*3 Reversible gate with 3 inputs and 3 outputs. The input vector is I(A, B, C) and therefore the output vector is O(P, Q, R). The output is outlined by P=A^B, Q=BC^AC', R=BC^AC' and is shown within the Fig. 4.The Quantum price of associate NFT gate is five.

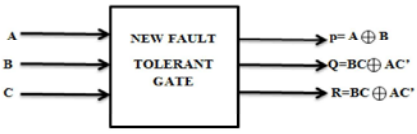

Fig. 3: 3*3 NFT gate.

Truth table of parity preserving Nft gate:

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	1	0	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	0	1	1
1	1	1	0	0	1

Modified Ig Gate (MIG): The MIG gate could be a 4*4 Reversible gate with four inputs and 4 outputs. The input vector is I (A, B, C, D) and also the output vector is O (P, Q, R, S). The output is outlined by P=A, Q=A^B, R= (A&B)^C, S=(A&B)^D and is shown within the Fig. 5. The Quantum price of a MIG gate is seven.

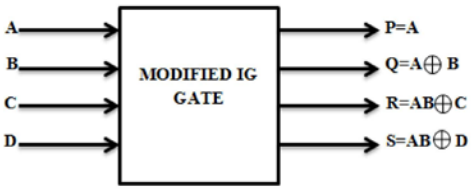

Fig. 4: 4*4 MIG gate.

Truth table of parity preserving mig gate:

Input				Output			
A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1

0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	1	0	1
1	0	0	1	1	1	0	0
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	0
1	1	1	1	1	0	0	1

Feynman Gate: Feynman gate may be a 2x2 reversible gate. The input vector is I (A,B) and thus the output vector is O (P,Q).The output made public by P=A,Q=A ^B. Quantum worth of a Feynman gate is one. Feynman gate is employed as repetition gate.

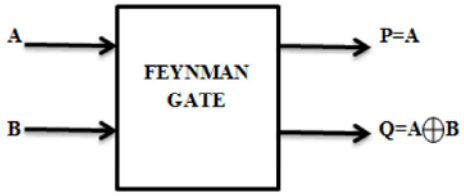

Fig. 5: 2*2 Feynman gate

Truth table of feynman gate

INPUT		OUTPUT	
A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Toffoli Gate: Toffoli gate is 3x3 reversible gate. The input vector is I (A,B,C) and therefore the output vector is O (P,Q,R).The outputs square measure outlined by P=A,Q=B,R=ABC. Quantum value of a TOFFOLI gate is five.

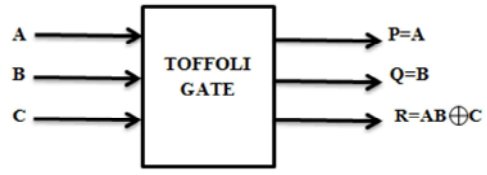

Fig. 6: 3*3Toffoli gate

Truth table of Toffoli gate:

INPUT			OUTPUT		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Peres Gate: Peres gate could be a 3x3 reversible gate. The input vector is I (A, B, C) and therefore the output vector is O(P,R,S). The output is outlined by P=A,Q=A+B and R=ABC. Quantum [5] value of a Peres gate is four.

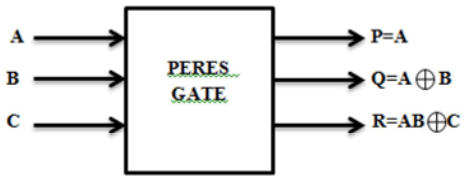

Fig. 7: Peres gate

Truth table of peres gate

INPUT			OUTPUT		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Double Peres Gate (DPG): DPG gate may be a 4x4 reversible gate [6]. The input vector is I (A,B,C,D) and also the output vector is O(P,Q,R,S).The output is P=A,Q=A^B,R=A^B^D and S=(A^B)D^AB^C. Quantum price of DPG gate is six.It will work separately as Reversible full adder with C=0 and D=Cin.

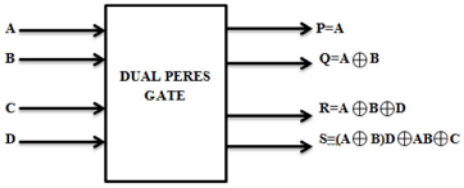

Fig. 8: 4*4 Dual peres gate

Truth table of dual peres gate:

INPUT				OUTPUT			
A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	1	0
1	0	0	1	1	1	1	1
1	0	1	0	1	1	0	1
1	0	1	1	1	1	0	0
1	1	0	0	1	0	0	1
1	1	0	1	1	0	0	0
1	1	1	0	1	0	1	1
1	1	1	1	1	0	1	0

Multiplexer: In physical science, an electronic device (or multiplexer) [7] could be a device that selects one amongst many analogs or digital input signals and forwards the chosen input into one line. An electronic device of 2n inputs has n choose lines; that area unit accustomed choose that input line to send to the output.

Multiplexers area unit in the main accustomed increase quantity |the quantity| the number} of information which will be sent over the network among a precise amount of your time and information measure. An electronic device is additionally known as an information selector. Multiplexers [8] may be accustomed implement mathematician functions of multiple variables.

An electronic, electronic device makes it potential for many signals to share one device or resource, as an example one A/D device or one communication line, rather than having one device per sign.

Conversely, a demultiplexer (or demux) could be a device taking one sign and choosing one amongst several data-output-lines, that is connected to the one input. An electronic device is usually used with a complementary demultiplexer on the receiving finish.

An electronic, electronic device [9, 10] are often thought of as a multiple-input, single-output switch and a demultiplexer as a single-input, multiple-output switch. The schematic image for an electronic device is Associate in Nursing symmetric trapezoid with the longer parallel aspect containing the input pins and, therefore, the short parallel aspect containing the output pin.The schematic on the proper shows a 2-to-1 electronic device on the left and identical start the proper. The seal wire connects the specified input to the output.

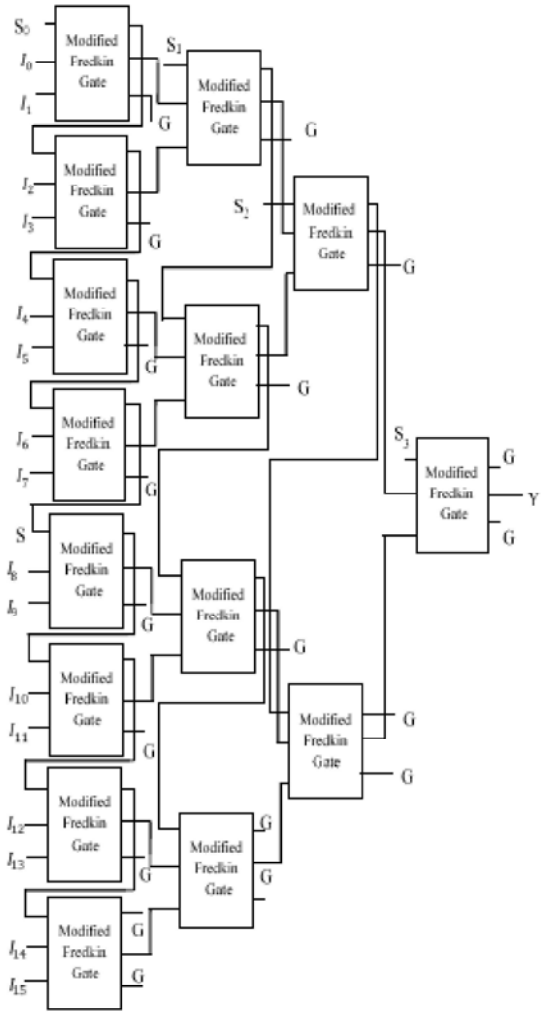

Fig. 9: 16:1 Multiplexer using Fredkin gate

RESULT

Simulation Output:

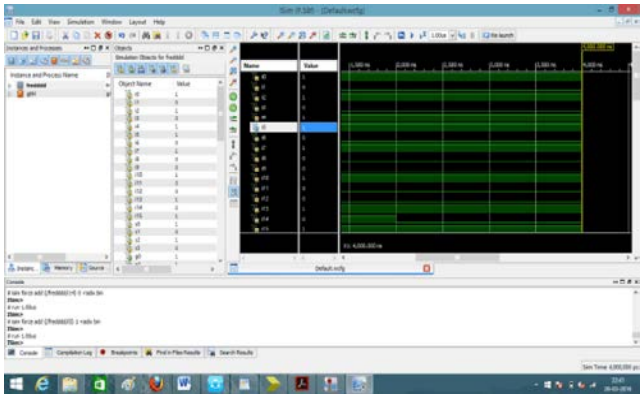

Fig. 10: Simulation output

AREA:

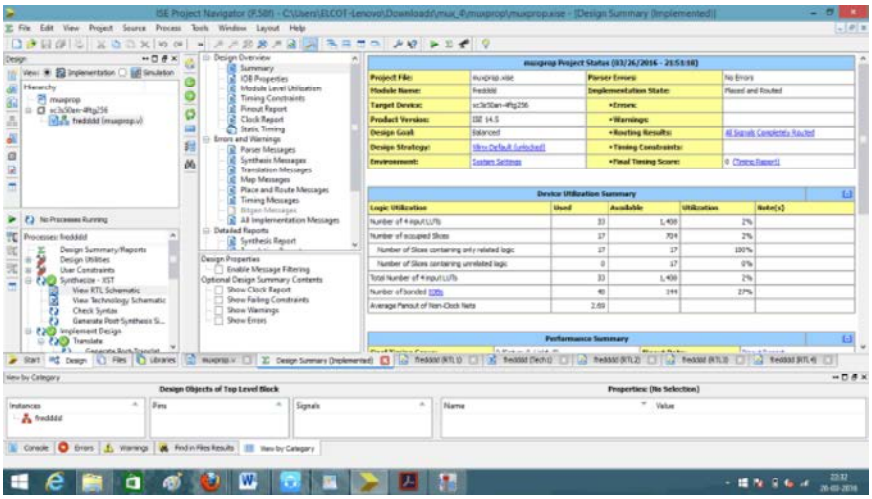

Fig. 11: Performance of area report

Calculate Delay:

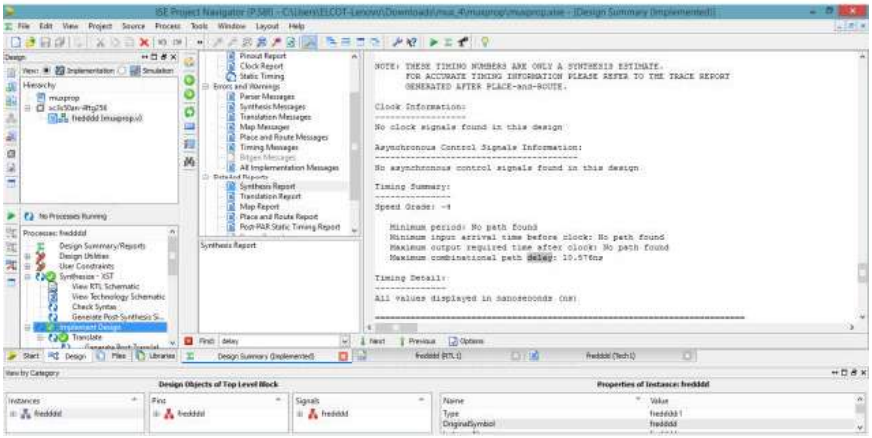

Fig. 12: Performance of path delay

RTL Schematic Diagram:

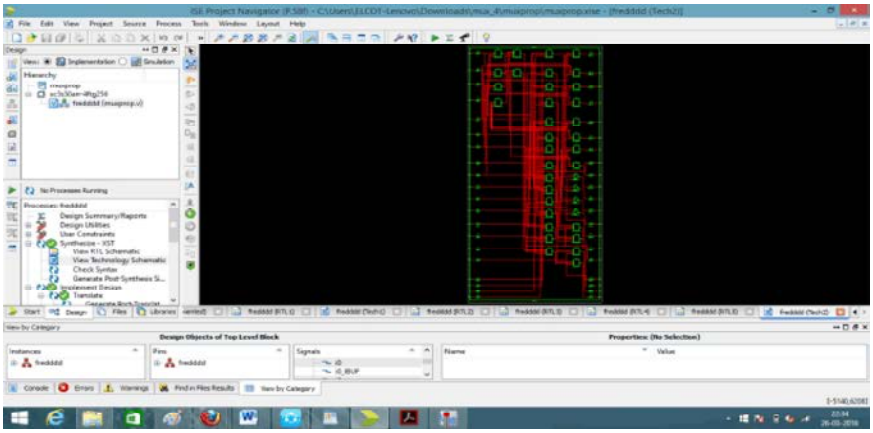

Fig. 13: RTL schematic diagram

Process of Technology:

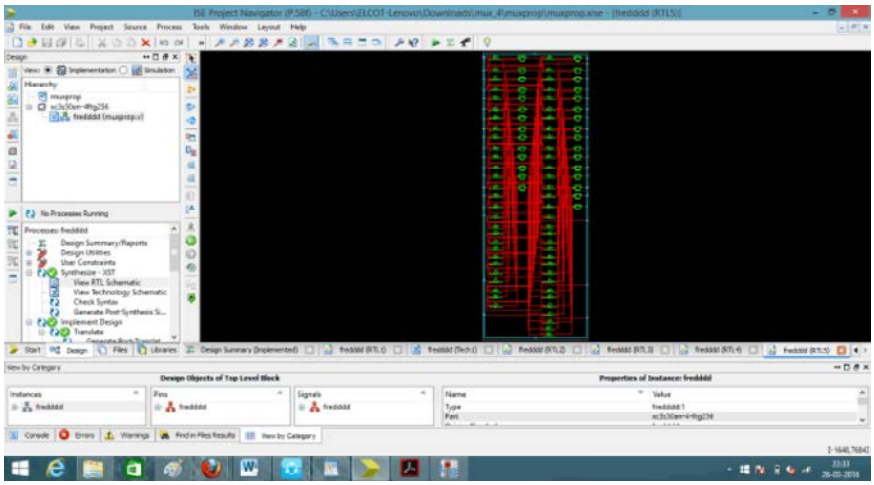

Fig. 14: Technology diagram

Power Consumption:

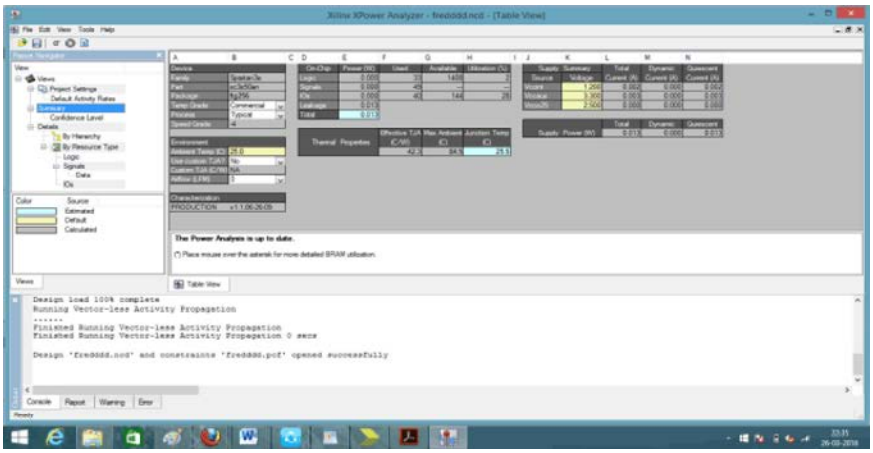

Fig. 15: Power consumption diagram

CONCLUSIONS

Reversible rationale entryways are utilized to Reduced the force utilization, Minimum deferral, Garbage yields ought to be least, Minimum quantum cost, execution is high because of zone is decreased.

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