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Design of an Efficient Codec with 100% Hardware Utilization Ratio Using Hcpm Technique for DSRC Applications

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Abstract: Dedicated short-range communication (DSRC) plays an important role in application for intelligent transportation system. Achieveing maximum hardware efficiency becomes an interesting issue in this. DSRC standards normally employ either FM0 code or Manchester code to improve the reliability of the signal. In this paper, a fully reused VLSI architecture of the codec with a 100% hardware utilization rate (HUR) achieveable technique is proposed. It is done using the half-cycle processing model (HCPM). The HCPM consists of three main sub-techniques: 1) half-cycle logic partition; 2) Boolean function reshaping; 3) reused-based retiming. The improvement of HUR for the codec involving the FMO and Manchester is from 27.33% to 100%. With a design trade-off between HUR and power consumption, this paper still presents a much higher energy efficiency. The experimantal results showcase that this paper presents a challenging output with 100% HUR in comparison with the works that are already in existence.

Key words: DSRC (Dedicated short range communication) · HCPM (Half cycle logic processing) · HCLP (Half cycle logic processing) and RBR (Reshape based retiming) · BFR (Boolean function reshaping)

INTRODUCTION

DSRC: The Dedicated Short-Range Communication (DSRC) is a protocol for one-way or two-way short to medium range communication especially for intelligent transportation systems. Using a modified 802.11a technology for North American cars and trucks [1], DSRC is designed for several applications. For example, ambulances can cause traffic lights down the road to change in their favor and traffic congestion can be transmitted to automobile navigation systems. It allows vehicles to sense that they are about to crash and the safety systems can begin to tighten seatbelts and warm up the airbags before impact [2]. In addition, a standard for wireless payment allows parking lots and fast-food drive-ins to offer the same convenience as the automated highway toll systems such as E-Z Pass. The DSRC can be briefly classified into two categories: automobile-to-automobile and automobile-to-roadside. In automobile-to-automobile, the DSRC enables the message-sending and broadcasting among automobiles for safety issues and public information announcement [3].

The safeties issues include blind-spot, intersection warning, inter cars distance and collision-alarm. The automobile-to-roadside focuses on the intelligen transportation service, such as electronic toll collection (ETC) system. With ETC, the toll-collecting is electrically accomplished with the contactless IC-card platform. Moreover, the ETC can be extended to the payment for parking-service and gas-refueling. Thus, the DSRC system plays an important role in modern automobile industry.

The DSRC standards have been [4] established by several organizations in different countries such as America, Europe and Japan. The data rate individually targets at 500 kb/s, 4 Mb/s and 27 Mb/s with carrier frequency of 5.8 and 5.9 Ghz. In DSRC, a wireless link is established between two basic units: on-board unit (OBU) and roadside unit (RSU)[5]. Consider a sensor node in the WSN for ITS applications. Suppose the OBU represents the sensor node and the RSU represents the data center to collect the information from all sensor nodes in WSN. The OBU should be equipped with a DSRC transceiver to interact with RSU. All above three DSRC standards support half-duplex communication for OBU [6]. This indicates that the OBU activates either transmitting function or receiving function one at a time.

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Architecture of DSRC: The system architecture of DSRC transceiver is shown in Fig. 1.1. The upper and bottom parts are dedicated for transmission and receiving respectively .This transceiver is classified into three basic modules.

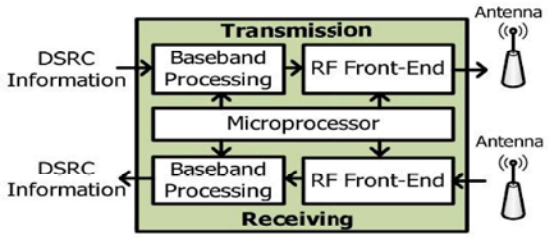

Fig. 1.1: Architecture of DSRC transceiver.

Microprocessor: The microprocessor interprets instructions from media access control to schedule the tasks of baseband processing and RF front-end.

Baseband Processing: The baseband processing is responsible for modulation, error correction and clock synchronization and encoding.

RF Front-end: The RF front-end transmits and receives the wireless signal through the antenna. The modulation methods incorporate amplitude shift keying, phase shift keying and frequency division multiplexing. Generally, the waveform of transmitted signal is expected to have zero-mean for robustness issue and this is also referred to as dc-balance.

The transmitted signal consists of arbitrary binary sequence, which is difficult to obtain dc-balance. The purpose of FM0 and Manchester [7] codes is to provide the transmitted signal with dc-balance. Both FM0 and Manchester codes are widely adopted in encoding for downlink

Literature Review

Dedicated Short Range Communication (DSRC) Standards in United States: The effectiveness of this technology is highly dependent on cooperative standards for interoperability. Included in the discussion are the IEEE 802 [8].11p amendment for wireless access in vehicular environments (WAVE), the IEEE 1609.2, 1609.3. The project shows how these standards fit together to provide a comprehensive solution for DSRC.

FSM Based Fmo and Miller Encoder for UHF RFID Tag Emulator: In this work, we have presented high-level architecture of tag emulator and the design of FM0 encoder and Miller encoder [9]. The synthesis result shows that FSM design is efficient and we have achieved operating frequency of 192.641 MHz and 188.644 MHz for FM0 and Miller encoders [10].

Buffer Minimization in Pass Transistor Logic: In this paper, we first analyze effects of buffer insertion on a circuit and give a sufficient and necessary condition for safe buffer insertion. Then, a buffer minimization problem is formulated. Although it is NP-hard in general, it can be solved linearly when buffers are required on multi fan-out nodes. We also consider the case when buffers are inverters, where phase assignment needs to be done with buffer insertio

FMO and Manchester Codes

Coding Principles of FMO: The FM0 code consists of two parts:

- Former-half cycle of CLK, A
- Later-half cycle of CLK, B.

The coding principle of FM0 is listed as the following three rules.

- If X is logic-0, the FM0 code must exhibit a transition between A and B.
- If X is logic-1, no transition is allowed between A and B.
- The transition is allocated among each FM0 code no matter what X is.

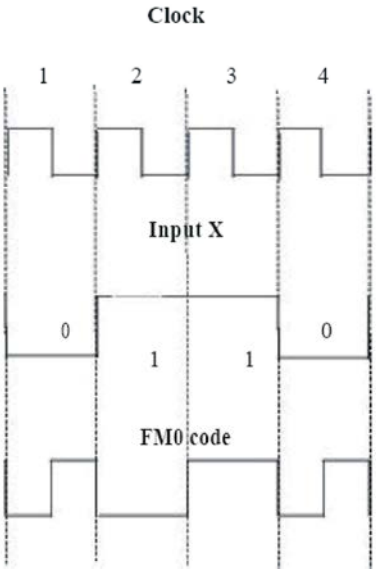

Fig. 3.1: Example of FM0 coding

The Boolean expressions for FMO are,

$$A(t) = B(t-1) \quad (1)$$

$$B(t) = A(t) \oplus B(t-1) \quad (2)$$

The simplified Boolean expression is,

$$CLK\ A(t) + CLK\ B(t) \quad (3)$$

Coding Principles of Manchester: The operation of the Manchester encoder is an exclusive OR of the signal with the clock signal. Then the rising edge will be obtained when the bit value is zero and the falling edge will be obtained in the opposite case . It doesn‘t take on a zero value.

$$\text{Manchester encoding} = X \oplus CLK \quad (4)$$

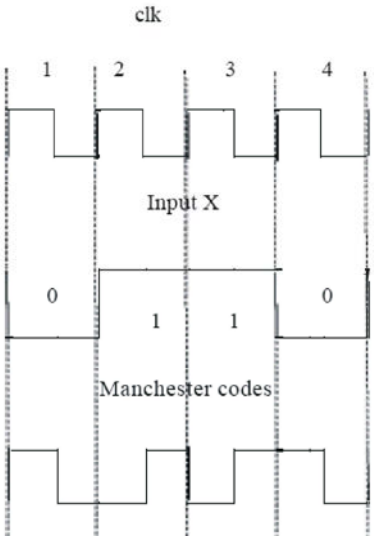

Fig. 3.2: Example of Manchester coding

Hardware Architecture of FMO and Manchester Encoding:

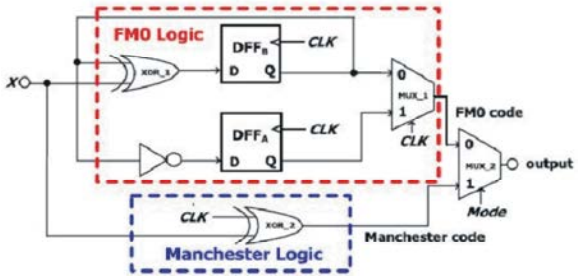

Fig. 3.3: Hardware architecture of FM0 and Manchester encodings

With (3) and (4), the hardware architectures of FM0 and Manchester encoders are shown in Fig. 3.3. The top part is the hardware architecture of FM0 encoder and the bottom part is the hardware architecture of Manchester encoder. As listed in (4), the Manchester encoder is as simple as a XOR operation of *X* and CLK. Nevertheless the FM0 encoding depends not only on *X* but also on the previous-state of the FM0 code. DFF*A* and DFF*B* store the state code of the FM0 code. The function of MUX-1 is to switch a (t) and B (t) through the selection of CLK signal. Both A (t) and B (t) are realized by (1) and (2) respectively. The determination of which coding is adopted depends on the Mode selection of the MUX-2, where the Mode = 0 is for FM0 code and the Mode = 1 for Manchester code. The Hardware utilization ratio (HUR) is defined as the ratio of active components to total components present in the architecture. It can be expressed as below

$$HUR = \frac{\text{Active components}}{\text{Total components}} * 100 \quad (5)$$

The component is defined as the hardware to perform specific logic function such as AND, OR, NOT and flip flop. The active components are the components that work for FM0 or Manchester encoding. The total components are the total number of components in the

Entire hardware architecture no matter which encoding method is adopted. The HUR of FM0 and Manchester encodings is listed in Table 3.1. For both encoding methods, the total components are 7; including MUX-2 to indicate which coding method is activated .For FM0 encoding, the number of active components is 6 and its HUR is 85.71%. For Manchester encoding, the number of active components is 2, comprising XOR-2 and MUX-2 and its HUR is 28.57%. On an average, this hardware architecture has a poor HUR of 57.14% and almost half of total components are wasted.

Table 3.1: Hur of FM0 and Manchester Encodings

Coding	Active components /Total components (transistor count)	HUR
FMO	6(86) / 7(98)	85.71%
Manchester	2(26) / 7(98)	28.57%
Average	4(56) / 7(98)	57.14%

The transistor count of the hardware architecture without SOL’s technique is 98, where 86 transistors are used for FM0 encoding and 26 transistors are used for Manchester encoding. On an average only 56 transistors canbe reused and this is consistent with its HUR. The

coding-diversity between the FM0 and Manchester code seriously limits the potential to design a fully reused VLSI architecture.Using SOLS; we obtain architecture with 100% hardware utilization ratio. This technique has two approaches.

- Area compact retiming
- Balance logic operation sharing. Using this technique, the hardware utilization ratio is improved from 57.14% to 100%.

Proposed SYSTEM

HCPM: (Half Cycle Processing Model): The HCPM is a model of the hardware architecture for FM0/Manchester codec. It classifies FM0/Manchester encoding and decoding into two parts: positive-cycle signal and negative-cycle signal. The HCPM model consists of three core techniques: HCLP, RBR and BFR as in Fig. 4.1.

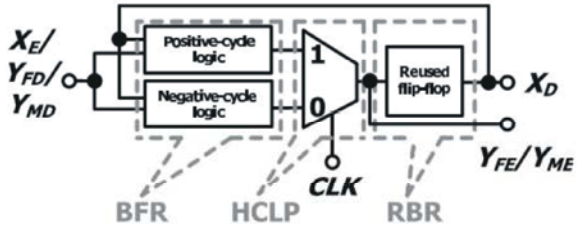

Fig. 4.1: HCPM for FM0/Manchester codec

If FM0/Manchester encoding is adopted, the output of the 2-to-1 multiplexer presents YME/YFE. If FM0/Manchester decoding is adopted, the XD is presented on the output of the reused flip-flop. With HCLP and RBR, the BFR further simplifies positive-cycle logic and integrates negative-cycle logic.

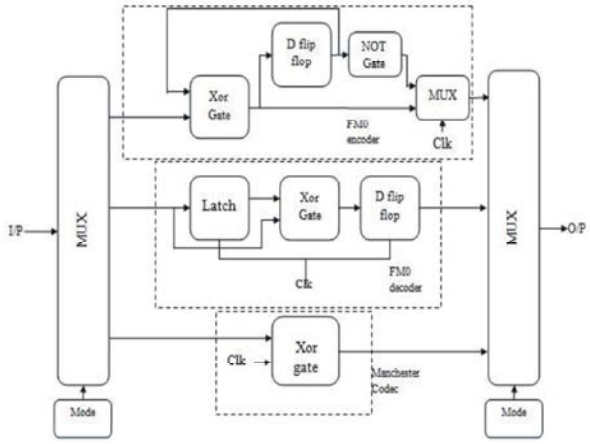

Fig. 4.2: Non-optimized structure for FM0/Manchester codec

Table 4.1: HUR of Non-optimized codec structure

Coding mode	Active transistors/Total transistors	HUR
FM0 encoding	38/86	44.19%
FM0 decoding	40/86	46.51%
Manchester encoding	8/86	9.30%
Manchester decoding	8/86	9.30%
Average	23.5/86	27.33%

HCLP: (Half Cycle Logic Processing): HCLP mainly focuses on the positive-cycle logic and the negative-cycle logic of FMO and Manchester encoding/decoding. The X denotes XE for Manchester encoding or YMD for Manchester decoding. A 2-input XOR gate can be transformed to a 2-to-1 multiplexer and so the positive-cycle logic and the negative-cycle logic of Manchester codec are XE / YMD and XE /YMD respectively.

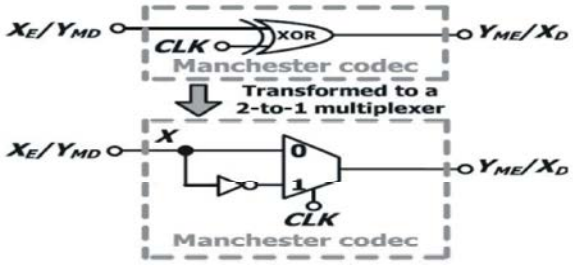

Fig. 4.3: A transformation of Manchester codec from a 2-input *XOR* gate to a 2-to-1 multiplexer

The 2-to-1 multiplexer is organized into FM0 decoder as a pseudo-multiplexer, as shown in Fig. 4.4. This pseudo-multiplexer has two identical inputs. Since both positive and negative cycles are identical and using this pseudo-multiplexer, the data path of FM0 decoder can be fitted into positive-cycle logic and negative-cycle.

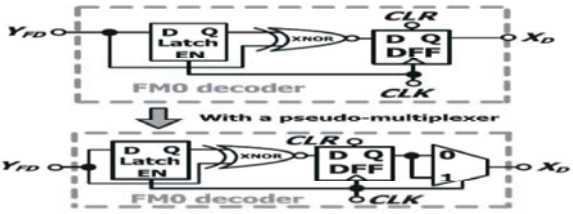

Fig. 4.4: Hardware architecture of FM0 decoder with a pseudo- multiplexer

RBR Technique: (Reused Based Retiming): As earlier shown in the Fig. 4.2, FM0 encoder and FM0 decoder requires a DFF which consumes the most transistors of 22 in all logic components as in Fig. 4.4. The HUR of FM0/Manchester codec can be greatly improved, if the DFF can be reused. It is the purpose of RBR to conduct a

reused DFF from positive-cycle logic and negative-cycle logic in FM0/Manchester encoding and decoding For FM0 decoder, positive-cycle logic and negative-cycle logic are identical. As a result, the DFF in Fig. 4.1 is originally reused with both. To fit the HCPM in Fig. 4.1 is directly relocated backward after the multiplexer, as shown in Fig. 4.5.

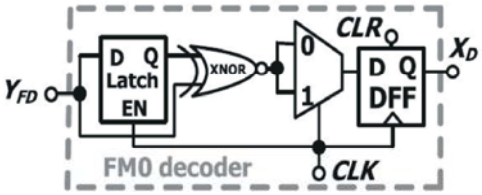

Fig. 4.5: FM0 decoder with RBR technique

For FM0 encoder, to conduct a reused DFF from YFP (t) and YFN(t), two conditions should be satisfied.

- Both YFP (t) and YFN (t) are required to be stored into two individual DFFs.
- The data paths from these two DFFs to a multiplexer are symmetrical.

With above two conditions, these two DFFs can be reduced to a single one, relocated after a multiplexer as a reused DFF.

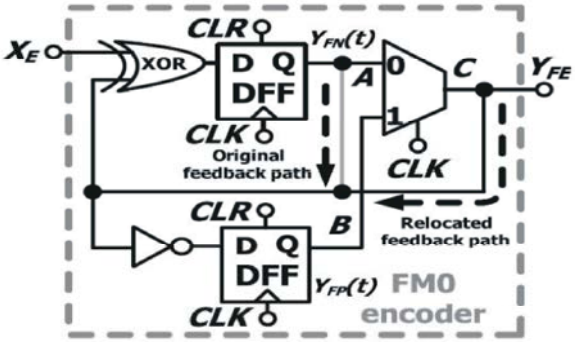

Fig. 4.6: Relocated feedback path.

The feedback path is referred to as the original feedback path marked by a gray solid-line from A to B. The B is periodically updated by YFN(t) at the positive-edge of the CLK. Consider the relocated feedback path from C to B, Both YFP(t) and YFN(t) sequentially appear on B at CLK = 1 and CLK = 0 respectively. The difference between these two timing diagrams is the life-time of YFN (t) on B. The life-time of YFN (t) on B in the original feedback path is two times as long as that in the relocated feedback path. With the relocated feedback path, the data paths from both DFFs to the multiplexer become symmetrical and thereby the second condition is satisfied. Then, these two DFFs are replaced by a reused DFF, located after the multiplexer, as shown in Fig. 4.7.

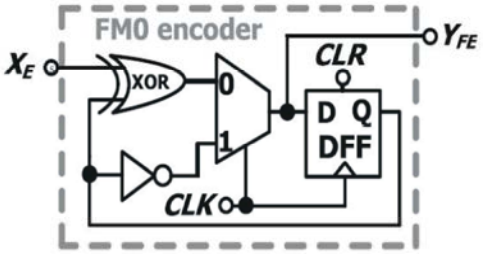

Fig. 4.7: FM0 encoder with RBR technique.

Note that in this hardware architecture, the life-time of YFN (t) on B is still an entire cycle, which is identical to that in the original feedback path. For the Manchester codec in Fig. 4.3, a DFF is directly placed after the multiplexer, as shown in Fig. 4.8. The YME and the XD are on the outputs of the multiplexer and the DFF, respectively. Actually, the XD can be also obtained on the output of the multiplexer.

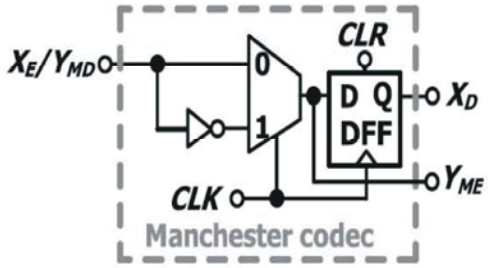

Fig. 4.8: Manchester codec with RBR technique

BFR Technique: (Boolean Function Reshaping): The purpose of BFR is to simplify positive-cycle logic and integrate negative-cycle logic. The simplified positive-cycle logic and the integrated negative-cycle logic are individually discussed in following subsections.

- Simplified Positive-Cycle Logic
- Integrated Negative-Cycle Logic

Simplified Positive-Cycle Logic: There is no data dependency between positive-cycle logic and negative cycle logic in FM0/Manchester decoding. Hence, the positive cycle logic of FM0/Manchester decoding can be omitted. This feature can be observed from FMO/ Manchester decoding waveform. As a result, the positive-cycle logic can be omitted.

Integrated Negative-Cycle Logic: The XOR inFM0 encoding and the XNOR in FM0 decoding are most complex functions in negative-cycle logic. If the other negative-cycle logic can be integrated with them, the HUR of FM0/Manchester codec can be greatly improved. To reach this target, the other negative-cycle logic is transformed to XNOR function. After optimizing the Fig. 4.2 using the three techniques, the proposed VLSI hardware architecture of FM0/Manchester codec is as shown in Fig. 4.9. The simplified positive-cycle logic is reused with the integrated negative-cycle logic by the output of MUXB.

Fully Optimized FM0/manchester Codec: The proposed FM0/Manchester codec supports four coding modes, including FM0 encoding/decoding and Manchester encoding/decoding. Each coding mode is specified by four parameters, SP, SN, I1 and I0, as listed in Table 4.2. The output of INVA denotes YFE for FM0 encoding or YME for Manchester encoding

Table 4.2: Coding Modes

Types of Coding	SP	SN	I1	I0
FMO Encoding	1	0	0	1
FMO Decoding	0	0	1	0
Manchester Encoding	0	1	0	1
Manchester Decoding	0	0	1	1

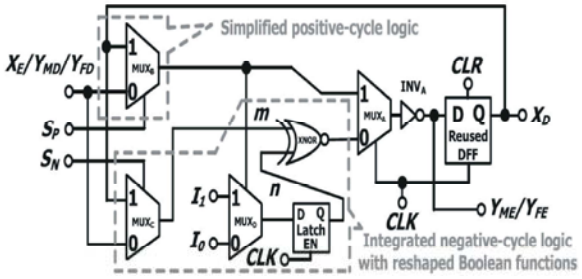

Fig. 4.9: Proposed VLSI hardware architecture of FM0/Manchester codec

This hardware architecture has three advantages listed as,

- Every logic component is fully-reused, no matter which element in N is adopted.
- Only one multiplexer MUXD is required in the data path of n.
- The control signal of MUXD is reused with the output of MUXB without any extra logic.

Thus the output of reused DFF represents XD for FM0 decodes or Manchester decoding and is valid every cycle. Every logic component is fully-reused, no matter which coding mode is activated. No logic component is wasted; therefore, the HUR of FM0/Manchester codec is as high as 100%.

RESULTS

Different Modes are adopted in CODEC Structure for FM0 and MANCHESTER Encoding and Decoding, given as SP, SN, I0, I1 where SP and SN are select lines to Multiplexer B and Multiplexer C respectively and I0, I1 are inputs to Multiplexer D.

FM0 Encoding: The Mode given for FM0 encoding is 1001 and it can be observed that when input in is 0, a transition is exhibited for every half cycle and when the input is 1, no transition would be exhibited and it is observed in ye.

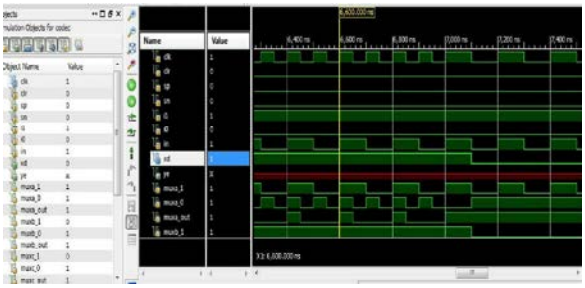

Fig. 6.1: Simulation of FM0 Encoding

FM0 Decoding: The Mode given for FM0 decoding is 0010 and it can be observed that when input in is 0, a transition is exhibited for every half cycle and when the input is 1, no transition would be exhibited and it is observed in xd.

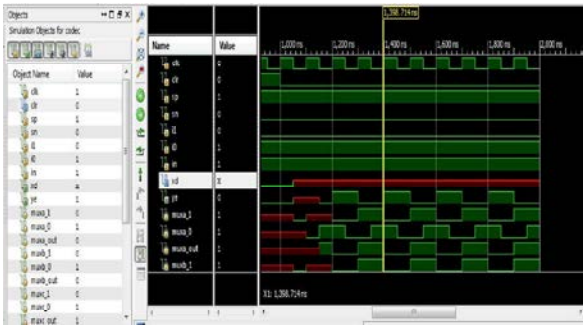

Fig. 6.2: Simulation of FM0 Decoding

Manchester Encoding: The Mode given for MANCHESTER encoding is 0101 and it can be observed that output is obtained by performing XOR operation between Clk and input in and output is observed in ye.

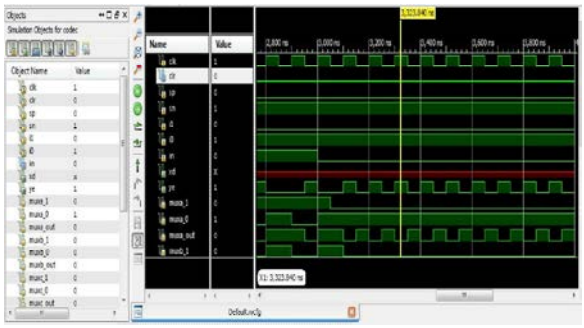

Fig. 6.3: Simulation of Manchester Encoding

Manchester Decoding: The Mode given for MANCHESTER decoding is 0011 and it can be observed that output is obtained by performing XOR operation between.

Clk and input in and output is observed in xd.

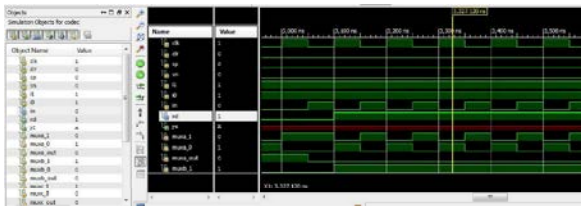

Fig. 6.4: Simulation of Manchester Decoding

Device Utilization Summary: The Device Utilization Summary for Non-optimized codec Structure given below utilizes 9% of IOBs and 12% of BUFG.

Table 6.1: Utilization summary for Non-optimized Codec

Logic Utilization	Used	Available
Number of Slice Registers	6	4800
Number of Slice LUTs	7	2400
Number of fully used LUT-FF pairs	0	13
Number of bonded IOBs	10	102
Number of BUFG/BUFGCTRLs	2	16

The Device Utilization Summary for Optimised codec structure given below utilizes 8% of IOBs and 12% of BUFG

Table 6.2: Utilization summary for Optimized Codec

Logic Utilization	Used	Available
Number of Slice Registers	3	4800
Number of Slice LUTs	7	2400
Number of fully used LUT-FF pairs	0	10
Number of bonded IOBs	9	102
Number of BUFG/BUFGCTRLs	2	16

Inference

Hur for Codec Structure:

Number of Active Transistors = 66
Total number of Transistors = 66
Where every D-FF utilizes 22 Transistors
MUX utilizes 6 Transistors
XNOR utilizes 8 Transistors
NOT utilizes 2 Transistors
LATCH utilizes 10 Transistors

Hardware utilization rate (HUR) is defined as;

$$HUR = \frac{\text{Active components}}{\text{Total components}} * 100$$

$$= (66/66) * 100 = 100\%$$

CONCLUSION

DSRC can provide a wireless link for sensor networking in ITS applications. It achieves higher hardware efficiency up to 100% . In this project, a fully reused VLSI architecture of FM0/Manchester codec with the HUR of 100% is proposed for DSRC-based sensor node. It is based on the HCPM, incorporating HCLP, RBR and BFR. The HCLP is responsible to classify FM0/Manchester codec into the positive-cycle logic and negative-cycle logic. The RBR can conduct a reused flip-flop from positive-cycle logic and negative-cycle logic. The BFR further simplifies positive-cycle logic and integrates negative-cycle logic. With the HCPM, the HUR of FM0/Manchester codec is improved from 27.33% to 100%.

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