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Implementation of 13 Level Full Bridge Switched Capacitor Inverter With Self Voltage Balancing

B. Veeramuthupandian and P. Usha Rani

Department of Electrical & Electronics Engineering,
J.N.N Engineering College, R.M.D. Engineering College, Chennai

Abstract: This paper proposes a step-up switched-capacitor multilevel inverter topology. The proposed system consists of multilevel dc-dc converter and full bridge topology. The dc-dc converter is based on switched capacitor (SC) technique to achieve the multilevel output voltage with reduced number of switches. The proposed system is to avoiding the voltage balancing problem. Finally, the performance of the proposed multilevel inverter is evaluated with the simulation as well as experimental results of an 13-level prototype inverter.

Key words: H-bridge · Multilevel inverter · Selective harmonic elimination (SHE) · Sinusoidal pulse width modulation (SPWM) · Switched capacitor (SC)

INTRODUCTION

With the increasing higher power quality requirements for numerous industrial applications and renewable energy sources such as photovoltaic, wind and fuel cells, classical three level inverters have difficulty in meeting these requirements of clean non polluted sinusoidal waveforms and a minimal distortion factor. As a result, multilevel inverters have been introduced as an alternative in high power quality situations. For several attractive features, such as near-sinusoidal staircase output voltage waveforms, reduced dv/dt stress, operating with a lower switching frequency stress, etc. [1], multilevel inverters, as an alternative solution, have been receiving much attention. As a result, many different topologies and a wide variety of control strategies have been proposed [2].Conventionally, multilevel inverter topologies can be divided into three categories, i.e., neutral-point-clamped inverters [3], flying capacitors [4] and the H-bridge cascade [5, 6]. In many industrial applications, these inverters have been playing motor drivers because of their good performance [7], [8]. In recent years, numerous new multilevel inverter topologies that cannot be attributed to the traditional three classifications aforementioned have been reported in [9] and [10]. Specifically, multiple sub multilevel converter units and full bridge converters are employed in the new multilevel inverter topology. In, a simple topology is proposed, but multiple separated dc voltage sources are still required. The coupled-inductor technique used in multilevel inverters was introduced in and. The structures are simplified, but it is difficult to expand this technique to higher level applications. In and, novel topologies based on switched capacitor (SC) and boost techniques were presented. In contrast, the multilevel topology introduced in can be extended to higher levels. Based on the SC technique that has been applied in many applications, a novel multilevel inverter topology connecting a multilevel dc– dc converter and a full bridge is presented in this paper. With the proposed topology, only one dc voltage source is required and many other problems, such as voltage balancing, numerous active switches and complex gate driver circuits, are avoided. The dc–dc conversion section is the key point of the whole topology, which is designed by connecting multiple SC cells. Each SC cell consists of a capacitor, an active switch and two diodes. Consequently, the output voltage levels of the proposed inverter could be flexibly varied by employing different numbers of SC cells.

Topology: The proposed multilevel inverter is cascaded by a dc–dc multilevel converter and a full bridge, as shown in Fig. 1. For its dc–dc converter section that consists of the number of n SC cells, it is capable of

Corresponding Author: B. Veeramuthupandian, Department of Electrical & Electronics Engineering, J.N.N Engineering College, R.M.D Engineering College, Chennai, India.

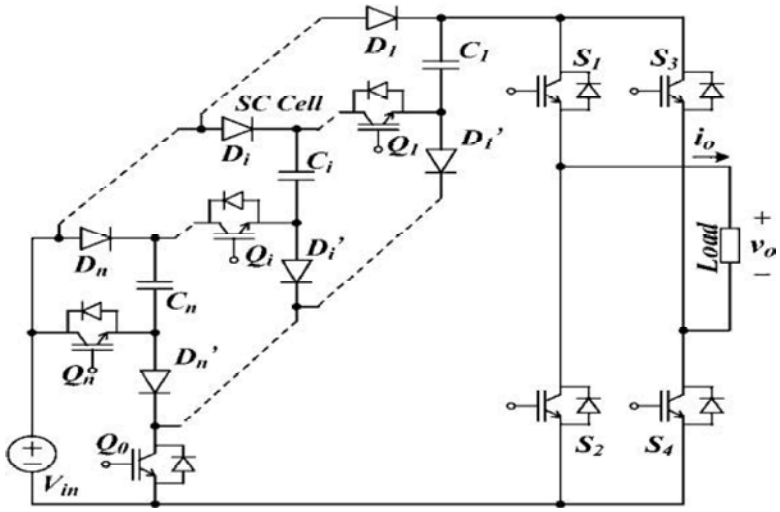

Fig. 1: Topology of the proposed multilevel inverter

providing the number of n + 1voltage levels according to different switching states. With the operation of the H-bridge, a total of $2n + 3$ voltage levels can be produced, i.e., 0, ±Vin, ±2Vin, . . . , ±(n + 1)Vin. Without loss of generality, the following assumptions have been made for analysis.

- The values of all SCs Ci are large enough and the voltage ripples across them are negligible.
- All the switching devices are ideal, i.e., no ON-state voltage drop and on-resistance.
- Input power source VIN is ideal, i.e., it is constant and there is no series impedance.

Here, modes of operations are divided into four more types. They are zero level output, level of $\pm v_{in}$ output, level of $\pm i \times v_{in}$ output, level of $\pm(n + 1)v_{in}$ output and etc., In zero level output mode, When switch Q turned on while Qi (i=1, 2, ..., n) is off and all SCs Ci are charged by input power source V_{in} through diodes Di and D_i',. For the H-bridge, only switch S_1 is turned on, whereas the others are off. There is no voltage developed for the load. The output voltage is therefore equal to zero. Similarly; other modes are operated. Hence, variable output voltage is possible.

Modulation Strategies: A variety of modulation strategies have been used in multilevel inverters to synthesize the output voltage as close as possible to the sinusoidal waveform. These modulation methods can be classified into two main categories according to the switching frequency, i.e., the high-frequency modulation (HFM) and the fundamental frequency modulation (FFM).

Table 1: Combination of the Working States for The Proposed Inverter

No. of states	Switching states										Output levels
	Q_0~Q_n						S_1~S_4				
1	0	1	1	1	1	1	1	0	0	1	$+(n+1)V_{in}$
2	0	1	1	1	1	0	1	0	0	1	$+n\times V_{in}$
⋮	0	1	1	1	...	0	1	0	0	1	⋮
n-i+1	0	1	1	1	0	0	1	0	0	1	$+(i+1)V_{in}$
n-i+2	0	1	1	0	0	0	1	0	0	1	$+i\times V_{in}$
⋮	0	1	...	0	0	0	1	0	0	1	⋮
n	0	1	0	0	0	0	1	0	0	1	$+2V_{in}$
n+1	1	0	0	0	0	0	1	0	0	1	$+V_{in}$
n+2	1	0	0	0	0	0	1	0	0	0	0
n+3	1	0	0	0	0	0	0	1	0	0	
n+4	1	0	0	0	0	0	0	1	1	0	$-V_{in}$
n+5	0	1	0	0	0	0	0	1	1	0	$-2V_{in}$
⋮	0	1	...	0	0	0	0	1	1	0	⋮
n+i+3	0	1	1	0	0	0	0	1	1	0	$-i\times V_{in}$
n+i+4	0	1	1	1	0	0	0	1	1	0	$-(i+1)V_{in}$
⋮	0	1	1	1	...	0	0	1	1	0	⋮
2n+3	0	1	1	1	1	0	0	1	1	0	$-n\times V_{in}$
2n+4	0	1	1	1	1	1	0	1	1	0	$-(n+1)V_{in}$

HFM for Proposed Inverter: For the HFM methods, there are many commutations for the power switches in one period of the fundamental output voltage. The HFM can be further divided into several specific modulation methods, of which a very popular method is the multilevel carrier-based sinusoidal pulse width modulation (SPWM). Therefore, this method will be introduced to control the proposed inverter and is discussed as follows. For the proposed (2n + 3)-level inverter, 2n + 2 triangular carriers are needed. The carriers have the same peak-to peak amplitude AC and the same frequency f_c. The modulating signal is a sinusoidal waveform with frequency f_c and amplitude A_c.During each period of the fundamental cycle,

each carrier is compared with the modulating signal and the results of the comparison are used to control the corresponding active switches, as shown in Fig.2.5, in which

$\pm e\,0, \pm e1, ..., \pm ei, ..., \pm en$

are carriers and *es* is the modulating signal.All of them can be mathematically described as;

$$e_s = A_s \sin(2\pi f_s t) \quad (1)$$

$$e_o = \begin{cases} 2A_c f_c (t - \frac{k-1}{f_c}), & \frac{k-1}{f_c} < t \le \frac{2k-1}{2f_c} \\ A_c[1 - 2f_c(t - \frac{2k-1}{2f_c})], & \frac{2k-1}{2f_c} < t \le \frac{k-1}{f_c} \end{cases} \quad (2)$$

$$\begin{cases} e_i = i * A_c + e_o \\ i = 1, 2, \ldots n \end{cases} \quad (3)$$

$$M_a = A_s / (n+1) A_c \quad (4) \quad M_f = f_c / f_s \quad (5)$$

where k is the number of triangle waves. It is a natural number and ranged from 1 to infinity.

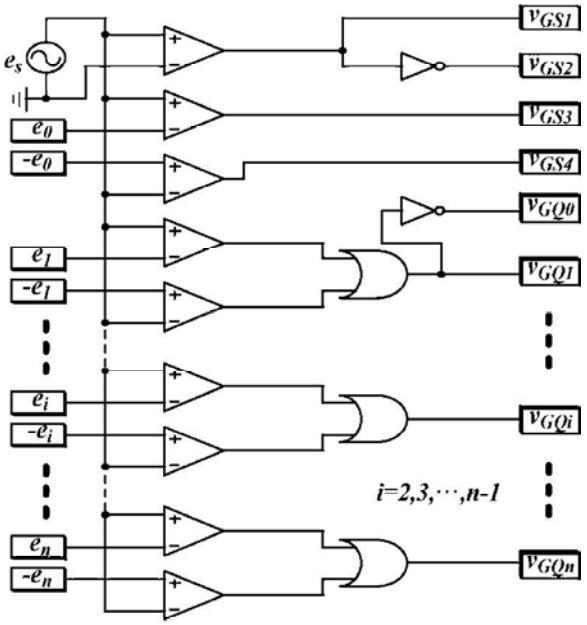

Fig. 2: Multicarrier logic modulating circuit for the proposed inverter

FFM for the Proposed Inverter: For the FFM methods, a staircase voltage waveform is generated by connecting different numbers of capacitor sources to the output terminal and with only one or two commutations of active switches during one cycle of the fundamental output voltage. A representative of this family is the selective harmonic elimination (SHE) method. It was also introduced to modulate the proposed inverter to output a staircase voltage. The following table clearly explain FFM analysis for the proposed inverter are shown in Table 2.

Table 2: FFM for the Proposed Inverter

Level	Q0	Q1	Q2	Q3	Q4	S1	S2	S3	S4	Voltage across level
Zero	1	0	0	0	0	1	0	0	0	0
Level 1	1	0	0	0	0	1	0	0	1	34.9
Level 2	0	1	0	0	0	1	0	0	1	69.8
Level 3	0	1	1	0	0	1	0	0	1	103.6
Level 4	0	1	1	1	0	1	0	0	1	138.2
Level 5	0	1	1	1	1	1	0	0	1	170.2

Simulation Results: Developing switched capacitor based MLI for 13-level with stair case modulation technique is simulated in MATLAB Simulink for performance analysis. Circuit analysis, performance will be shown as snapshot in below. Table 3 shows parameters of proposed inverter.

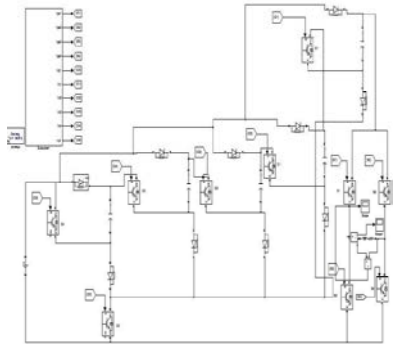

Fig. 3: Proposed System Simulation Circuit

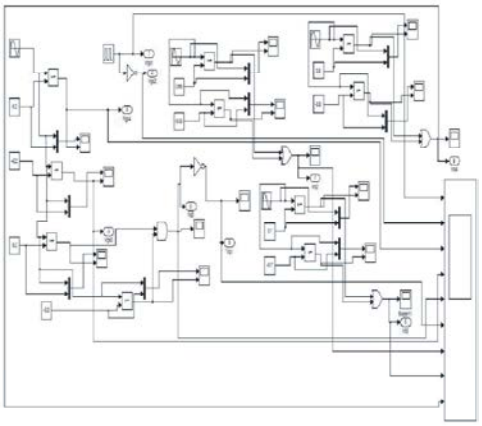

Fig. 4: Modulation for Proposed Design

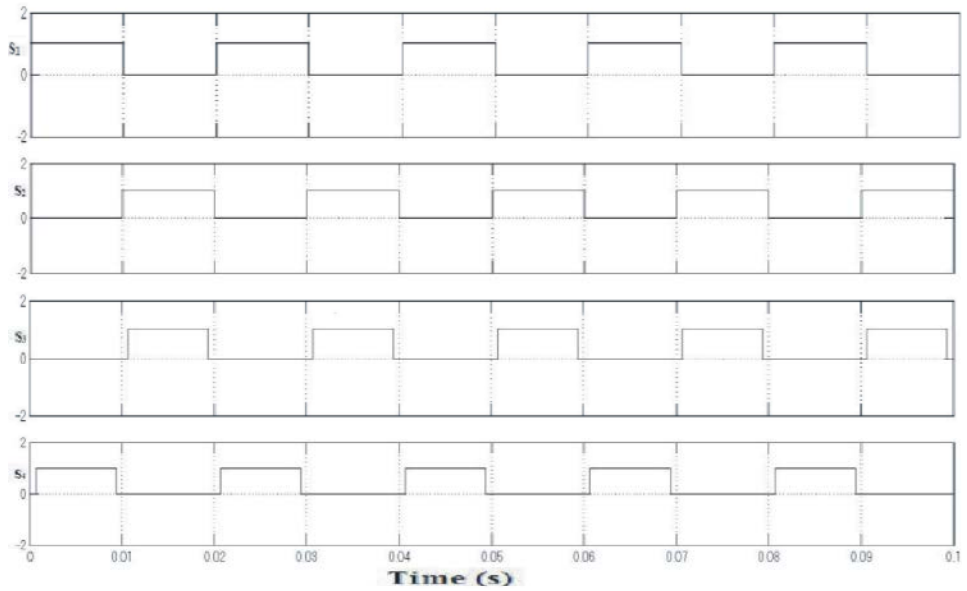

Fig. 5: Gate Pulse for S1, S2, S3,

Table 3: Parameters for the Proposed Inverter

S.NO	Parameters	Value
1	Input voltage in V	12V
2	Output voltage in V	60V
3	THD in output	5.47
4	Power factor in output	0.95 app
5	Level in output waveform	13
6	Modulation	SPWM

Table 4: Comparison between Existing and Proposed Inverter

Parameters analysis	Existing system	Proposed system
Output voltage waveform	Square waveform	Stepped sine waveform (13-level)
THD	45.68%	5.47%
Power factor	<8.5	0.95

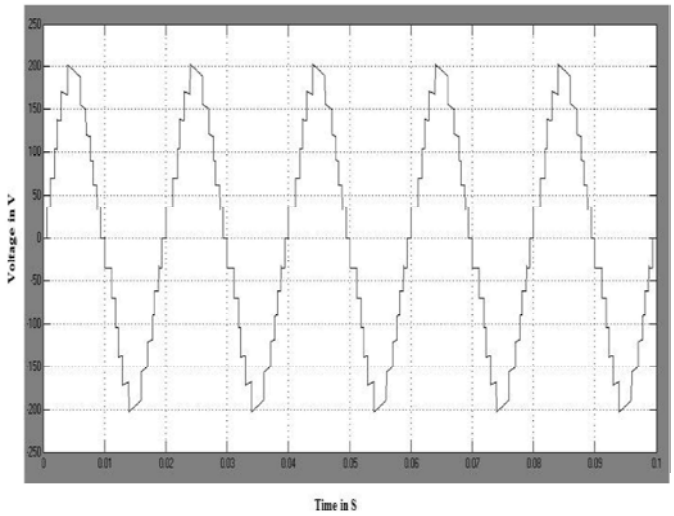

Fig. 6: Proposed inverter output voltage waveform [13-level]

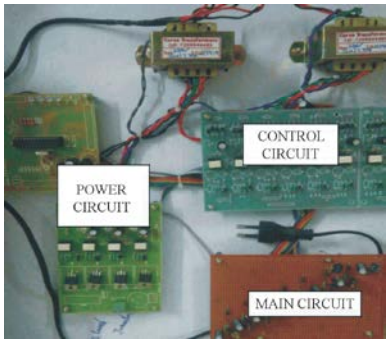

Fig. 7: Proposed Hardware circuit

CONCLUSION

In this project, a Full Bridge SC 13-level inverter, which is a combination of a multilevel dc–dc converter and a full bridge, has been proposed. The dc–dc conversion section consists of multiple SC cells. By connecting different numbers of SC cells the output voltage level could be varied flexibly. It has been analyzed that the proposed inverter provides $2n + 3$ levels on the output voltage, using only n capacitors and $n + 5$ active switches. It enables the simple structure and low cost of the gate driver circuits. Meanwhile, the high switching frequency modulation and fundamental switching frequency modulation methods for the proposed inverter are discussed. Proposed inverter. In addition, the voltage ripples across capacitors and power losses are analyzed in detail. Finally, the operation and performance of the proposed inverter are verified with experiments on a 13-level inverter prototype.

Future Scope: As we have said that this project can be implemented in renewable system (Photovoltaic system) both in residential based or industrial based application. If we are going for PV based application then we can also implement the MPPT control techniques for to get better output. At the output side we can also improve the levels so that the THD can be minimized beyond the proposed level. Recent days DAIKINS Air Conditioner Companies are using such type of inverter. So we can also develop our project according to such a requirement.

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