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Multilevel Inverter Topology with Reduced Number of Switches Using Switched DC Sources

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Abstract: Power-electronic inverters are becoming popular for various industrial drives applications. The multilevel inverter was introduced as a solution to increase the converter operating voltage above the voltage limits of classical semiconductors. In this paper new multilevel inverter that has been hypothesized to decrease the number of switching devices and other components, particularly in higher output levels. It involves floating input dc sources connected alternately in opposite polarities with one another through power switches. The working principle of this proposed technique is verified with the help of a single-phase five-level inverter and the quality of the multilevel waveform is enhanced by increasing the number of levels to seven-level output. This approach results in reduced number of power switches as compared to conventional topologies.

Key words: Multilevel inverter (MLI)

INTRODUCTION

In recent years also high-power and medium-voltage drive applications have been installed. To overcome the limited semiconductor voltage and current ratings, some kind of series and/or parallel connection will be necessary. A multilevel inverter (MLI) is a linkage structure of multiple input dc levels (obtained from dc sources and/or capacitors) and power semiconductor devices to synthesize a staircase waveform.The multilevel voltage source inverter is recently applied in many industrial applications such as ac power supplies, static VAR compensators, drive systems, etc. One of the significant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output. The output voltage waveform of a multilevel inverter is composed of the number of levels of voltages, typically obtained from capacitor voltage sources. The so-called multilevel starts from three levels. As the number of levels reach infinity, the output THD (Total Harmonic Distortion) approaches zero.In addition, the multilevel waveform has a better harmonic profile as compared to a two-level waveform obtained from conventional inverters. Other advantages of MLIs are reduced *dv/dt* stress on the load and possibility of fault tolerant operation. The proposed topology may also be suitable for battery-powered applications. The existing system results only with symmetrical output voltages whereas the proposed scheme will be able to provide the output voltages in asymmetrical nature also.A comparison of the proposed topology with classical topologies is presented.

Proposed System: Here the structure of the proposed topology is introduced and its working principle is explained with the help of a single-phase five-level inverter. The generalized single-phase structure of the proposed topology is shown in Fig. 1. Here it has n number of isolated input dc sources and the higher potential terminal of the preceding source is connected to the lower potential terminal of the succeeding source and vice versa through power switches. In this topology input sources are designated as E_j(where j = 1 to n). Source current from each source is designated as $i_j(t)$. Here power switches can be implemented by using a transistor device [e.g., MOSFET and insulated-gate bipolar transistor (IGBT)] with an anti-parallel diode. $v_j(t)$ (where j = 1 to n

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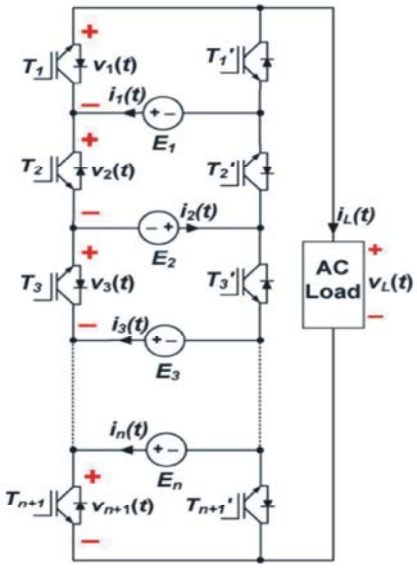

Fig. 1: Generalized single-phase structure of the proposed topology

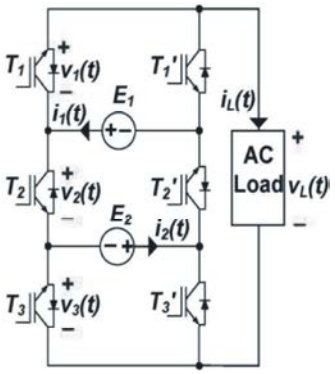

Fig. 2: Single-phase inverter based on the proposed topology with two input sources

+ 1) are used to indicate nodal voltages and $v_L(t)$ and $i_L(t)$ are used to indicate load voltage and load current respectively. Now the single-phase inverter with two input dc sources E_1 and $E_2$is used to explain the working principle of the proposed topology, as shown in Fig. 2. The three pairs of active switches are (*Tj, T'j*) where (*j* = 1, 2, 3). There are eight valid operating modes as the elements are complementary.

The eight modes are shown in Fig. 3 and their operating features with nodal voltages and source currents are clearly depicted in Table 1. Five level load is supplied such that $\pm V_{dc}$, $\pm 2V_{dc}$ and zerofor $E_1 = E_2 = V_{dc}$. It is to be noted that all positive voltage levels and one "zero" level (modes 1, 3, 4 and 5) always conducts with switch T'_2 and all negative voltage levels and another "zero" level (modes 2, 6, 7 and 8), always conducts switch T_2.

Hence desired level output is obtained by operating those two switches at fundamental frequency.Losses incurred can be described under three categories: 1) when the device is blocking (i.e., OFF state); 2) when the device is conducting (i.e., ON state); and 3) when the device is switching (i.e., the state is changing from ON to OFF or vice versa). The losses are insignificant since leakage currents during blocking state are practically negligible. Only conduction and switching losses are considered forthe proposed inverter.

Switching Scheme: For modulation control of MLI, high-switching-frequency modulation methods like multicarrier PWM and space vector modulation techniques have been used. Some low-switching-frequency methods considered are active harmonic elimination, selective harmonic elimination and fundamental frequency methods. In this paper, the multicarrier PWM scheme is used. The pulses obtained are used for switching of devices corresponding to respective voltage levels and carrier signals are compared with the reference signal. More than one level at output terminals can be synthesized by one switch. To obtain a five-level

Table 1: Modes, Switching States, Nodal Voltages and Source Currents for the Proposed Topology with Two Input Sources

	Switch states(1=on;0=off)						Nodal voltages			Source currents		Output voltages
Mode	T_1	T_1'	T_2	T_2'	T_3	T_3'	$V_1(t)$	$V_2(t)$	$V_3(t)$	$i_1(t)$	$i_2(t)$	$V_L(t)$
1	0	1	0	1	0	1	$-V_{dc}$	$2V_{dc}$	$-V_{dc}$	0	0	0
2	1	0	1	0	1	0	0	0	0	0	0	
3	1	0	0	1	0	1	0	$2V_{dc}$	$-V_{dc}$	$i_L(t)$	0	$+V_{dc}$
4	0	1	0	1	1	0	$-V_{dc}$	$2V_{dc}$	0	0	$i_L(t)$	
5	1	0	0	1	1	0	0	$2V_{dc}$	0	$i_L(t)$	$i_L(t)$	$+2V_{dc}$
6	0	1	1	0	1	0	$-V_{dc}$	0	0	$-i_L(t)$	0	$-V_{dc}$
7	1	0	1	0	0	1	0	0	$-V_{dc}$	0	$-i_L(t)$	
8	0	1	1	0	0	1	$-V_{dc}$	0	$-V_{dc}$	$-i_L(t)$	$-i_L(t)$	$-2V_{dc}$

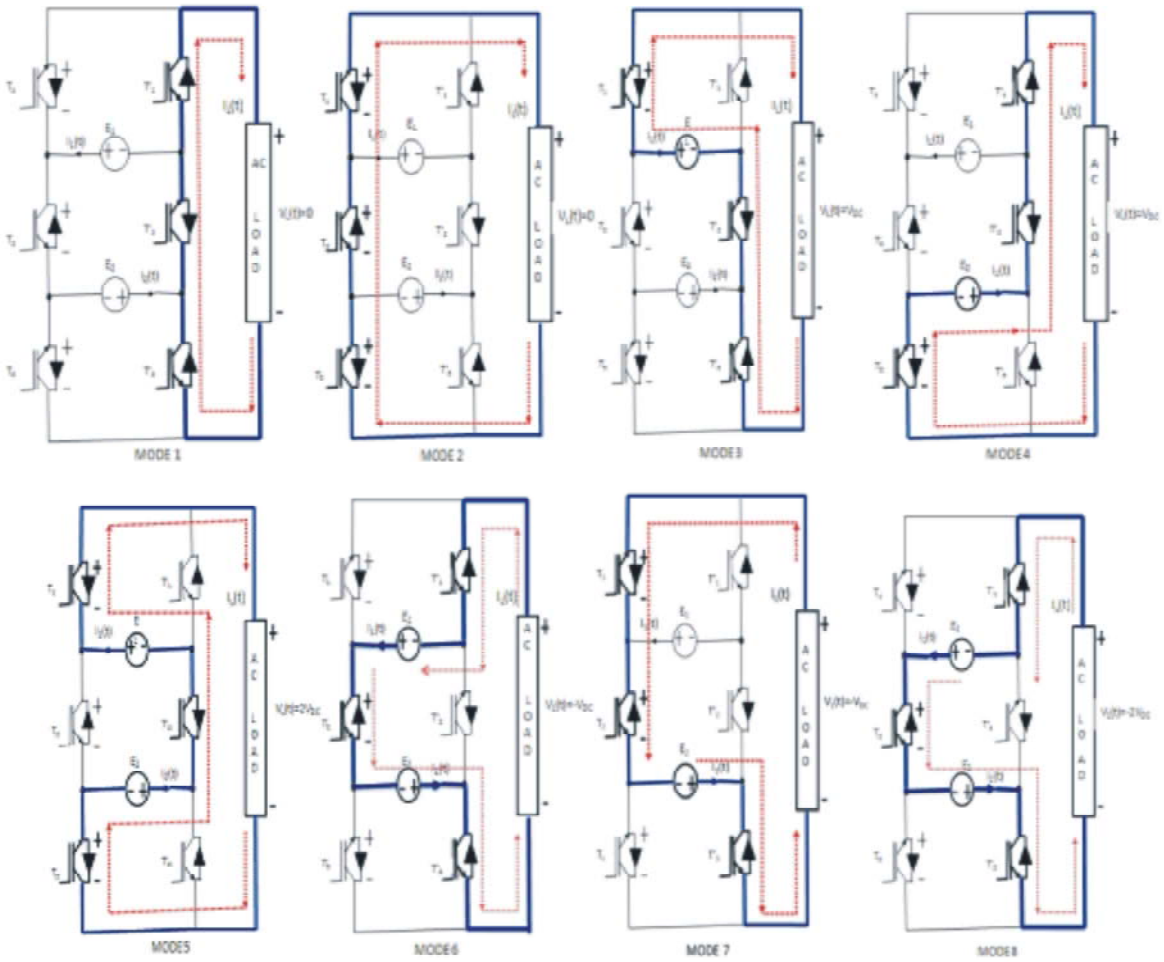

Fig. 3: Eight valid operating modes for the inverter

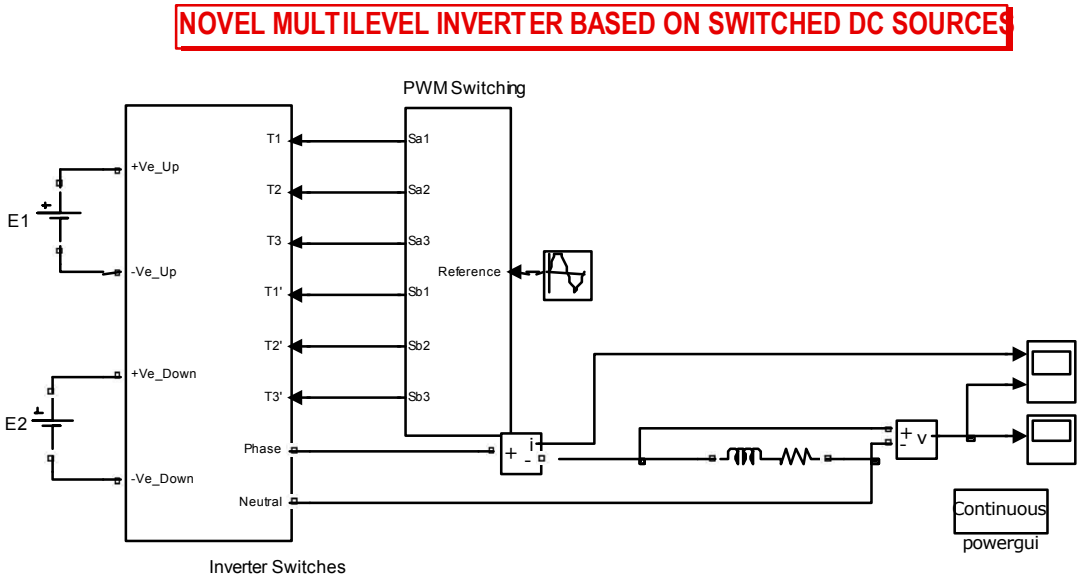

Fig. 4: Proposed control scheme for a 5 and 7-level inverter

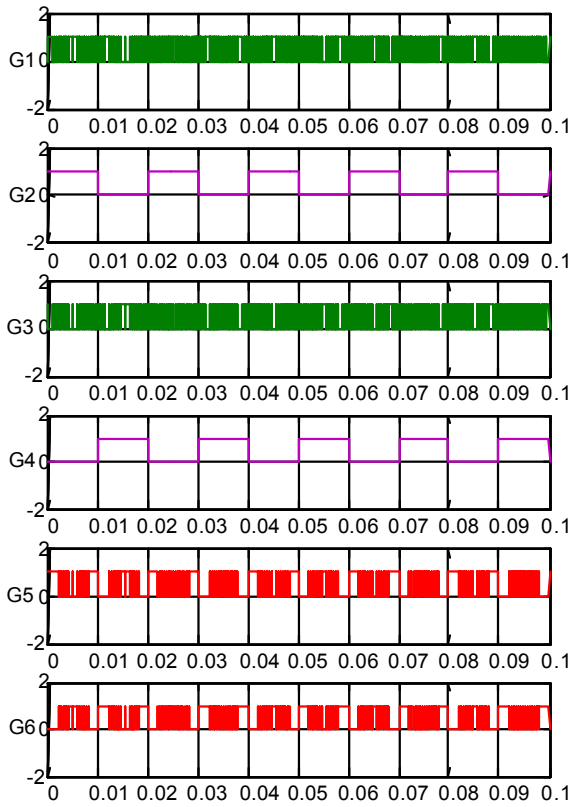

Fig. 5: Switching Strategy for the five-level inverter

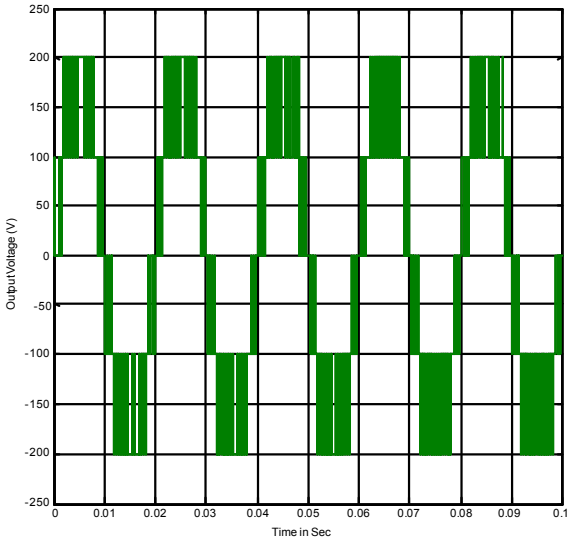

Fig. 6: Simulation results of 5-Level MLI Voltage

output, a control scheme is described where these modes are utilized. The reference signal has the frequency of 50 Hz. Carrier signals above the zeror eference and below the zero reference is designated and is shown in Fig. 5.

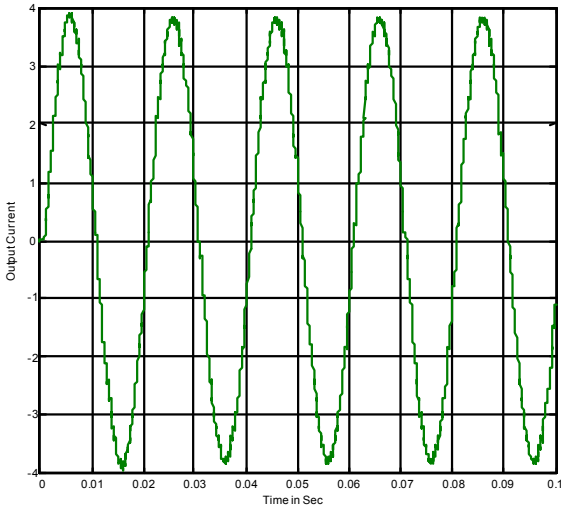

Fig. 7: Simulation results of 5-Level MLI Current

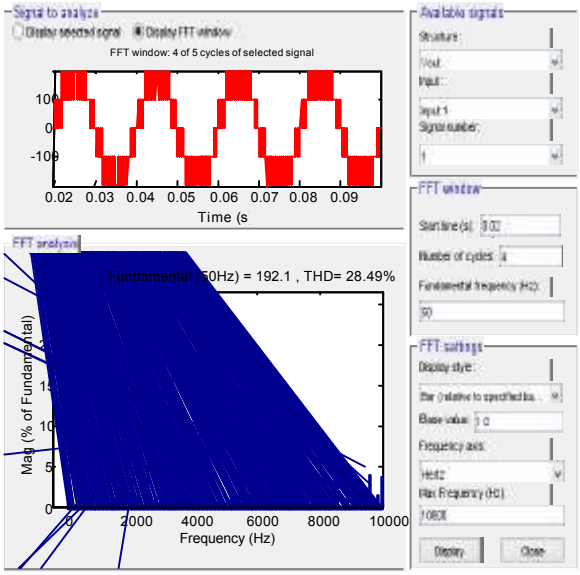

Fig. 8: Harmonic Analysis for 5-Level Output Voltage

A simulation model of a single-phase five level inverter is developed with MATLAB/Simulink tool, to examine the performance of the proposed topology and the control scheme. Two input dc sources with $E_1 = E_2 = 24$ V are used. The switching pulses so obtained are shown in Fig. 6, which shows that switches T_2 and T'_2operate at a fundamental frequency of 50 Hz while switches T_1, T'_1, T_3 and T'_3 operate at a frequencyof 1 kHz. Thus at high frequency, low-voltage-rated switches are operated and incur more switching losses and at fundamental frequency, high-voltage rated switches are operated and incur more conduction losses. Hence the total losses among

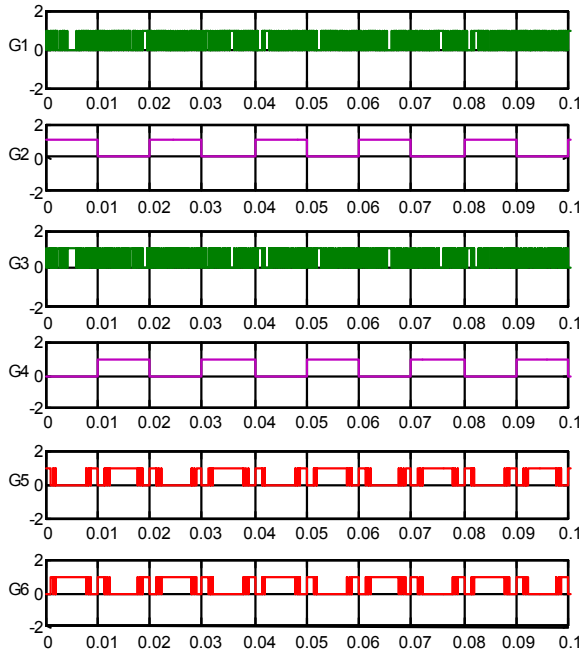

Fig. 9: Switching Strategy for the 7-level inverter

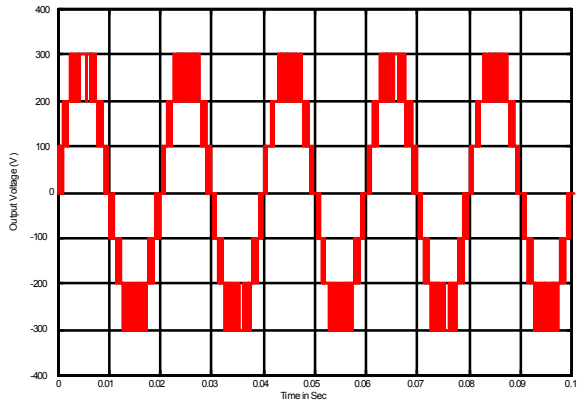

Fig. 10: Simulation results of 7-Level MLI Voltage

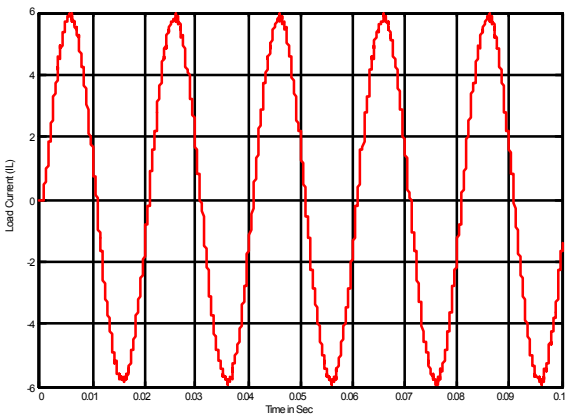

Fig. 11: Simulation results of 7-Level MLI Current

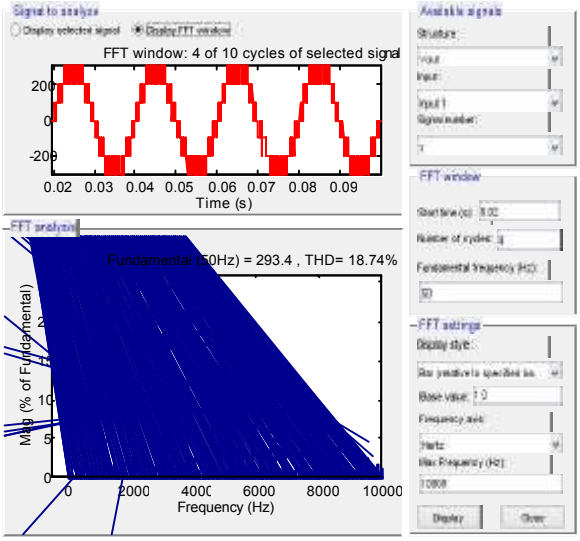

Fig. 12: Harmonic Analysis for 7-Level Output Voltage

Table 2: Comparison of 5-level and 7-level

Description	Five level	Seven level
Total harmonic distortion (THD)	28.49%	18.74%
Fundamental frequency (50 HZ)	192.1	293.4

the switches get distributed.The waveform for load voltage is shown in Fig. 6, which shows that the five-level voltage waveform has equal steps.

Then with an *R–L* load ($R = 2\ \Omega$ and $L = 2$ mH), the load current waveform is shown in Fig. 7. It is important to balance the power among input dc sources, so that all dc sources have equal lifetimes. If dc sources are renewable sources such as PV cells, then power balancing becomes crucial. In case of CHB inverter, carrier rotation scheme is employed for equal utilization of sources. Here power balancing can be achieved if sources E_1 and E_2 are utilized alternately in full cycles of the output waveform and balancing can be achieved in two cycles.

Thus power balancing among input dc sources can be ensured, by utilizing all the modes mentioned in Table 2.

Comparison: Here the proposed technology is compared with the conventional topologies. The topology is compared in terms of component requirements, switching losses and conduction losses. Most importantly the total harmonic distortion (THD) of the proposed 7-level topology is compared with the conventional 5-level topology for fundamental frequency of 50 HZ.

Also the proposed topology is compared with classical CHB topology as the proposed topology resembles CHB topology in configuration and functional features. It can be observed that the proposed topology requires significantly lesser number of power switches than the classical topologies.

CONCLUSION

The main reason for having MLIs is that they increase the output level by reducing the device counts. This proposed work also implemented to reduce the device count. In conventional 5-level topology, the two input voltages are symmetrically equal. Assuming the same specifications, the topology has been modified to asymmetrical input voltages to achieve the seven level voltages. The proposed topology significantly reduces the number of power switches and associated gate driver circuits as compared with the conventional topologies. If the dc sources available are isolated, then the proposed topology can give an effective output.

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