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Design of a Power Clock Generator Using DLL Based Pulse Combiner Circuit for Adiabatic Logic

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Abstract: The paper presents the implementation of a power clock generator for an adiabatic logic. The paper reports the detail implementation issues of power clock generator design using Phase combiner. The architectures operations and structure for adiabatic circuits are entirely different from the conventional CMOS circuits. In our work we produce a power clock of frequency greater than 1 GHz. The extended version using FinFET based architecture will be proposed in future. The simulations are carried out in HSPICE using predictive technology models in 32nm.

Key words: Adiabatic logic · Power Clock · Phase Combiner · CMOS · DLL

INTRODUCTION

In the contemporary electronic systems, reduction of energy dissipation in the circuit is one of the main challenges for the research technologies, circuits and architectures because of lower power demand. The low energy is of supreme significance in most of circuits. For example, the performance of a hand held computer is not critical, but a battery life is of foremost concern. In this judgment adiabatic computing [1] is an attractive approach. In recent years several multiphase AC power supply (the power clock) designed for low power logic families. The clock charges the node capacitance during the rise time and fall time stored energy recover for the operation of the logic circuit. The circuit capacitance associated with the time constants which are much smaller than the rise and fall time of the power clock, without energy loss almost 'adiabatically' such energy transfers occurs. The problem with the existing circuits is the requirement of two or four phase clock [2-5] with respect to standard CMOS solutions. The research in clock generators is been expanding in recent years and it's capable of providing a wide frequency bands, multiple frequency clock signals for mobile communication system, clock and data recoveries and microprocessors.

Literature Review: In literature various Power Clock Generator (PCG) architecture investigated for the adiabatic logic families are usually introduced by demonstrating the operating principle with some logic circuits. However these studies elucidate major details of DLL [6] and PLL [7, 8], because those are used in many PCG systems. Jaehyouk Choi *et al.* [9] developed a PCG for high multiplication factor based on programmable delay locked loop. The proposed clock generator has higher multiplication factor compared to other systems. In serial network-on-chip data links it's provide high speed clock up to 4 GHZ. In the charge pump, current mismatch produces the delay mismatch between the delay cells. To reduce the delay mismatch in charge pump Sewook Hwang *et al.* [10] proposed analog self calibration method and a phase detector with an auxiliary charge pump for DLL. It consists only D flip flops and inverters. Chihun Lee *et al.* [11] designed the quadruplicate harmonic-locked PD, a low-voltage Colpitts voltage-controlled oscillator and a wide-range divide-by-2 divider for clock generator. An All Digital Phase Locked Loop (ADPLL) clock generator is proposed for an asynchronous locally Synchronous (GALS) Multiprocessor Systems-On-Chip (Mpsocs) Architecture [12]. Adjusting type portable multiphase clock generator [13] has Clock phase adjusting options according to input clock frequencies. Similar work done by Behzad Mesgarzadeh and Atila Alvandpour [14] also discussed about the multiphase clock generator. The proposed clock generator is simple and robust because of their digital CMOS design. Still dynamic

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frequency scaling based clock generator is designed [15] based on DLL method. In short time the design can generate clock signals from 120 MHZ to 1.8 GHZ by varying the frequency dynamically.

Implementation Issues

Adiabatic Logic: In digital logic for reducing power dissipation several methods are available.

In a static CMOS inverter with the supply voltage V_{DD} the energy dissipation during the charging or discharging cycle is given by equation 1.

$$E_{STATIC} = \alpha \frac{1}{2} CV_{DD}^2 \tag{1}$$

where,

α is the switching probability. The main factor affecting the performance of the CMOS circuit is the leakage current due to switching. Similarly, for an adiabatic inverter circuit, the energy dissipation in the charging and recovering cycle is given by

$$E_{AL} = \varsigma \frac{RC}{T} CV_{DD}^2 \tag{2}$$

where,

R is the Resistance offered during charging through PMOS and discharging through NMOS. ς is the shaping factor if non-ramp power clock is used. But previous results in literature prove that the trapezoidal voltage waveforms achieve the best energy efficiency. T is the transition time. The energy expression of adiabatic logic shows that the dissipated energy is inversely proportional to the transition time, T.

$$\begin{aligned} &E_{AL} < E_{STATIC} \\ &2\frac{RC}{T} CV_{DD}^2 < \alpha \frac{1}{2} CV_{DD}^2 \\ &T > 4\frac{RC}{\alpha} \end{aligned} \tag{3}$$

Equation 3 provides the condition to minimize energy. From the above expression, the energy loss is inversely proportional to the transition time, T. The energy loss is less when the capacitor charges in a slower manner. Adiabatic switching is a new approach and an emerging trend which reduces the power through recycling instead of dissipation as heat. When adiabatic switching is manipulated, the stored signal energies on circuit capacitances may be recycled instead of abandoned as heat. For an energy recovery circuit, a capacitance is charged from '0' to V_{DD} or discharge from V_{DD} during energy dissipation occurs. Defined by Ideal energy dissipation at time T is given by

$$E_{diss} = I^2 RT = \left(\frac{CV_{dd}}{T} \right)^2 \text{RT} = \left(\frac{\text{RC}}{\text{T}} \right) \text{CV}_{\text{dd}}^2 \tag{4}$$

When T >> RC, the energy dissipation of the adiabatic circuit is much smaller than the Conventional Complementary Metal Oxide Semiconductor (CMOS), during the charge or discharge cycle energy of $CV^2_{DD}/2$ is required.

Implementation of a DLL Pulse Combiner: The DLL based clock generator and clock oscillators express less jitter and phase noise compared to the PLL. To overcome the difficulty of frequency multiplication, a DLL based clock generator and a local oscillator has been designed. The presented frequency multiplier increases the maximum operating frequency and enables dynamic voltage scaling and can multiply the input frequency dynamically. The presented DLL consisting of inverters and D flip flops, a high multiplication factor provided from the clock generator up to 24. Dynamic logic circuit based PFD is implemented. Compared to the static logic circuit based conventional PFD, the proposed method needs fewer transistors and less power consumption.

The overall block diagram of the Pulse combiner based DLL clock generator illustrated in the Fig. 1 and it consists of DLL, pulse generator and pulse combiner. The various blocks of the DLL are phase frequency detector, charge pump, loop filter and VCDL. The circuit can be controlled by programming. The proposed circuit is shown in Fig. 2.

In this method 0.18 um CMOS technology based programmable DLL designed with high multiplication factor. An input reference frequency range of a DLL as low as 30 MHz while sustaining small chip area and better phase noise performance.

The relative delay cell from each D flip flop generates one pulse, the VCDL a high multiplication factor acquire with the same number of delay cell. Also DFF and inverter are operating only when clocks are triggering them, so the power consumption is reduced. There is no need of the separate phase selection process required and non-essential pulses are not generated for the specific output clock. A 32 nm CMOS technology based pulse triggered flip flop, delay cell, pulse combiner and the overall proposed pulse combiner schematic view and the simulation output waveforms are illustrated in the Fig. 3 to 9.

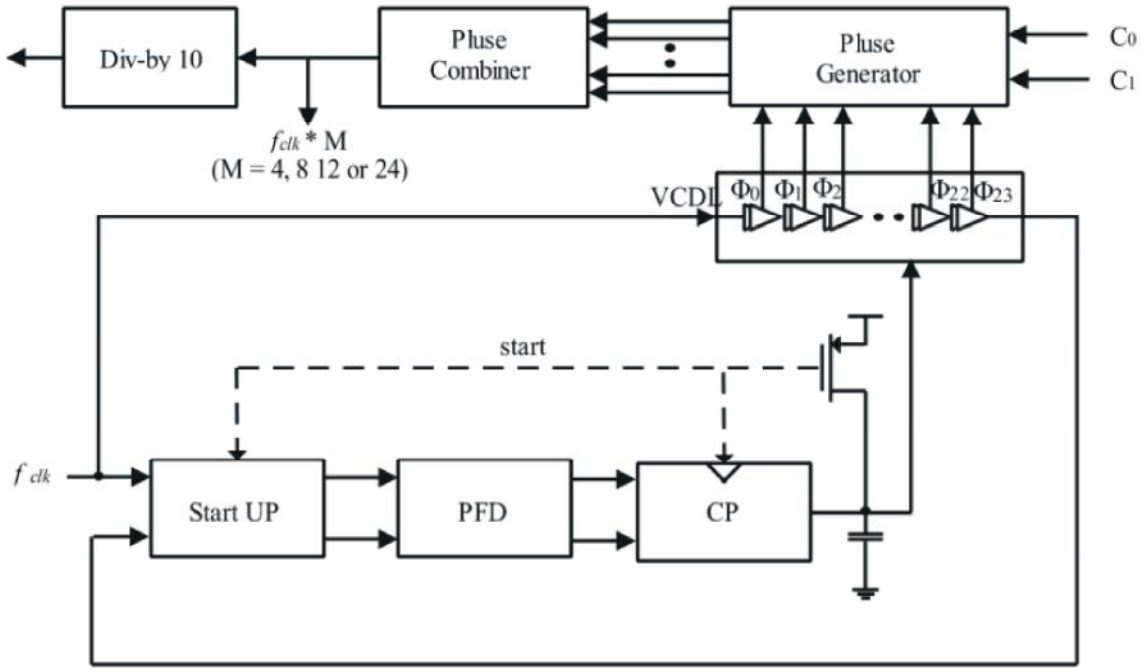

Fig. 1: Proposed DLL based clock generator

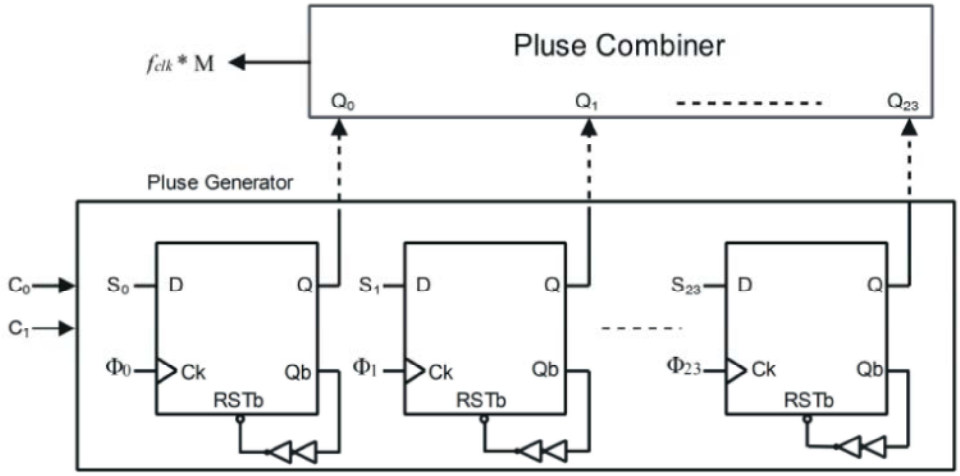

Fig. 2: Proposed pulse generator and combiner

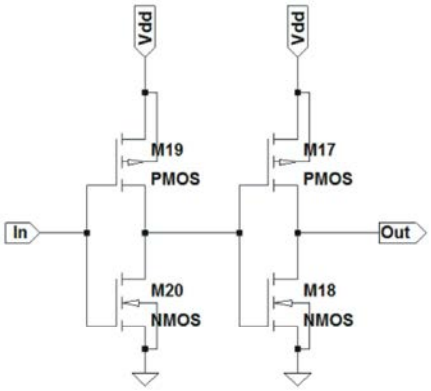

Fig. 3: Schematic view of the delay cell

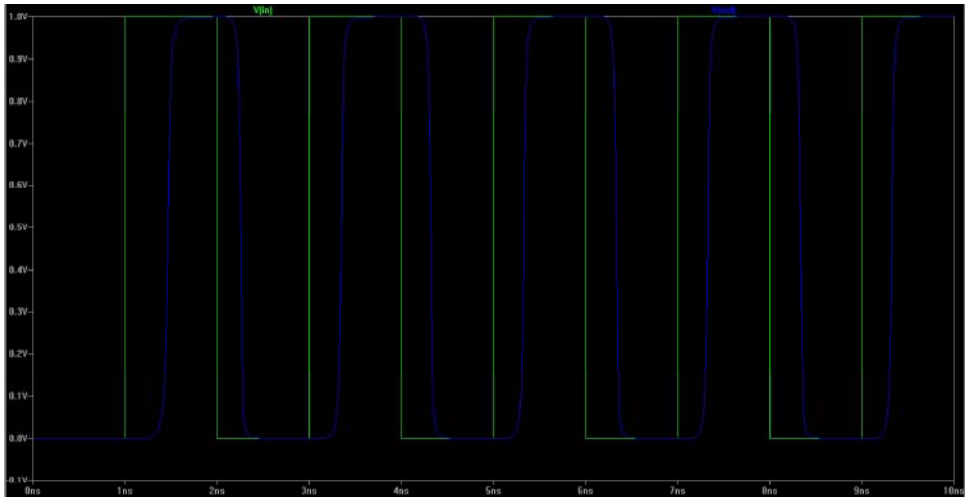

Fig. 4: Simulation output waveform of the delay cell

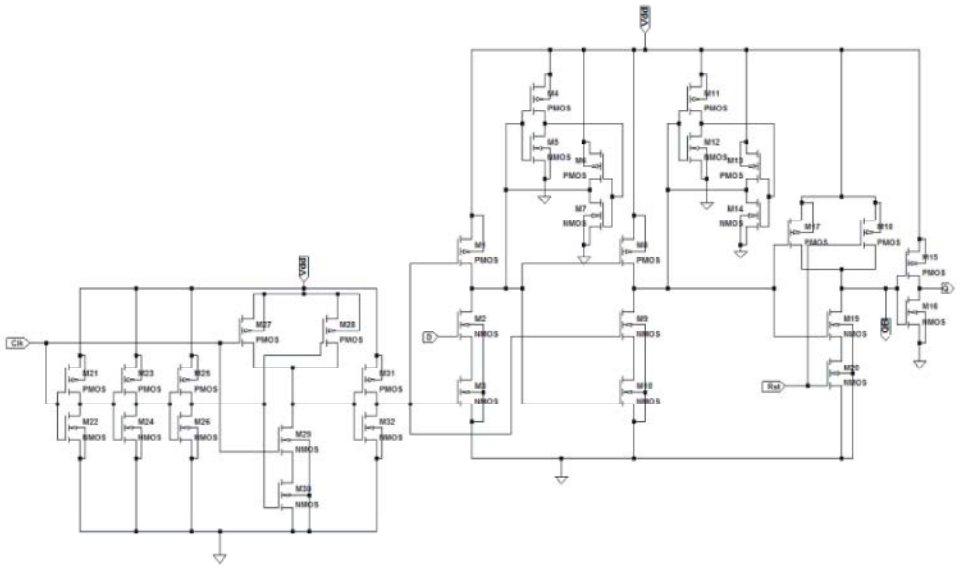

Fig. 5: Schematic view of the pulsed flip flop

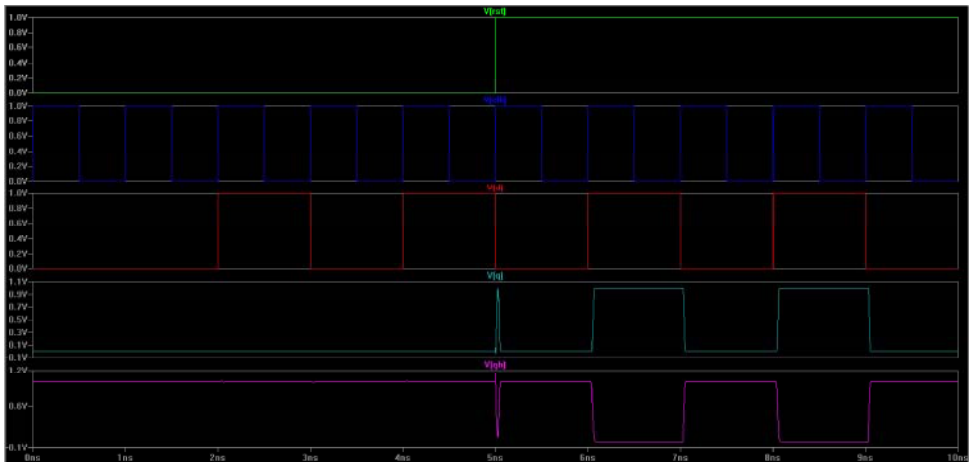

Fig. 6: Simulation output of the pulsed flip flop

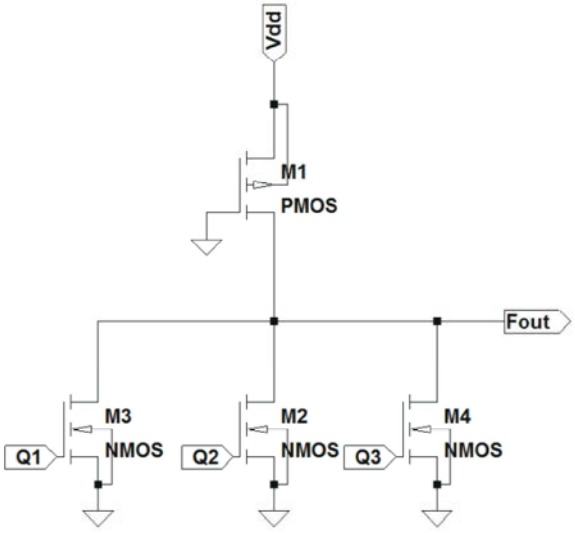

Fig. 7: Schematic view of the pulse combiner

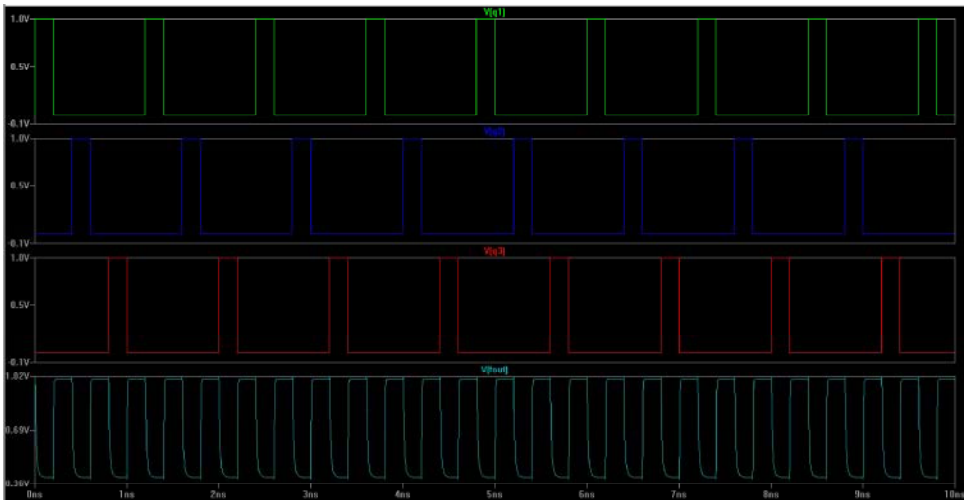

Fig. 8: Simulation output waveform of the pulse combiner

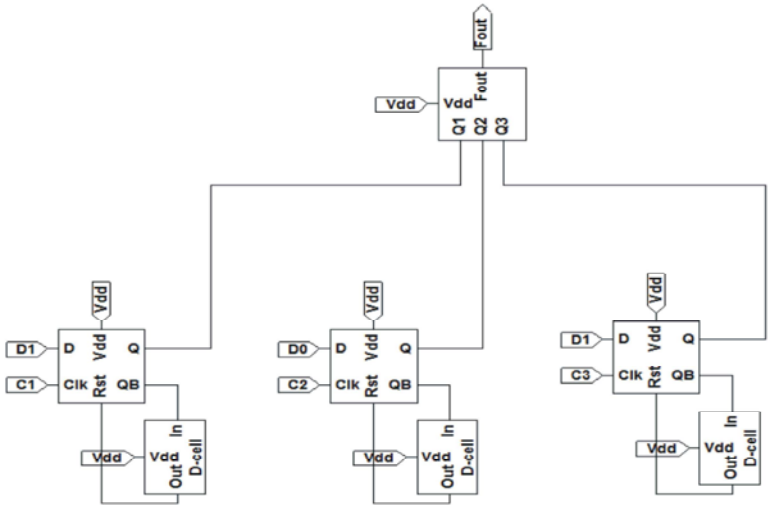

Fig. 9: Schematic view of pulse combiner and pulse generator

Table 1: HSpice Analysis VDD=1 V

S.NO	PARAMETER	VALUE
1	Average power (W)	8.0976E-02
2	Peak power (W)	1.9383E-01
3	Average current (A)	8.1017E-02
4	Peak current (A)	1.6987E-03

LTSpice power dissipation value = 835.14 uW

The simulation results are shown in Figure 3 to 9 and the results are tabulated in Table 1. The power supply voltage used was 1V and the frequency of operation for the adiabatic logic is 1GHz. The various parameters shows that the proposed combiner is efficient in the performance.

CONCLUSION

The implementation of a power clock generator for a proposed adiabatic logic using Complementary Energy Path Adiabatic Logic (CEPAL) is presented. The implementation issues of power clock generator using Phase combiner is elaborated with detailed analysis. The architectures operations and structure for adiabatic circuits are entirely different from the conventional CMOS circuits. In future the work will be extended to using FinFET based architecture. The simulations are carried out in HSPICE using predictive technology models in 32nm.

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