

Single Phase Asymmetrical Cascaded Multi Level Inverter with Reduced Number of Switches

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Abstract: In this paper mainly focused on the design and implementation of new topology in a single phase 11 level asymmetrical multilevel inverter by using only a 14 switches and five equal DC power source. The main objective of this paper is to reduce the complexity while increasing the output step levels with a low number of switches and sources at fixed frequency. The multilevel voltage source inverters unique structure allows them to obtain high voltages with reduced switches without the use of transformers. The general function of the multilevel inverter is to provide a required AC output voltage from several levels of dc input voltage for these reason multilevel inverters can easily used for the high power applications. In this paper, Single phase 11-level inverter for better accuracy with reduced number of switches and unequal dc input sources. The proposed system used the topology of Asymmetrical cascade H-Bridge Multilevel inverter with separate unequal dc sources for the switching circuit. As the number of step level and voltage increases in the output waveform has more steps, which produces a desired output waveform with low harmonic distortion. Application of multilevel inverter for high power equipments in industry has become popular because of its high-quality output waveform.

Key words: Asymmetrical cascaded H-bridge inverters • Switch Reduction • Total Harmonic Distortion • 11-Level inverters

INTRODUCTION

Now-a-days, in industries, power conversion systems become very popular and are used extensively. The power conversion system includes AC-DC, DC-AC, DC-DC, AC-AC conversions. Many high and medium voltage applications require such power conversion systems. Those applications are HVDC transmission, FACTS, AC/DC drives, renewable energy sources such as PV solar cells, wind, fuel cells etc. This paper concentrates on DC-AC conversion (Inverter action). A conventional single phase inverter is able to produce voltage levels of +V_{dc}, 0, -V_{dc}, so the output waveform of the inverter is quasi-square wave, which is not advisable to use as an input to any AC system. Hence, to get nearly sinusoidal waveform, multilevel inverter is introduced in 1975. The output of multilevel inverter is a staircase wave, which is nearly sinusoidal. By increasing the number of output voltage levels in multilevel inverter the THD can be minimized. Also ripple content in the output of multilevel

inverter is lesser than that of conventional inverter. One more advantage that MLI possesses over the conventional inverter is voltage stress across the individual switch is lesser in case of MLI. Many topologies of MLI are developed and studied. They are generally classified into [1-9]:

- Flying-capacitor inverter
- Diode-clamped inverter
- Cascaded H-bridge inverter

From these inverter topologies cascaded H-Bridge multilevel inverter is widely used. Cascaded inverter has 'n' number of series connected cells, with an individual DC voltage source connected to each cell. There are two groups of cascade multilevel converters, the symmetric and the asymmetric multilevel converters. In symmetric MLI all the DC voltage sources used are of equal magnitude, whereas in asymmetric MLI magnitudes of DC voltage sources are unequal.

In the asymmetric topologies, the values of DC voltage sources magnitudes are unequal. By giving proper switching sequence to the gate driver circuits, desired number of output voltage levels can be obtained. So the number of power electronic components required, will be reduced as compared to that of MLI with symmetrical DC voltage sources. One of the advantages of asymmetrical MLI is that with the same number of switches and DC voltage sources, the number of output voltage level obtained is more, when compared to the symmetrical topology.

This paper proposes new asymmetric topology for 11-level voltage output with reduced number of switches. The proposed topology has been also analyzed without using any PWM technique. But after using SPWM techniques THD of the output can be reduced further. The hardware is designed using SPWM technique and compared the result among inverter circuits, to figure out the technique which gives least THD.

Previous Research: Numerous related research works are already existed in literature which based on multilevel converter of the system. Some of them are reviewed here.

Mohamad Fathi *et al.* [10] presented the concept of an asymmetrical cascaded multilevel inverter based on a five-level transistor-clamped H-bridge power cell. A two-cell configuration with a dc link voltage ratio of 4: 1 is presented. The modulation method is based on the fundamental frequency switching. An analysis of the inverter output voltage and harmonics is presented. Injection of the third harmonic voltage as to maximize the output voltage and the issue of the inverse power flow or regeneration in the low-voltage cell are presented. The prototype of the proposed inverter was built and its functionality was verified through experimental results.

Vincent Roberge *et al.* [11] implemented Genetic algorithm based Multilevel inverters to improve the high power inverters due to their high-voltage operation, high efficiency, low switching losses and low electromagnetic interference. A parallel implementation of the GA on graphical processing unit is proposed in order to accelerate the computation of the optimal switching angles for multilevel inverters with varying dc sources. GA is used to ignore solving the equation associated with the highest order harmonics. A reduction in the eliminated harmonics results in an increase in the degrees of freedom. As a result, the lower order harmonics are eliminated in more operating points. A 9-level inverter is chosen as a case study. The genetic algorithm (GA) for optimization purposes is used.

Pedram Sotoodeh *et al.* [12] presented the capability of a new single-phase wind energy inverter with flexible AC transmission system. The proposed inverter is able to regulate active and reactive power transferred to the grid and which is placed between the wind turbine and the grid. Power factor can be controlled by using this inverter because of this inverter is equipped with distribution static synchronous compensator. The main objective of this his paper is to introduce new ways to increase the growth of renewable energy systems into the distribution systems. This will encourage the utilities and customers to use interactive supply of energy. Moreover, by using these types of converters will significantly reduce the total cost of the renewable energy application. In this paper, modular multilevel converter is used as the desired topology to meet all the requirements of a single-phase system such as compatibility with IEEE standards, total harmonic distortion (THD), efficiency and total cost of the system. This paper was implemented using 11- level inverter then the simulations have been done in MATLAB/Simulink.

Bindeshwar Singh *et al.* [13] have presented the concept of decreased harmonic distortion in the output waveform without decreasing the inverter power output using 11-level inverter. The proposed multilevel inverters have been attracting the industry in the recent decade for high-power and medium-voltage energy control. This paper presents the most important topologies like diode-clamped inverter (neutral- point clamped), capacitor-clamped (flying capacitor) and cascaded multilevel with separate dc sources. This paper also presents the most relevant modulation methods developed for this family of converters: multilevel sinusoidal pulse width modulation, multilevel selective harmonic elimination and space-vector modulation. Authors strongly believe that this survey article will be very much useful to the researchers for finding out the relevant references in the field of topologies and modulation strategies of multilevel inverter.

Zhong Du *et al.* [14] implemented cascaded H-bridge multilevel inverter using only a single dc power source and capacitors. Generally, The Standard cascaded multilevel inverters require n dc sources for $2n + 1$ level. Without requiring transformers, the scheme proposed here allows the use of a single dc power source with the remaining $n- 1$ dc sources being capacitors, which is referred to as hybrid cascaded H-bridge multilevel inverter (HCMLI) in this paper. The proposed inverter can simultaneously maintain the dc voltage level of the capacitors and choose a fundamental frequency switching

pattern to produce a nearly sinusoidal output. HCMLI using only a single dc source for each phase is promising for high-power motor drive applications as it significantly decreases the number of required dc power supplies, provides high-quality output power due to its high number of output levels and results in high conversion efficiency and low thermal stress as it uses a fundamental frequency switching scheme. This paper was implemented for 7-level HCMLI with fundamental frequency switching control and how its modulation index range can be extended using triple harmonic compensation.

D. Kalyanakumar *et al.* [15] investigated Hybrid 7-Level H-bridge Inverter was used in a Distribution Static Compensator (DSTATCOM) in Power System industry, so that the proposed system benefits of low harmonics distortion with reduced number of switches to achieve the output over the conventional cascaded 7-level inverter and reduced switching losses. The proposed system is used to obtain the improved power factor, compensate the reactive power and suppress the total harmonics distortion (THD) drawn from a Non-Liner Diode Rectifier Load (NLDRL) of DSTATCOM, by using Sub-Harmonics Pulse Width Modulation (SHPWM) technique is used as control for the switches of HSL H-bridge Inverter. The proposed hybrid seven levels H-bridge implemented using MatLab/Simulink simulation software for shunt compensation of a 4.5 kV distribution system.

Proposed Approach: The proposed structure of the Asymmetrical cascaded H-Bridge 11-Level inverter is shown in Figure 1. An asymmetrical multilevel inverter can be defined as a multilevel converter fed by a set of DC voltage source where at least one of them is different to the other one. The main advantage of asymmetrical multi level converter is, it uses less number of semiconductor switches compared with symmetrical topology. One interest of the asymmetrical configurations is that the number of levels is higher with the same number of cells. The number of levels is higher with the same number of cells in the symmetrical case, whereas it grows exponentially, in the asymmetrical case, the asymmetrical topology requires only 14 switches to obtain 11 level output voltage. Whereas in case of symmetrical topology 28 switches are needed.

This proposed inverter consists of an H Bridge circuit with 14 switching devices, five equal dc sources and SPWM generation unit. The equal DC voltage sources of 50V are connected with MOSFET switches to provide the required output voltage with low distortion for eleven Level. Only one H-bridge is connected with all the switches to acquire both positive and negative polarity. Time based pulse generation circuit is designed with the above inverter switches for eleven level output [16-18].

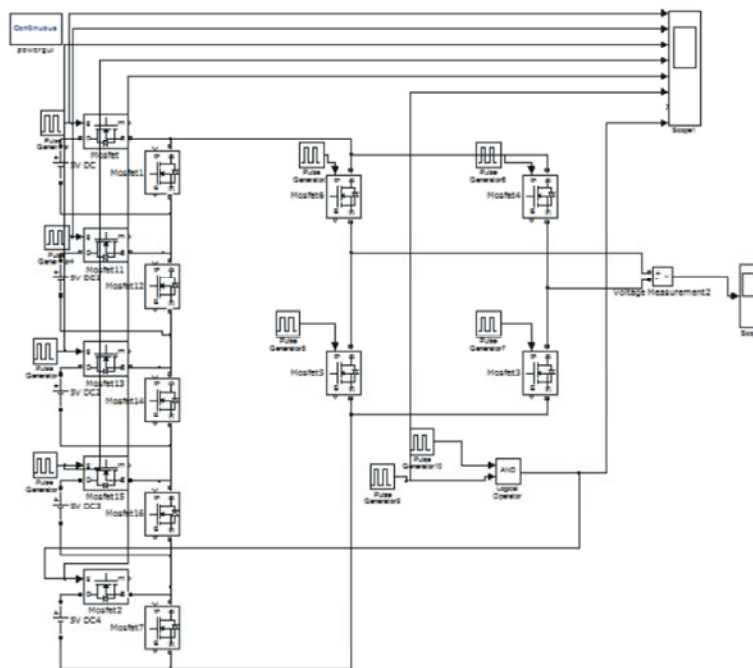


Fig. 1: Asymmetric cascaded H-Bridge inverter for 11 level with reduced switches

For each full bridge inverter the output voltage is given by

$$V_{oi} = V_{dc} (S_{1i} + S_{2i}) \quad (1)$$

And the input dc current is

$$I_{dci} = I_m (S_{1i} + S_{2i}) \quad (2)$$

where,

- $i=1 \dots 5$ (number of full bridge inverters employed) for the 11 level type.
- I_m is the output current of the cascaded inverter.
- S_{1i} and S_{2i} is the upper switch of each full bridge inverter.

Now the output voltage of each phase of the multilevel cascaded inverter is given by:

$$V_{out} = V_{in} \times S_i \quad i=1, 2, \dots, n \quad (3)$$

In multilevel inverters, the amplitude modulation index (m_a) is the ratio of reference amplitude (a_m) to carrier amplitude (a_c).

$$m_a = A_m / (m-1) A_c \quad (4)$$

The frequency ratio (m_f) is ratio of carrier frequency (f_c) to reference frequency (f_m).

$$m_f = f_c / f_m \quad (5)$$

Pulse Width Modulation: Mainly the power electronic converters are operated in the “switched mode”. This means the switches within the converter are always in either one of the two states - turned off or turned on. Any operation in the linear region, other than for the unavoidable transition from conducting to non-conducting, incurs an undesirable loss of efficiency and an unbearable rise in switch power dissipation. To control the flow of power in the converter, the switches alternate between these two states. This happens rapidly enough that the inductors and capacitors at the input and output nodes of the converter average or filter the switched signal. The switched component is attenuated and the desired dc or low frequency ac component is retained. This process is called Pulse Width Modulation, since the desired average value is controlled by modulating the width of the pulses.

For maximum attenuation of the switching component, the switch frequency f_c should be high many times the frequency of the desired fundamental ac component f_l seen at the input or output terminals. In large converters, this is in conflict with an upper limit placed on switch frequency by switching losses. For POWER MOSFET converters, the ratio of switch frequency to fundamental frequency f_c/f_l may be as low as unity, which is known as square wave switching. Another application where the pulse number may be low is in converters which are better described as amplifiers, whose upper output fundamental frequency may be relatively high. These high power switch-mode amplifiers find application in active power filtering, test signal generation, servo and audio amplifiers. These low pulse numbers place the greatest demands on effective modulation to reduce the distortion as much as possible. The low pulse numbers place the greatest demands on effective modulation to reduce the distortion as much as possible.

In general, the modulation index, M of proposed inverter is defined as

$$M = V_{ref} / V_m \quad (5)$$

where V_m is the total dc link voltage per phase for H bridge cells and V_{ref} is the voltage reference

$$V_m = \sum_{n=1}^N V_{dc,n} \quad (6)$$

$$V_{ref} \in [0, V_m]$$

RESULTS AND DISCUSSIONS

In this thesis, new modified single phase 11 level H-Bridge inverter will be focused. Multilevel, i.e., positive, negative and zero level waveform are synthesized using such an inverter. In the thesis, the total harmonic distortion (THD) methods are used to indicate of the quantity of harmonics contents in the output waveforms. To reduce the THD in the output voltage, the lowest $s-1$ harmonics in each phase voltage need to be eliminated, where s is the number of the full-bridge inverter per phase.

The Figure 3 shown below is the simulink model of the new modified H Bridge 11-Level level inverter using power system block set. The following parameter values are used for simulation: dc inputs of 5V, 14 MOSFET switches and time based pulse generation unit.



Fig. 2: Simulation results of proposed system 11- Level inverter for Voltage with respect to time

Table 1: Comparison of parameter values

	Proposed method Parameters using 11 Level
THD	3.36%
Output voltage	$\pm 250V$
Frequency	50Hz
Number of switches	14
Number of sources	5

Table 2: System Parameters

Dc link voltage, $v_{dc,1}$	60V
Dc link voltage, $v_{dc,2}$	240V
IGBT	IRG4PH%)UDPBF, 24A, 1200V
Capacitor	3400uF, 200V
Diode	30CPF12PBF, 30A, 1200V
Braking resistor	40 Ohms
Voltage regular switching frequency	10 kHz
Induction motor	1 kW, 415V, 50Hz

In this proposed system of an simulation result is the output voltage, output current and step level will be displayed with repect to time. The maximum step level of 11-Level displayed. and the voltage level for various steps displayed. The output voltage per steps with the time will be displayed. The range of voltage is upto $\pm 250V$ can be delivered. Simulations are done for various values of modulation index and the corresponding THD% are observed using FFT block and listed in Table 1.

Experimental Results and Discussion: To validate the proposed topology and theory, hardware of the 11 level new modified H-bridge multilevel inverter has been built using the MOSFET as the switching devices. DC source

voltage is getting by using diode rectifier circuit which is placed in front of the inverter circuit. Five equal DC source voltages are applied which is equal to 5 volts. Hence finally the output AC voltage for each phase is equal to 250 volts. The MOSFET driver ICs are employed to drive the MOSFET switches. The MOSFETs are switched ON and OFF by using the PWM pulses which are generated by using the microcontroller called PIC microcontroller algorithm for the switching is written in the high level language and then it is embedded in the PIC microcontroller. The output terminal of the inverter is connected to single phase induction motor. The experimental results are exposed in the Figures 6 and 7. The output of the eleven level inverter is 250 volts with frequency of 50Hz.

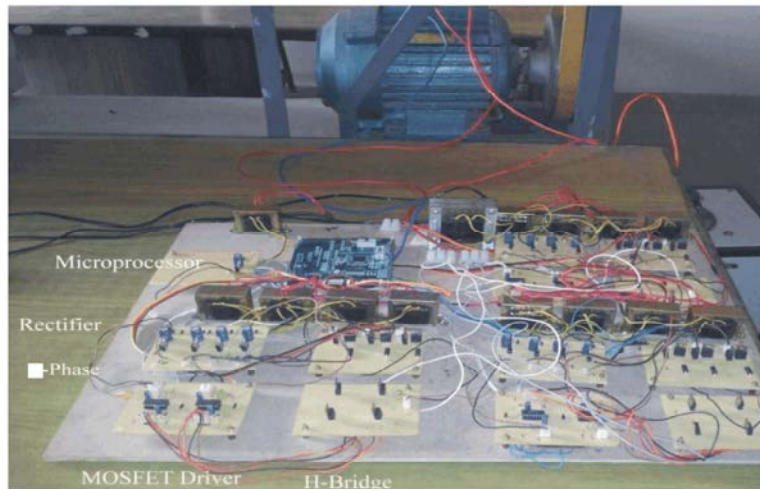


Fig. 3: Hardware Setup

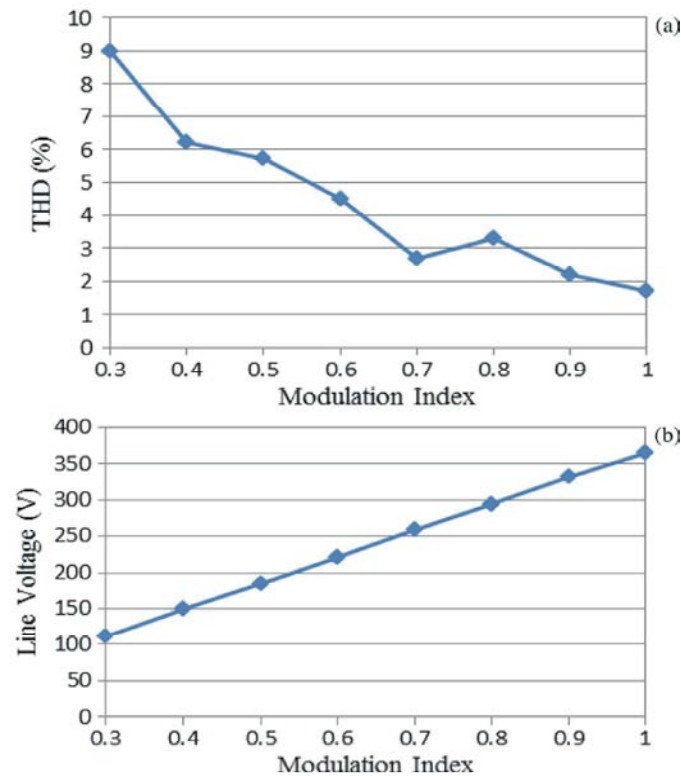


Fig. 4: (a) The total harmonic distortion and (b) the RMS line voltage of the proposed inverter versus the modulation index

The experimental setup is shown in Fig. 3 and the detailed system parameters are given in Table 2.

By using the power quality analyser equipment the THD value for the output voltage of the inverter is measured. The measured values and the simulation results are coordinates with each other. The value of THD is found to be 3 with the modulation index of 1.

The experiment results are showing that this topology is well suited are the industrial applications. The total harmonic distortion, THD of the line voltage measured using proposed Power Analyzer at different modulation indexes are plotted in Fig. 4(a). The RMS line voltage plotted against the modulation indexes is shown in Fig. 4 (b).

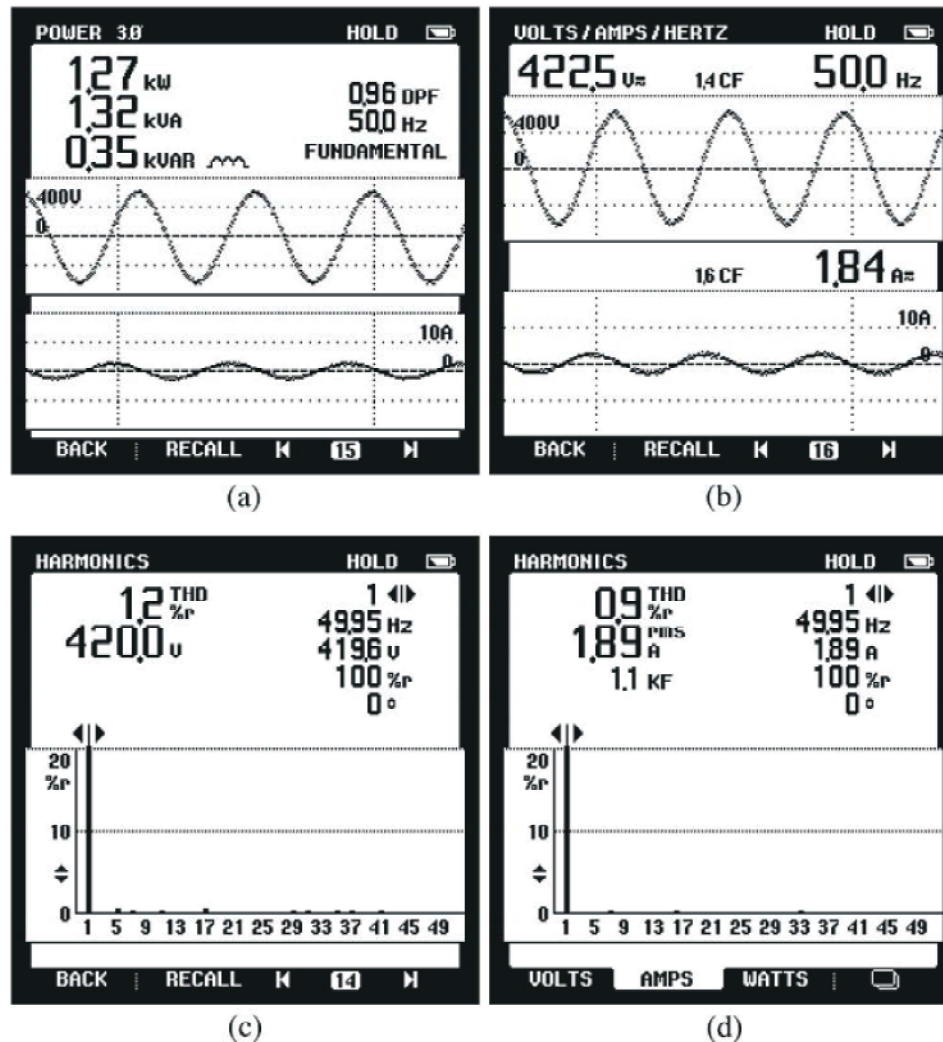


Fig. 5: Measured (a) output power. (b) RMS line voltage and current. (c) THD of line voltage. (d) THD of line current, for the extended modulation index, $M = 1.15$

The measured power, line voltage and load current are 1.27 kW, 422.5 V and 1.84 A, respectively and are shown in Fig. 5(a) and (b). The measured THD for the line voltage, 1.2% and the load current, 0.9% are shown in Fig. 6(c) and (d), respectively.

CONCLUSION

Prototype of the 11-level single-phase multilevel inverter consists of H-bridge inverters that it uses separate dc power sources. The control signals for power electronic switches are by using pulse width modulation technique. In this paper both simulation results and hardware prototype model results are correlated. Harmonic analysis carried out using Mat Lab 13.0 version software. It is proved that proposed work of Single phase

11 level multilevel inverter output voltage total harmonics distortion is reduced and improve the efficiency of system compare with previous topologies of single phase nine level multilevel cascade inverter. It is also proved that low total harmonics distortion in proposed technique.

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