Middle-East Journal of Scientific Research 20 (2): 214-217, 2014
ISSN 1990-9233

DOI: 10.5829/idosi.mejsr.2014.20.02.11330

Design of Multiplexer Using Tolerant Keeper Techniue by Reduceing the Leakage Current of the Transistor

S. Rajeswari.

Department of ECE,
Bharath University, Chennai, India

Abstract: The dynamic gates have been excellent choice in the design of modern processor, but limitations of dynamic gates includes low noise margin and leakage current, hence keeper techniques are used to overcome these limitations, but that traditional keepers are susceptible to process variation, hence the tolerant keeper architecture overcomes the leakage current by using keeper technique and if it is affected by threshold variation means, noise margin also affected, hence this keeper is replaced by an ideal keeper, that is an current source which supplies minimum required current to maintain the noise margin. in this proposed paper this current source is spilited into 3 parts namely, control circuitry process variation sensor, variation coupled keeper, here the process variation sensor and the variation coupled keeper act as a current sources and this keeper with OR gate is used for the design of multiplexer, the delay value for the proposed multiplexer is compared with the design of multiplexer with traditional keepers and the comparison table shows that delay of multiplexer is reduced from 3.10ns to 2.91 ns and leakage current is reduced from to for a single transistor.

Key words: Dynamic OR gate · Tolerant keeper · Leakage current · MOS transistor · Multiplexer · Processors

INTRODUCTION

Leakage Current Mechanisms: Definition of leakage current: The current, which flows through the conducting device to the ground even though the device in OFF condition.

This paper explores the leakage mechanisms contributing the off-state current (not just the current from the drain terminal). Other leakage mechanisms are applicable for the small geometries themselves. As the drain voltage increases, the drain to channel depletion region widens, resulting in a significant increase in off state leakage current.

We describe six short-channel leakage mechanisms as illustrated in Fig. 1. I_1 is the reverse-bias pn junction leakage; I_2 is the sub threshold leakage; I_3 is the oxide tunnelling current; I_4 is the gate current due to hot-carrier injection; I_5 is the GIDL; I_6 is the channel punch through current. The currents, I_2, I_5 and I_6 are off-state leakage mechanisms, while the current I_1 and I_3 occurs in both ON and OFF states and I_4 occurs in the off state (more typically occurs during the transistor bias states in transition).

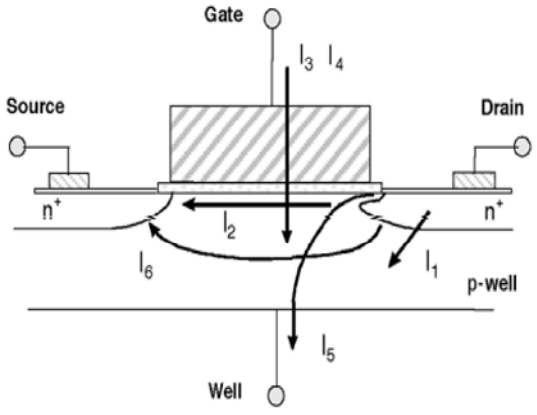


Fig. 1: Leakage current in MOS transistor

Prior Work: This part has two categories: first one decreases the leakage current through reengineering of pull down network, second one is design of innovative keeper circuits. The design of innovative keeper circuits includes the following literatures..

This is a fixed keeper (Fig. 2), where the p-MOS keeper is introduced in the dynamic OR gate to reduce the leakage current.

Corresponding Author: S. Rajeswari, Department of ECE, Bharath University, Chennai, India.

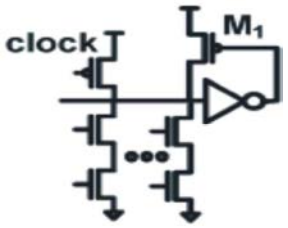


Fig. 2: Fixed Keeper

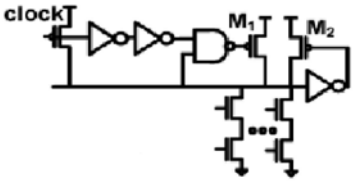


Fig. 3: Conditional Keeper

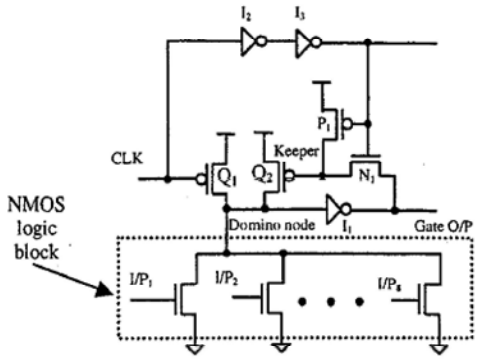


Fig. 4: High Speed Domino Keeper

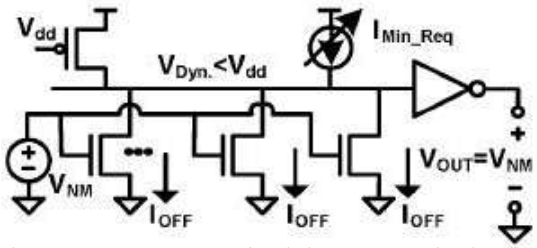


Fig. 5: Measurement of Minimum Required Current for Noise Margin in Vth Variation

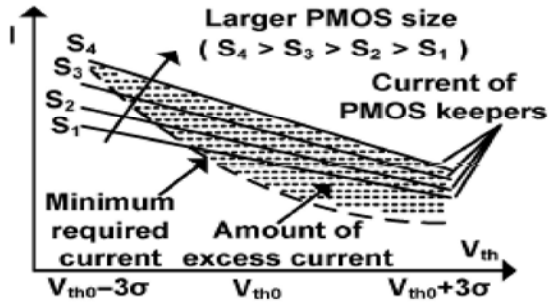


Fig. 6: Minimum Required Current (Broken Line Shows), Current of Traditional Keeper (Solid Line)

In this conditional keeper Fig. 3, the keeper circuit [1] is split into two parts so that during evaluation phase, first part is always ON and the second component turns ON after a delay. Delay is used to decrease the amount of contentions between keeper and pull-down network. The drawback of this approach is that the keeper is significantly weak during the transition of pre-charge /evaluation clock signal.

In this high speed domino keeper (Fig. 4), the keeper circuit [2] is composed of only one p-MOS transistor, which remains OFF during the early part of evaluation phase and only turns ON if the dynamic node is supposed to remain high for rest of the period depending on the input pattern. Here noise margin is low only at the begin of the evaluation period.

Proposed Keeper Circuit

Keeper Sizing for Dynamic or Gates

Definition of Noise Margin: There are several metrics have been proposed to improve the noise margin of the dynamic gate [2]. Here, we considering unity gain noise margin (UNG). UNG [3] is defined as the input voltage which if applied to the input of all dynamic node results in the signal of same amplitude at the output node. In Fig 9, voltage source of V_{NM} is applied to all MOS transistors in the pull down network and current source supplies enough current to the dynamic node so that voltage of the output nodes (V_{OUT}) is equal to V_{NM}. In this configuration, for a given threshold voltage of transistor, amplitude of current source Imin-Req is called *minimum required current for* UNG it is equal to $V_{NM.}$

In the presence of Vth variation, leakage current drawn out of the dynamic nodes has large deviation, so minimum required current must be supplied by an ideal keeper to maintain UNG. For particular noise margin (UNG), threshold voltage of transistors varied over large range and minimum required current is measured. Minimum required current sketch is shown in fig6, here vertical axis shows current and horizontal axis shows threshold voltage variation.

The broken line in the Fig 6 displays minimum required current to sustain a constant UNG over threshold voltage range from Vth0-3ó to Vth0+3ó.Alternatively,the solid lines represent the drive current of traditional PMOS keepers, which shows linear behavior with respect to threshold voltage variation. Hashed area in Fig. 10 corresponds to the excess amount of current injected into the dynamic node this can be reduced with the proper design of keeper transistor.

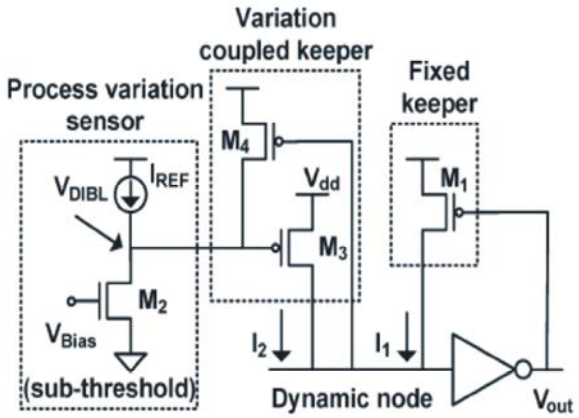


Fig. 7: Proposed Keeper Architecture

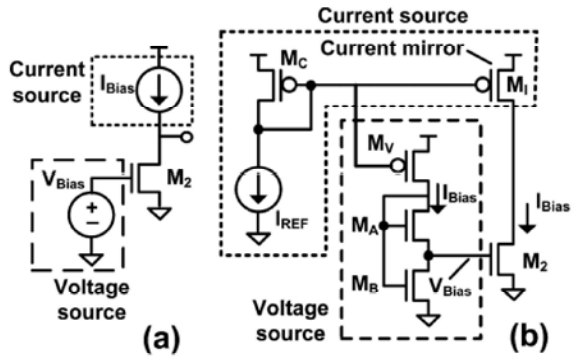


Fig. 10: (a) Schematic Sensor block Diagram (b) Transistor Level Diagram of Sensor

To meet the minimum current criteria over Vth variation range, PMOS keeper should be enlarged, only top solid line satisfies the requirement. Minimum required current curve, which presents behavior of an ideal keeper, is our reference to evaluate the efficiency of other keeper circuits under process variation. It is very difficult to design a keeper which provides exact minimum required current over entire threshold voltage variation, so it is desirable to propose a circuitry that does not provide many variations.

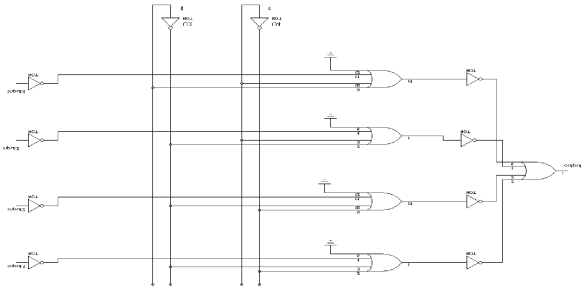
This proposed architecture has three major modules [4]: 1) Fixed keeper 2) Variation coupled keeper 3) Process variation sensor. Fixed keeper is a conventional keeper and the output of process variation sensor is coupled to fixed keeper using variation coupled keeper. The process variation sensor used in this paper based on DIBL (Drain Induced Barrier Lowering)[3] effect, it observed that for short channel devices, threshold voltage is modulated by drain voltage, assuming all other parameters to be constant, the threshold voltage becomes linearly depends on drain voltage that is sensitive to process variation.

Process variation insensitive circuitry is proposed in Fig 7, which is the tolerant keeper and it is used in our keeper circuit the reference current and voltage generated by bias circuitry are only function of the thermal voltage and width of the transistor and hence, they are effectively independent of channel length variations.

The sensor circuit in Fig 10 (a), which is composed of transistor M2 and current and voltage sources, the bias current (I_{Bias}) is generated using a current source (I_{REF}) and a current mirror, which consist of MI and MC. Since both these devices have identical gate-to-source voltages, the current of M2 is equal to $I_{Bias}=I_{REF}\times[(W/L)M1/(W/L)MC]$. The bias voltage is implemented using transistors M_V and M_B and M_C. Here M_V, M_B, M_C form a current mirror, where with proper sizing of devices, the bias current of M_A and M_B set to be I_{Bias}. It can be easily shown that if M_A and M_B are both biased in sub threshold region, VBias is independent of I_{Bias} value and it is equal to $[n(kT/q)\times(WA/WB)]$,where W_A and W_B are widths of M_A and M_B, respectively. Operation of bias circuitry is a function of fixed parameters $[(kT/q)\times(WA/WB)]$ and it is insensitive to fluctuations induced by noise or process variation so leakage current is reduced.

Design of Multiplexer Using Proposed Keeper: A **multiplexer** (or **MUX**) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of 2^n inputs has n select lines, which are used to select which input line to send to the output. Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. A multiplexer is also called a **data selector**.

Larger multiplexers are also common and, as stated above, require $[\log_2(n)]$ selector pins for *n* inputs. Other common sizes are 4-to-1, 8-to-1 and 16-to-1. Since digital logic uses binary values, powers of 2 are used (4, 8, 16) to maximally control a number of inputs for the given number of selector inputs.



Logic diagram of 4-to-1 multiplexer using OR gate and inverter

Table 1: Truth Table for Multiplexer

INPUT 1 (B)	INPUT2 (C)	OUTPUT
0	0	INPUT1
0	1	INPUT2
1	0	INPUT3
1	1	INPUT4
Output= (INPUT1+B+C) +(INPUT4+B+C)	+(INPUT2+B+C)	+(INPUT3+B+C)

Table 2: Comparison of Leakage Current

Keeper logic	Input (v)	Output (v)	Leakage current input'0'(A)
4 Input Dynamic OR gate logic	0	0	
Without keeper	1	1	83.3 (nA)
Conditional keeper	0	0	
	1	1	83.2(nA)
High speed domino keeper	0	0	83.2(nA)
Tolerant keeper	0	0	
	1	1	1.65(uA)

Table 3: Comparison table for multiplexer

Logic	Delay (ns)
Existing multiplexer	2.91
Proposed multiplexer	3.10

RESULT AND DISCUSSION

The keepers in literatures and proposed areas are simulated using Tanner EDA Tool; with gate oxide thickness have been 1.25ìm and VDD=5V.

CONCLUSION

Continues scaling of device parameters have been increases the leakage current even though it reduces the size, therefore keepers are used to reduce the leakage current, this papers explains the keeper for OR gates and if this keeper with OR gate is used for the design of multiplexer, which is in the registers of the register files, the leakage current of register files also reduced and it reduces leakage current of processors which increases its the performance. The delay for the multiplexer is reduced from 3.10ns to 2.9ns [5-8].

ACKNOWLEDGEMENTS

The authors would like to thank everyone, just everyone!

REFERENCES

1. Fotty, D., 1998. MOSFET Modeling with SPICE. Englewood Cliffs, NJ: Prentice-Hall, 1997, ch. 11, pp: 399, Fundamentals of Modern VLSI Devices. New York: Cambridge Univ. Press, ch. 2, pp: 95-97.
2. Li, D. and P.Mazumder, 2004. On circuit techniques to improve noise immunity of CMOS dynamic logic, IEEE Trans.Very LARGE scale Integr. (VLSI) Syst., 12(9): 910-925.
3. Griffin, M. M, J. Zerbe, G. Tsang, M. Ching and C.L. Portmann, 1998. A process-independent, 800-MB/s, DRAM byte-wide interface featuring command interleaving and concurrent memory operation, IEEE *J.* Solid-State Circuits, 33(11): 1741-1751.
4. Dadgour, H.F., R.V. Joshi and K. Banerjee, 2006. A novel variation-aware low-power keeper architecture for wide fan-in dynamic gates, in Proc. Des. Autom. Conf., pp: 977-982.
5. Vladimir G. Andronov, 2013. Approximation of Physical Models of Space Scanner Systems World Applied Sciences Journal, 28(4): 528-531.
6. Ahmed Naseer, 2013. Ultrasonically Assisted Turning: Effects on Surface Roughness World Applied Sciences Journal, 27(2): 201-206.
7. Tatyana Nikolayevna Vitsenets, 2014. Concept and Forming Factors of Migration Processes Middle-East Journal of Scientific Research, 19(5): 620-624.
8. Shafaq Sherazi and Habib Ahmad, 2014. Volatility of Stock Market and Capital Flow Middle-East Journal of Scientific Research, 19(5): 688-692.