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VLSI Based 1-D ICT Processor for Image Coding

T. Saravanan, M. Sundar Raj and K. Gopalakrishnan

Department of ETC,
Bharath University, Chennai, India

Abstract: The Integer Cosine Transform (ICT) presents a performance close to Discrete Cosine Transform (DCT) with a reduced computational complexity. The ICT kernel is integer-based, so computation only requires adding and shifting operations. This paper presents a parallel-pipelined architecture of an 1-D ICT(10,9,6,2,3,1) processor for mage encoding. The main characteristics of 1-D ICT architecture are high throughput, parallel processing, reduced internal storage and 100 % efficiency in computational elements. The arithmetic units are distributed and are made up of adders/subtractors operating at half the frequency of the input data rate. In this transform, the truncation and rounding errors are only introduced at the final normalization stage. The performance of the processor has been compared with various multiplier algorithms for the existing pipe-lined architecture.

Key words: Integer Cosine Transform % Image compression % Multiplication free DCT % Parallel pipelined architectures % VLSI

INTRODUCTION

The Discrete Cosine Transform (DCT) is widely considered to provide the best performance for transform coding and image compression [1]. The DCT, which is known to be the closest to the ideal energy compaction transform, has become an international standard for sequential codecs as JPEG, MPEG, H.261, H.263, etc. VLSI implementation of DCT using floating-point arithmetic is highly complex and requires multiplications [2, 3]. The Integer Cosine Transform (ICT) [4] is generally applying the concept of dyadic symmetry and presents a similar performance and compatibility with the DCT using either a programmable processor or dedicated hardware.

The ICT basis components are integers they do not require floating-point multiplications, as these are substituted by fixed-point addition and shifting operations, as they have more efficient hardware implementation.

Decomposition of the ICT: The ICT was derived from DCT by the concept of dyadic symmetry. Let T be the matrix that represents the order-N DCT. The mnth element of this matrix is defined as

$$T_{mn} = \left(\frac{1}{N}\right)^{1/2}\left[K_m \cos\left(\frac{m(n+1/2)p}{N}\right)\right] \quad (1)$$
$$m,n = 0,1...,N-1$$

where

$$k_m = \begin{cases} 1, & if\ m \neq 0\ or\ N \\ \frac{1}{\sqrt{2}}, & if\ m = 0\ or\ N. \end{cases}$$

where K is the normalization diagonal matrix and J an orthogonal matrix made up of the basis components of DCT. is defined as

$$\mathbf{J} = \begin{bmatrix} g & g & g & g & g & g & g & g \\ a & b & c & d & -d & -c & -b & -a \\ e & f & -f & -e & -e & -f & f & e \\ b & -d & -a & -c & c & a & d & -b \\ g & -g & -g & g & g & -g & -g & g \\ c & -a & d & b & -b & -d & a & -c \\ f & -e & e & -f & -f & e & -e & f \\ d & -c & b & -a & a & -b & c & -d \end{bmatrix} \quad (4)$$

a, b, c, d, e, f and g being constants; g is 1. The dyadic symmetry present in reveals that to ensure their orthogonality, the constants a, b, c and d must satisfy the following only condition

Corresponding Author: Saravanan, T., Department of ETC, Bharath University, Chennai, India.

$$ab = ac + bd + cd \quad (5)$$

Furthermore, if J must be similar to DCT, it implies that

$$abc\ d \text{ and } e\ f \quad (6)$$

Those T matrices that satisfy (5) and (6) also have a, b, c, d, e and f constants, which are integers, are called integer cosine transform and are denoted as ICT(a, b, c, d, e, f).

The 1-D ICT for a real input sequence x(n) is defined as

$$X = Tx = KJx = KY \quad (7)$$

where X and x are dimension-8 column matrices and K is the diagonal normalization matrix. Reordering the input sequence and the transform coefficients according to the rules

$$x'(n) = x(n)$$
$$x'(7 - n) = x(n + 4)\ n\ [0, 3] \quad (8)$$
$$X'(m) = X(Br8[m])$$
$$X'(m + 4) = X(2m + 1)\ m\ [0, 3] \quad (9)$$

where Br8 [m] represents bit-reverse operation of length8, then the 1-D ICT can be expressed as

$$X' = T_R x' = K_R J_R x' = K_R Y' \quad (10)$$

The reordered basis components of ICT can be expressed as

$$J_R = \begin{bmatrix} J_{4e} & 0 \\ 0 & J_{40} \end{bmatrix} \begin{bmatrix} L_4 & L_4 \\ L_4 & -L_4 \end{bmatrix} \quad (11)$$

I_4 being the dimension- 4 identity matrix and

$$J_{4c} = \begin{bmatrix} g & g & g & g \\ g & -g & -g & g \\ e & f & -f & -e \\ f & -e & e & -f \end{bmatrix}, \text{ and } J_{4c} = \begin{bmatrix} a & b & c & d \\ b & -d & -a & -c \\ c & -a & d & b \\ d & -c & b & -a \end{bmatrix} \quad (12)$$

Applying the decomposition rules defined in (8) and (9) to the J_{4e} matrix results in

$$J_{4e} = \begin{bmatrix} J_{2e} & 0 \\ 0 & J_{20} \end{bmatrix} \begin{bmatrix} I_2 & I_2 \\ I_2 & -I_2 \end{bmatrix} R_4 \quad (13)$$

where R_4 is the reordering matrix of length 4, I_2 is the dimension-2 identity matrix and

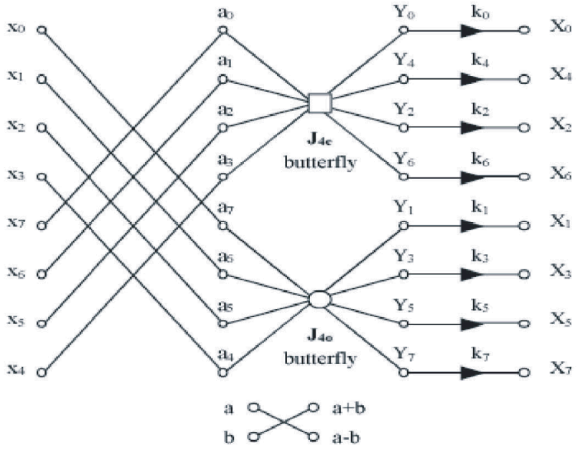


Fig. 1: Signal flow graph of 1-D ICT

$$J_{4e} = \begin{bmatrix} g & g \\ g & -g \end{bmatrix} \text{ and } J_{2o} \begin{bmatrix} e & f \\ f & -e \end{bmatrix} \quad (14)$$

In this case, the matrices J_{4e} and J_{4o} are defined as

$$\mathbf{J_{4e}} = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & -1 & -1 & 1 \\ 3 & 1 & -1 & -3 \\ 1 & -3 & 3 & -1 \end{bmatrix} \quad (15)$$

$$\mathbf{J_{4o}} = \begin{bmatrix} 10 & 9 & 6 & 2 \\ 9 & -2 & -10 & -6 \\ 6 & -10 & 2 & 9 \\ 2 & -6 & 9 & -10 \end{bmatrix} \quad (16)$$

1-d Ict Parallel Pipeline Architecture

Signal Flow Graph: Fig:1 shows the signal flow graph obtained by applying the decomposition process to ICT(10, 9, 6, 2, 3, 1).

As can be seen in Fig:1, the first computing level operates on the input data, reordering them according to rule (8); additions and subtractions of data pairs formed with sequences x'(n) and x'(n+4) (n= 0, 1, 2, 3) are executed. In the second computing level the transformations J_{4e} and J_{4o}, are obtained, their nuclei being the matrices defined by (15). The transformation J_{4e} is applied to the first half of the intermediate data sequence, a_0 to a_3, giving as a result the even coefficients (Y_0, Y_2, Y_4, Y_6) of the ICT, without normalization. Similarly, J_{4o} is applied to the other half of the middle data sequence, a7 to a4, giving as a result the odd coefficients (Y_1, Y_3, Y_5, Y_7) of the ICT, also without normalization. In the third computing level, the coefficients Y_i are normalized by k_i and the transform sequence of the coefficients X(m) appears reordered according to rule (9).

Applying the decomposition procedure of J_{4e} established in (10) and (11), we get

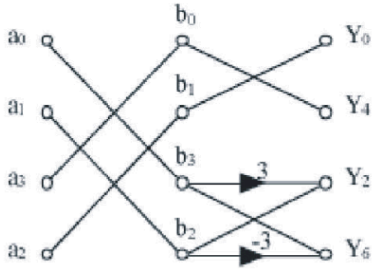


Fig. 2: Signal flow graph of J_{4e} processor

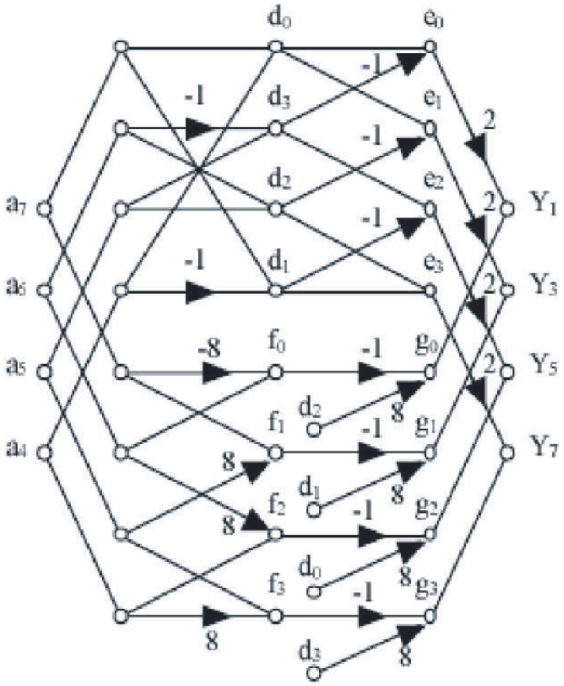


Fig. 3: Signal flow graph of J_{4o} processor

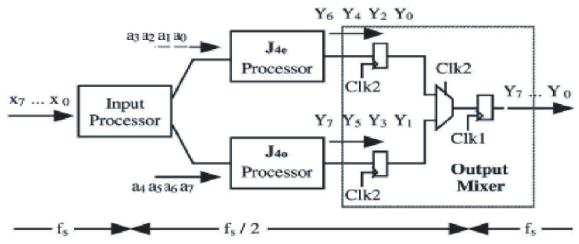


Fig. 4: Architecture of 1-D ICT processor

$$\begin{bmatrix} Y_0 \\ Y_4 \\ Y_2 \\ Y_6 \end{bmatrix} = \begin{bmatrix} 1 & 1 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 3 & 1 \\ 0 & 0 & 1 & -3 \end{bmatrix} \begin{bmatrix} 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \\ 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & -1 \end{bmatrix} \begin{bmatrix} a_0 \\ a_1 \\ a_3 \\ a_2 \end{bmatrix} = \begin{bmatrix} 1 & 1 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 3 & 1 \\ 0 & 0 & 1 & -3 \end{bmatrix} \begin{bmatrix} b_0 \\ b_1 \\ b_3 \\ b_2 \end{bmatrix} \quad (17)$$

b_0, b_1, b_2 and b_3 being the intermediate data of the computation of transformation. J_{4e} operating on (17), we get:

$$\begin{bmatrix} Y_0 \\ Y_4 \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \begin{bmatrix} b_0 \\ b_1 \end{bmatrix} \quad \text{and} \quad \begin{bmatrix} Y_2 \\ Y_6 \end{bmatrix} = \begin{bmatrix} 3 & 1 \\ 1 & -3 \end{bmatrix} \begin{bmatrix} b_3 \\ b_2 \end{bmatrix} \quad (18)$$

Fig:2 shows the signal flow graph obtained from (17) and (18).

As can be seen in (17), the computation of the even coefficients of the ICT can be performed with additions and subtractions, as multiplication by 3 can be easily implemented by means of add and shift operations. The computation of the odd coefficients of the ICT can also be simplified; decomposition of the J_{4o} matrix as the addition of matrices having elements that are powers of 2, gives:

$$\begin{bmatrix} Y_1 \\ Y_3 \\ Y_5 \\ Y_7 \end{bmatrix} = \begin{bmatrix} 2 & 2 & -2 & 2 \\ 2 & -2 & -2 & 2 \\ -2 & -2 & 2 & 2 \\ 2 & 2 & 2 & -2 \end{bmatrix} \begin{bmatrix} a_7 \\ a_6 \\ a_5 \\ a_4 \end{bmatrix} + \begin{bmatrix} 0 & 8 & 8 & 0 \\ 8 & 0 & 0 & -8 \\ 8 & 0 & 0 & 8 \\ 0 & -8 & 8 & 0 \end{bmatrix} \begin{bmatrix} a_7 \\ a_6 \\ a_5 \\ a_4 \end{bmatrix} - \begin{bmatrix} -8 & 1 & 0 & 0 \\ 1 & 0 & 8 & 0 \\ 0 & 8 & 0 & 1 \\ 0 & 0 & 1 & 8 \end{bmatrix} \begin{bmatrix} a_7 \\ a_6 \\ a_5 \\ a_4 \end{bmatrix} \quad (19)$$

In this form, the odd coefficients of the ICT can be implemented simply in terms of add and shift operations. Fig: 3 shows the signal flow graph, obtained from (19) for the transformation J_{4o}, having three computing levels, d_i, f_i, e_i and g_i (i = 0, 1, 2, 3) being the intermediate data.

Architechture of 1-d Ict Processor: The 1-D ICT multiplication-free processor architecture, whose scheme is shown in Fig: 4, has been designed to implement the computing diagram of Fig:1 with the highest degree of efficiency. It has an input processor computing the intermediate data of the first computing level, a_0 to a_7, two processors in parallel, computing the transformations J_{4e} and J_{4o} and an output mixer generating the coefficients sequence of the ICT, ordered in natural form. The three processors have parallel architecture, allowing the operation frequency to be reduced to $f_s/2$, where f_s is the input data sampling frequency. The output mixer gives the coefficients sequence of the ICT at the frequency f_s. The control of the processor is very simple and is carried out using four signals: Clk1, external clock at frequency f_s; Clk2, internal clock at frequency ; and the multiplexer selection signals S1 at frequency $f_s/2$ and S2 at frequency $f_s/8$. The arithmetic multiplications have been separated into x 2, x 3, x 8 terms so that the arithmetic units are reduced to adders and to substractors combined with wired-shift operations [5-7].

Input Processor: The input processor has a shift register which stores the input data sampled at frequency f_s, two multiplexers 4:1, an adder and a subtractor. The adder and the subtractor both have pipeline structure and operate in parallel at frequency f_s /2, generating the input sequences, (a_0, a_1, a_2, a_3) and (a_7, a_6, a_5, a_4), of processors J_{4e} and J_{4o}

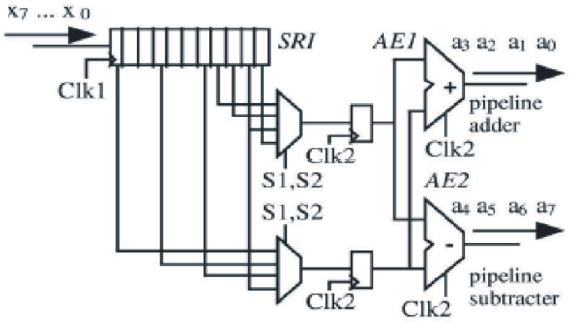


Fig. 5: Architecture of Input processor

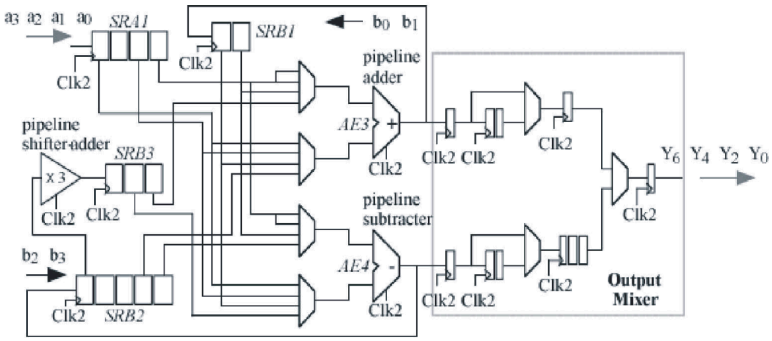


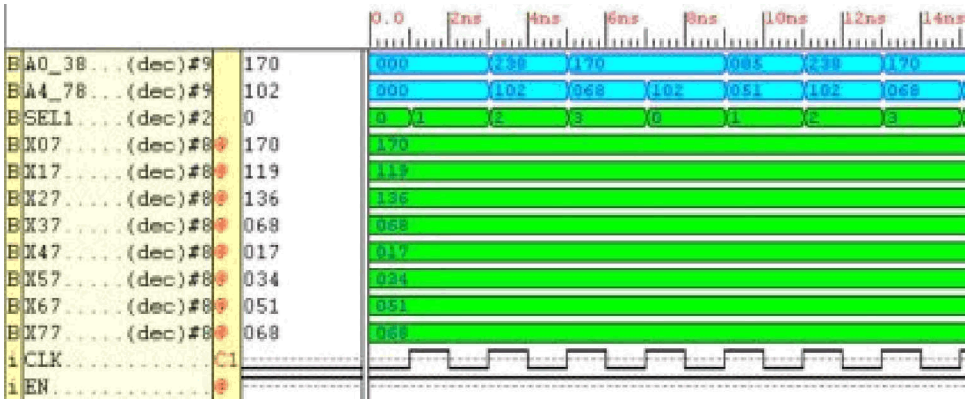
Fig. 6: Architecture of J_{4e} processor

from the data stored in the register. In this way an efficiency of 100% is attained for the arithmetic elements [8-11].

J_{4e} Processor: The processor J_{4e} has been conceived to calculate the even coefficients of the ICT using the procedure established in (13), (14) and its signal flow graph shown in Fig: 2. The adder and the subtractor, which operate in parallel at frequency $f_s/2$, generate first the intermediate data (b_0, b_1, b_2, b_3) from the input sequence (a_0, a_1, a_2, a_3), stored in the register SRA1; b_0 and b_1 are stored in register SRB1, while b_2 and b_3 are stored in SRB2. The multiplier by 3, implemented by adding and shifting, generates the data 3b2 and 3b3, which are stored in register SRB3. After that, the even coefficients of the ICT are generated from the data stored in SRB1, SRB2 and SRB3: Y_0 and Y_2 in the adder AE3, Y_4 and Y_6 in the subtracter AE4. The output mixer orders the even coefficient sequence of the ICT (Y_0, Y_2, Y_4, Y_6). In this processor, the adder and the subtractor have an efficiency of 100%.

Output Waveforms:

Input Processor Output



Output of J_{4e} Processor

Output of 1-d Ict Processor

Modification: The performance of the processor has been verified with various algorithms for the existing pipe-lined architecture. Multiplier architectures can be classified as either array topologies or tree topologies [6]. The pipe-lined adder/subtractor algorithm is effective for both array and tree multipliers. The proposed algorithm can be applied to many digital systems practically, where minimizing power consumption is important. There is a substantial reduction in the number of logic transitions and a corresponding power savings with a small increase in area.

CONCLUSION

This paper presents a parallel-pipelined architecture of an 1-D ICT(10,9,6,2,3,1) processor for mage encoding. Two 1-D ICT processors can be pipe-lined to make a 2-D ICT architecture. The parallel-pipeline architecture proposed allows a higher operating speed and the pipelined adders/subtractors have 100% efficiency operating at half the frequency of the input data rate. The performance is evaluated based on different algorithm for the same architecture and results are discussed. Other characteristics of this architecture are high throughput, parallel processing and reduced internal storage. The authors think the ICT will be used in increasingly many applications in the future.

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