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High Speed CMOS Charge Pump Circuit for PLL Applications Using 90nm CMOS Technology

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Abstract: The performance of charge pumps depends heavily on the ability to efficiently generate high voltages on-chip while meeting stringent power and area requirements. The paper presents a High Speed CMOS charge pump circuit for PLL applications using 90nm CMOS technology that operates at 1V. The proposed circuit has simple symmetric structure and provides more stable operation while reducing spurious jump phenomenon. The experimental result shows significant improvement in overcoming the problem of jitter. The output voltage of presented design can be increased up to 1010mV. The functionality of charge pump has been tested at operating based frequency of 1000 MHz.

Key words: Charge pump · Phase locked loops (PLL) · High speed · High speed network · Low voltage

INTRODUCTION

Wireless telecommunication has typical element known as Phase locked loop (PLL) are mostly used in computers, radio, telecommunications and other electronic applications. PLL has elements such as WLANs, mobile communications and satellite. In the 1930s, phase locking concept was invented and swiftly found wide usage in electronics & communication. While the basic phase-locked loop has remained nearly the same since then, its implementation in different technologies and for different applications continue to challenge designers.

PLL is simple feedback system that compares the output phase with the input phase and produces the output frequency which is proportional to the input phase difference

Now days low-cost and small size circuits are increasing in demand; So RF designers face this problem. They are doing more effort in low-cost CMOS technologies for achieving higher levels of integration of RF transceivers. To enable single-chip fully integrated solutions, PLL synthesizers are important building blocks, alongside the digital signal processors.Worlds of advanced IC technology, PLLs are available cheaper monolithic ICs.

Theory of PLL: After the invention of PLL in1932, the basic phase locked loop has remained nearly the same but its implementation in different technologies is still a challenge for technicians.

A PLL is a feedback system that compares the output phase with the input phase. The comparison is performed by a 'phase comparator' or 'phase detector'. A phase detector is a circuit whose average output voltage is proportional to the phase difference ÄΦ, between two inputs. While in ideal case relation between output voltage and input phase difference is linear.

The basic elements of a Phase locked Loop (PLL) are a Phase detector (PD), Low Pass Filter (LPF) and a voltage-controlled oscillator (VCO) in a feedback loop (Fig. 1). The role of Phase Detector is to compare the phase of V_{out} and V_{in} then generating an error.

To remove the high frequency content in PD output voltage, the output of PD is passed through low pass filter. This is required because; the control voltage of oscillator must remain quit in steady state. To avoid losses due to large interference transient filter also provides a memory for the loop.

A Low pass filter is interpose between the PD and The VCO which is used to suppress the high-frequency components of the Phase Detector (PD) output and presenting the dc level to the oscillator.

Input of VCO receives the filtered controlled voltage. Control voltage forces the VCO to change the frequency in the direction that reduces the difference between input frequency and output frequency. If two frequencies are sufficiently close, the PLL feedback mechanism forces the two PD input

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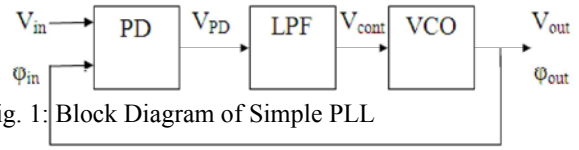

Fig. 1: Block Diagram of Simple PLL

frequency frequencies to be equal and the VCO is locked with incoming frequency this is called as locked state of PLL.

Once the loop is in locked state, there will be small phase difference between the two PD input phase signals. To shift the VCO from free running state and keeping the loop in locked state output is required from phase detector.

According to that error, VCO frequency varies until the phases are aligned, i.e. the loop is locked. The phase detector (PD) output, V_{PD}, consists of a high-frequency components (undesirable), dc component (desirable) and the control voltage of the oscillator must remain quiet in the steady state, i.e. the PD output must be filtered.

Above diagram explains the simple working of PLL. If the loop of Fig.1 is locked, we postulate that Φ_{out} - Φ_{in} is constant and preferably small. We therefore define the loop to be locked if Φ_{out} - Φ_{in} does not change with time. An important corollary of this definition is that

$$(d\Phi_{out}/dt) - (d\Phi_{in}/dt) = 0 \quad (1.1)$$

And hence

$\omega_{out} = \omega_{in}$ Which is unique property of PLL's

The PD output contains a dc component equal to *K*PD (Φout -Φin) along with high frequency components which are filtered by the LPF. PD is simply modeled as a subtractor whose output is amplified by *K*PD. The overall PLL model consists of the phase subtractor, the LPF transfer function $1/(1+ s/\omega LPF)$, where ωLPF is the 3 dB bandwidth and the VCO transfer function *KVCO*/*s*. Here, Φ in and Φ out are the excess phases of input and output waveforms, respectively.

The open loop transfer function is given by

$$H(s)|open = \frac{\Phi_{out}}{\Phi_{in}}(S)|_{open} \quad (1.2)$$

$$= K_{PD}.\frac{1}{(1+s/\omega_{LPF})}.\frac{K_{VCO}}{s} \quad (1.3)$$

From (1.3) closed loop transfer function can be obtained as:

$$H(s)|_{colsed} = \frac{KPD\ .\ KVCO}{(s^0/\omega_{LPF}+s+K_{PD}.K_{VCO})} \quad (1.4)$$

Here $H(s)|_{closed}$ is simply denoted by Φ_{out}/Φ_{in}. Further since the frequency & phase are related by linear operator, the transfer function of (1.4) can be expressed as:

$$\frac{\omega_{out}(s)}{\omega_{in}} = \frac{K_{PD}.K_{VCO}}{(s^2/\omega_{LPF}+s+K_{PD}.K_{VCO})} \quad (1.5)$$

This is second order transfer function of type 1 PLL. Using the control theory approach the "natural frequency" & "damping ratio" are given by:

$$\omega_n = \sqrt{(\omega_{LPF}.K_{PD}.K_{VCO})} \quad (1.6)$$

$$\xi = \frac{1}{2}\sqrt{(\omega_{LPF}/K_{PD}.K_{VCO})} \quad (1.7)$$

The step response is given by:

$$\omega_{out}(t) = \left[1 - \frac{1}{\sqrt{1-\xi^2}}e^{-\zeta w_n t}\sin\left(\omega_n\sqrt{1-\xi^2}t+\theta\right)\right]\Delta\omega u(t) \quad (1.8)$$

Where ω_{out} denotes the change in output frequency & $\theta = \sin^{-1}(1-\xi^2)^{1/2}$. Thus as per control theory approach we can say that the step response will contain a sinusoidal component with frequency $\omega_n = (1-\xi^2)^{1/2}$ that will decay with time constant $(\xi\omega_n)^{-1}$.

Referring to above Discussion it Can Be Concluded That:

In most of the applications settling speed of PLL is of great concern. Equation (1.8) thus, shows that the exponential decay determines how fast the output approaches its final value, provided that $\zeta\omega_n$ is maximized. Using equation (1.6) and (1.7), yields,

$$\zeta\omega_n = \frac{1}{2}\omega\omega_{LPF} \quad (1.9)$$

this result shows the critical tradeoff between settling speed and ripple on the VCO control line. Greater high frequency components are suppressed, only if we reduce the cutoff frequency of the filter but at the same time pull in time increases.

In addition to value of $\zeta\omega_n$, value of ζ is also important. If ζ is less than typically 0.5, step response exhibits high amplitude oscillations before settling. Hence in order to avoid this ringing, the value of damping ratio is normally kept 0.707 or even greater than or equal to 1.

Equation (1.7) shows that both phase error and ζ are inversely proportional to *KPD* and *KVCO*. Hence lowering the phase error makes the system less stable. Thus in summary the simple PLL (type I) has a drawback of trade off between the pull in time, the ripple on the

control voltage, the phase error and the stability. If PLL uses simple Phase detector in its architecture, it is called as simple PLL. But if PLL uses Phase Frequency Detector accompanied with Charge Pump, it is called as "Charge Pump PLL".

A PLL serving the task of clock generation in a microprocessor appears quite similar to a frequency synthesizer used in a cell phone, but the actual circuits are designed quite differently. PLL is used to recover a signal from a noisy communication channel, generate stable frequencies or distribute clock timing pulses in microprocessors. PLL's have been successfully integrated in many technologies, e.g. bipolar. MESFET, CMOS and SiGe, with frequencies of operation from the mega-Hertz to the giga-Hertz ranges PLL plays a significant role in a pure digital system. Digital signal processor clock generation, High-performance microprocessors clock distribution and clock synchronization are similar to phase locked loop. Fully monolithic phase-locked loops in CMOS have been usually used in many applications, such as workstations, PC and wireless communication systems. Now days, PLL is used in every places in our daily life. The PLL based frequency synthesizer plays a very significant role in direct frequency modulator, frequency demodulator and the regeneration of the carrier from the input signal in the wireless communications. PLL is used for clock and data recovery circuit in the broadband data communication network, which is used to recover the data from the NRZ clock and data re-timed decision.

This paper is organized as follows Section II presents the basic concept of charge pump phase locked loop (CPPLL). In section III, circuit description of the charge pump is presented. Section IV shows the simulation results of the proposed charge pump circuit and finally conclusion is presented in the last section.

Charge Pump Phase Locked Loop(CPPLL): Charge pump is one of the important parts of PLL which converts the phase or frequency difference information into a voltage, used to tune the VCO.

Charge pump based phase-locked loops (CPLL) are widely used as clock generators in a variety of applications including microprocessors, wireless receivers, serial link transceivers and disk drive electronics. A charge pump is a three position electronic switch which is controlled by the three states of PFD. When switch is set in UP or DOWN position, it delivers a pump voltage $\pm VP$ or a pump current $\pm IP$ to the loop filter. When both UP and DOWN of PFD are off, i.e. N position, the switch is open, thus isolating the loop filter from the charge pump and PFD.

One of the main reasons for the widely adopted use of the CPLL in most PLL systems is because it provides the theoretical zero static phase offset and arguably one of the simplest and most effective design platforms. The loop bandwidth, damping factor, lock range can be obtained by providing flexible design tradeoffs by decoupling. While there are numerous CPLL design examples in the literature, precise analysis and a mathematical clarity of the loop dynamics of the CPLL is lacking.

The intent of this paper is to clarify and provide mathematically exact and insightful understanding of the PLL dynamics and accurate transfer functions of a practical CPLL system. The focus of the detailed derivations and analysis is on the CPLL example because IC designers predominantly choose CPLLs over other PLL architectures.

Although the presentation is for a CPLL, the analysis can be readily extended for other PLL systems.

Charge Pump PLL: In this paper, we focus on the CPPLL architecture, because it can provide zero phase error and an extended frequency range of operation. Many PLL systems have adopted this architecture as it is one of the simplest and effective.

A block diagram of a CPPLL is shown in Figure 2. It consists of five blocks, namely phase frequency detector (PFD), charge pump (CP), loop filter (LF), voltage controlled oscillator (VCO) and divider. We will describe the blocks one by one in the remaining of this section. The PLL system is typically mixed analog-digital in nature.

The structure shown in Fig. 2 is called a charge pump PLL (CPPLL), such an implementation senses the transistor at the input and output, detects phase or frequency difference and activates the charge pump accordingly.

One application of CPPLLs is to generate a signal of changing frequency for clock generation. The output frequency can be set to multiples of the reference input frequency Fref by changing the ratio N of the divider: $F\text{out} = N\,F\text{ref}$. Due to changing value of the the divider the CPPLL is oscillating in unlocked frequency which is different from the desired one. The locking time is defined as the time taken by the CPPLL to synchronize with or to lock onto the new frequency. In this application the fast dynamic is more critical than the noise rejection in other applications,E.g. clock recovery.

Additional stability of the PLL system must be guaranteed. Therefore the phase margin and reference frequency to Unity-gain-bandwidth ratio (RUR) must be considered. Usually the PLL locking time and stability

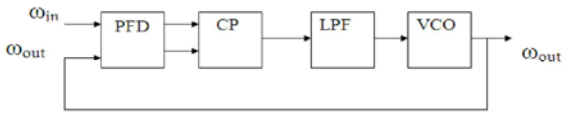

Fig. 2: Block Diagram of CPPLL

are analyzed in the *s*-domain. But the *s*-domain analysis is based on a continuous time approximation of the CPPLL and cannot accurately estimate the locking time. Besides *s*-domain analysis, two analyses using an event-driven non-linear model for a 2nd-order CPPLL in and state-space equations for a 3rd-order CPPLL in are proposed, which can provide exact models of the PLL dynamics. But it is difficult to set up or adapt these equations to other architectures especially for higher-order PLLs. In contrast behavioral models can be set up and modified for other applications or higher-order PLLs rather easily relative to provide a more accurate estimation of the locking time than *s*-domain analysis.

Introduction: Charge pump is one of the important parts of PLL which converts the phase or frequency difference information into a voltage, used to tune the VCO. Before arriving at the concept of charge pump, the problem of simple PLL which uses phase detector is discussed here.

Limitations Of Simple PLL Architecture: For type I PLL there are always trade-offs between damping ratio of loop filter, loop filter bandwidth and the phase error. Hence the performance of PLL cannot improve beyond certain limit.

Apart from this, a simple PLL suffers from a critical drawback i.e. limited acquisition range,Suppose when a PLL circuit is turned on, its oscillator operates at a frequency far from the input frequency, i.e. the loop is not locked. Now PLL starts acquiring a lock. The transition of the loop from unlocked to locked condition is very nonlinear process because phase detector senses unequal frequency. Also for this kind of PLL, the "acquisition range" is on the order of ω_{LPF}, that is, the loop locks only if the difference between ω_{in} and ω_{out} is less than roughly ω_{LPF}. If ω_{LPF} is reduces to suppress the ripple on control voltage, the acquisition range decreases. Even if the input frequency has a precisely controlled value, a wide acquisition range is often necessary because the VCO frequency may vary considerably with the process and temperature. Hence in order to remove this problem, frequency detection is also incorporated in addition to phase detection. The concept is such that let the two frequencies (reference and VCO output frequency) be equal, once these two frequencies are equal, phases are compared and VCO is tuned such that phases of reference and feedback waveform are equal. Frequencies are compared using frequency detector which generates a dc voltage equal to the difference of two input frequency and drives the VCO such that $\omega_{in} = \omega_{out}$. When $|\omega_{in} - \omega_{out}|$ is sufficiently small, phase locked loop takes over, acquiring lock. Such scheme increases the acquisition range to the tuning range of VCO.

As technology changes, our demands are also increases. High-speed, portable and low power consumption communication systems have become increasingly common day by day. These systems require high-precision local clock generator (1ocal oscillator) and difficulty is deal with the help of PLL circuit design. Due to the irreplaceable advantages, this technology is most widely in CMOS charge pump phase locked loop (CPPLL). CPPLL is a very simple and efficient method of designing PLL having low jitter and low power, zero static phase error and high speed.The output voltage of the charge pump circuit must be held on a constant voltage, when PLL locks in some frequency. So, this is important to generate a stable step voltage for designing of a charge pump circuit for PLL.

This is difficult to design of ideal CPPLL circuit. It is very typical issue, to decrease clock feed through from the charge pump to the local voltage controlled oscillator (VCO). The objective is to obtain minimum power dissipation with a large output voltage range under a low power supply. The frequency of operation of the VCO is controlled by output voltage of the CP; any spike in this voltage produces undesirable spurious tones in the VCO output signal. A new charge pump operates under a 1V power supply and does not bring about the common spurious jump phenomenon.

When the loop is turned on, ω_{out} may be far from ω_{in} and the charge pump, as a frequency detector, varies the control voltage such that ω_{out} approaches ω_{in}. When the input and output frequencies are very close, the PFD operates as a phase detector, performing phase lock. The loop locks when the phase difference drops to zero and charge pump remains relatively idle.

- *Now in this paper we would discuss the deailed scope of proposed charge pump and compare it with the conventional one.*

Conventional Charge PUMP: The circuit of charge pump is shown in Fig. 3. When the UP signal is high ("1"), the switch M1 is 'ON' and Cp is charged by the upper current source I1. When the DN signal is high, the switch M2 is 'ON' and Cp is discharged through the lower current source I2. If both of the signals UP and DN are low ("0"), then M1 and M2 are both off at node P and Vc holds the original voltage.

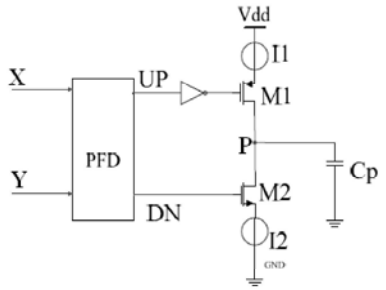

Fig. 3: The simple model of the charge pump circuit

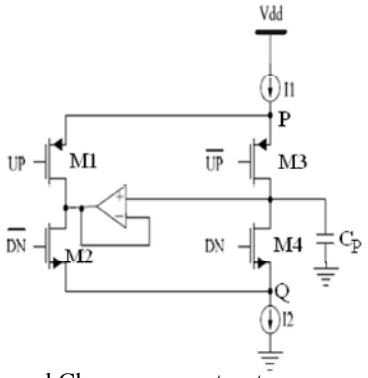

Fig. 4: Improved Charge pump structure

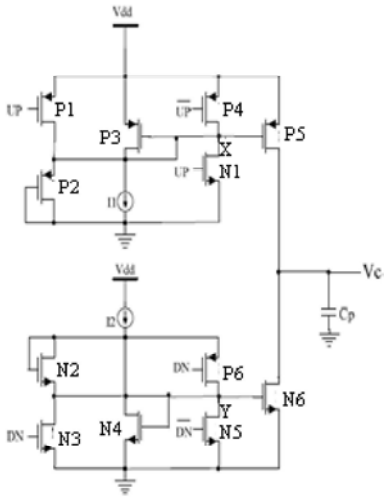

Fig. 5: New charge pump circuit

There are many limitations in the conventional charge pump circuit shown in Fig. 3 For example, when UP and Down both are low then voltage at capacitor Cp is left floating, while the voltages at the sources of I1 and I2 are rapidly pulled to VDD and ground respectively. MOS switch has non-ideal characteristics such as clock feed through and charge injection, this rapid change in the source voltages creates glitches in the capacitor current, which can result in a jump in the stored voltage VCp. If there is any jump in VCp then it adds undesirable spurious tones and phase noise to the output signal of the VCO

Fig. 4 shows the schematic diagram of the conventional improved charge pump circuit. It is a possible approach to overcome this problem. It uses the OP amp circuit as feedback; the function of this is to hold the voltages of node P and node Q. It also enhances the performance of the charge pump and improves the voltage jump phenomenon. It reduces the complexity and power consumption.

Proposed Charge PUMP Structure: There are number of charge pump circuits were designed to reduce jump phenomenon from time to time. The proposed circuit, as shown in Fig.5, is a new way to achieve this purpose and increases the output voltage range.

The Proposed charge pump circuit consists of pull-up & pull-down network. The charge pump circuit works as follows,

- When the signal UP =1 (high logical level), P1 is 'OFF' and the current source I1 drives P3. Since the power supply is 1V, when P3 is 'ON', the voltage headroom between gate and source of P2 is not enough to open it. Obviously, P5 is 'ON' and so P3 and P5 compose a current mirror. Capacitor Cp will be charged by the current source I1, raising the voltage Vc. In other hand DN =0 (Low logical level), pull-down network is OFF.
- When the signal UP =0 (low logical level), P1 and P2 are both 'ON'. Since IP1=IP2+I1, The current in P3 and P5 are so small that they are negligible. Then, the voltage Vc at the capacitor should, ideally, remain stable. P4 and N1 are used to predischarge to the gate of P5 (pre-discharge at the gate of N6). If they are cancelled in this charge pump circuit, when the UP signal is switched from 0 to 1, the charging time of P3 is relatively long, which results in delaying open speed of P5. So to overcome this problem, P4 and N1 are taken advantage at the gate of P5. Then, the voltage at the gate of P5 is rapidly pulled down once the UP signal switches from 0 to 1 opening P5 in a much shorter time. In other hand DN =1 (High logical level), pull-down network is 'ON' and capacitor Cp will be discharged.

When they are both ON, they operate in the saturation region. So, to carry the same currents, P4 and N1 have to be perfectly matched ($I_P4=I_N1$). M eanwhile, in order to minimize the introduction of the parasitic capacitance, the width and length values of P4, N1 must be as small as possible.

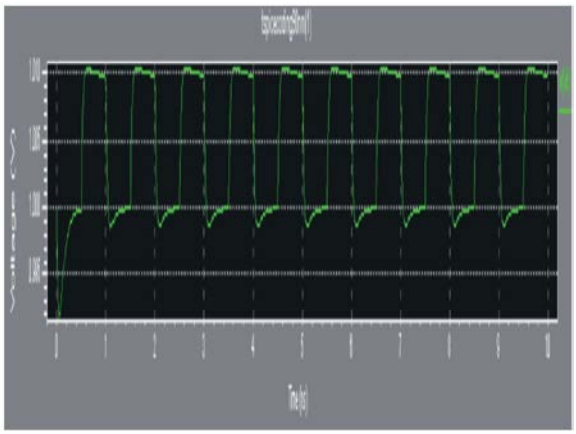

Fig. 6: Charging & Discharging waveform of the charge pump.

Table 1: Performance Summary

Parameters	Results
Power Supply (Vdd)	1V
Operating frequency	1000MHz
Pull up & Pull down current	100µA
Output voltage range	995mv to 1010mV
Technology	90nm CMOS

- *Thus we can say that A charge pump is a three position electronic switch which is controlled by the three states of PFD. When switch is set in UP or DOWN position, it delivers a pump voltage ±VP or a pump current ±IP to the loop filter. When both UP and DOWN of PFD are off, i.e. N position, the switch is open, thus isolating the loop filter from the charge pump and PFD, which could be seen in fig. of charge pump.*

Simulations Results: The new charge pump circuit is designed in 90nm CMOS process, simulated using T-Spice under a 1V power supply. The pull up current I1 and the pull down current I2 are both set to 100µA. The operating frequency is 1000MHz and Fig. 6 shows the charging and discharging result of the new charge pump circuit. The output voltage range is from 995mV up to 1010mV.

A summary of the circuit characteristics is presented in Table I.

CONCLUSION

In this paper, a high speed CMOS charge pump for PLL application has been designed and simulated using the 90nm CMOS technology. The simple and symmetric structure of the circuit reduces spurious jitter phenomenon and provide more stable operation under a 1 V power supply without use of op-amp circuit. It has output voltage range from 995mV up to 1010mV and more stable step voltage. Simulations were done using T-Spice. The pull-up current I1 and the pull down current I2 are both set to 100µA. The operating frequency is 1000MHz.

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