Middle-East Journal of Scientific Research 12 (1): 01-05, 2012
ISSN 1990-9233

DOI: 10.5829/idosi.mejsr.2012.12.1.1783

Hardware Realization of Robertson's Multiplier

Mohammed H. Al Mijalli and Muhammad H. Rais

Department of Biomedical Technology,
College of Applied Medical Sciences, King Saud University, Riyadh, Saudi Arabia

Abstract: In this paper we present Robertson's multiplier design and implementation in Spartan-3 device XC3S400 (package: pq208, speed grade: -5) and Virtex-5 device XC5VLX50 (package: ff676, speed grade: -3), Field Programmable Gate Array (FPGA), using Very High speed integrated circuit Hardware Description Language (VHDL). The FPGA resources utilization are obtained for 4×4, 6×6, 8×8, 12×12, 16×16 and 32×32 bit Robertson's multipliers. The four input look up tables (LUTs), occupied slices, total equivalent gate count and delay have been gradually incresed for Robertson's multipliers for Spartan-3 and Virtex-5 FPGAs. The values obatined for bonded IOBs are similar for Robertson's 4×4, 6×6, 8×8, 12×12, 16×16 and 32×32-bit multipliers in Spartan-3 and Virtex-5 FPGA devices. The Virtex-5 FPGA shows less use of embedded resourses for LUTs, occupied slices and total equivalent gate count as compared to Spartan-3 FPGA. The delay in Virtex-5 is reduced remarkably from 6.145 ns to 35.826 ns for 4×4-bit multiplier to 32×32-bit multiplier as compared to Spartan-3 from 14.958 ns to 90.720 ns for 4×4-bit multiplier to 32×32-bit multiplier.

Key words: Field Programmable Gate Array (FPGA) · Robertson's multipliers · Spartan-3 · Virtex-5 · Very High speed integrated circuit Hardware Description Language (VHDL)

INTRODUCTION

Inception of the digital computers is significantly based on multipliers. Multiplication is a sole part of Digital Signal Processing (DSP), communication and other Application Specific Integrated Circuits (ASICs) systems. Significance of multiplication in scientific and engineering computations has led to a number of implementation techniques for multiplication [1-6]. Many applications for multipliers illustrate different requirements for speed, area, power consumption and other specifications. Current progress in Field Programmable Gate Array (FPGA) performance and size offer a new hardware acceleration opportunity and provides real time configuration over ASICs. Contemporary communication system requirements are further pushing DSP system performance necessities outside the capabilities of DSPs. Xilinx FPGA family includes embedded DSP block multipliers which make them an exceptional solution for DSP systems. There are several reports have been reported on the realization of implementation of parallel multipliers [7-12].

The purpose of this paper is to present the hardware implementation of Robertson's 4×4, 6×6, 8×8, 12×12, 16×16 and 32×32 bit multipliers in Spartan-3 device XC3S400 (package: pq208, speed grade: -5) and Virtex-5 device XC5VLX50 (package: ff676, speed grade: -3) using Very High speed integrated circuit Hardware Description Language (VHDL).

MATERIALS AND METHODS

Spartan-3 and Virtex-5 FPGA Platform: FPGAs are primarily programmable hardware implementation devices. Computation intensive tasks assigning to hardware implementation has speedup in computation time. By trading off precision and range in the number format for an increased number of parallel arithmetic units is allowed for even higher performance by the suppleness of the FPGA. A new type of processing called reconfigurable computing has been introduced thereby in which time intensive tasks are offloaded from software to FPGAs. They make an ideal platform for the implementation of computationally intensive and

Corresponding Author: Dr. Muhammad H. Rais, Department of Biomedical Technology, College of Applied Medical Sciences, King Saud University, Riyadh, Saudi Arabia.

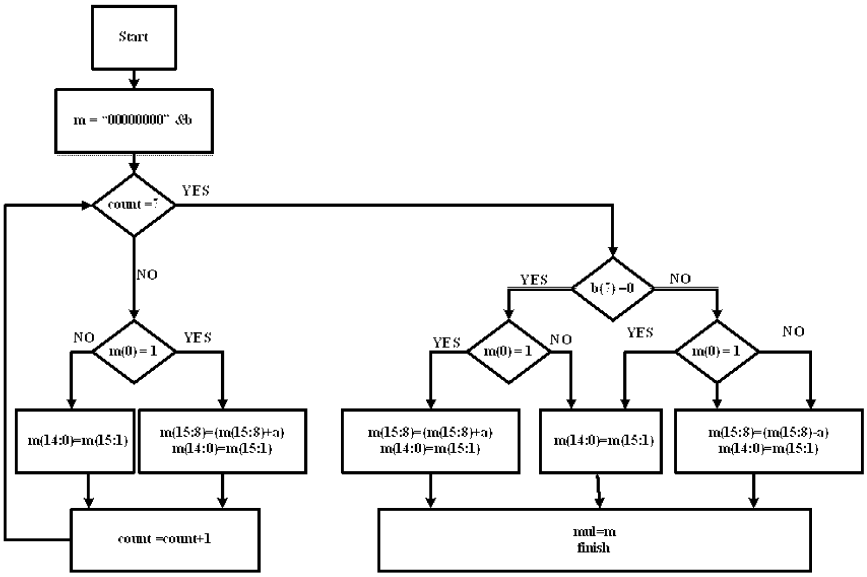

Fig. 1: The 8×8-bit Robertson's multiplier flowchart

massively parallel architecture owing to the parallel nature, high frequency and high density of modern FPGAs.

Spartan-3 [13] Xilinx FPGA is planned to meet the requirements of high volume and low cost electronic systems. The Spartan-3 family consists of eight member providing densities starting from 50,000 to five million system gates. The Spartan-3 FPGA consists of five fundamental programmable functional elements such as configurable logic blocks (CLBs), input-output blocks (IOBs), Block RAMs, 18×18 bit dedicated multipliers and digital clock managers (DCMs).

Computationally intensive DSP and image processing algorithms can be accelerated using advanced DSP48E slices available in Virtex-5 [14] Xilinx FPGAs. The static power consumption has been reduced in Virtex-5 due to triple-oxide technology. The Virtex-5 FPGA provides high speed serial transceiver block to be utilized for enhanced serial connectivity.

Robertson's Multipliers: Robertson's multiplier algorithm flowchart for 8×8-bit multiplier is shown in Figure 1. The Robertson's multiplier considers multiplication of two operands X and Y depending on their sign for 8×8-bit numbers, $X = X_{0...}X_{n-1}$ and $Y = Y_0....Y_{m-1}$ of which there are four cases to be considered.

i. When both operands are positive, that is, $X_0 = Y_0 = 0$, this is similar to multiplication of two unsigned numbers. The product P is calculated in a series of add and shift steps of the form.

$$P_t \leftarrow P_i + X_j \times Y$$
$$P_i \leftarrow P_i \times 2^{-1}$$

Each partial product is non negative, therefore leading 0s are introduced during right shift of the partial product.

ii. When first operand is negative and second is positive, i.e., $X_0 = 1$ and $Y_0 = 0$. Here partial product outcome is always positive. In the final step a subtraction is done, i.e.,

$$P \leftarrow P - Y$$

iii. When first operand is positive and second is negative, i.e., $X_0 = 0$ and $Y_0 = 1$, the output of the partial product is positive. Hence, leading 0s are shifted into the partial product until the first 1 in X is encountered. Multiplication of Y by this 1 and addition to the result thereby cause the partial product to be negative. Then, leading 1s are shifted into the partial product rather than 0s.

iv. When both operands are negative, i.e., $X_0 = 1$and $Y_0 = 1$, the leading 1s are shifted into the partial product. Since X is negative, the correction step similar to case (ii) is again applied.

RESULTS

The design of Robertson's multipliers 4×4, 6×6, 8×8, 12×12, 16×16 and 32×32 -bit are done using VHDL and implemented in Xilinx Spartan-3 FPGA XC3S400 (package: pq208, speed grade: -5) and Virtex-5 FPGA XC5VLX50 (package: ff676, speed grade: -3) using the Xilinx ISE 9.2i design tool [15].

DISCUSSION

The block diagrams of Robertson's 4×4, 6×6, 8×8, 12×12, 16×16 and 32×32-bit multipliers are illustrated in Figs. 2, 3, 4, 5, 6 and 7. Figs. 8, 9 and 10 demonstrate the internal complete RTL schematic of the 4×4 and 6×6 and 8×8-bit Robertson's multipliers. The part of internal RTL schematic of Robertson's 12×12, 16×16 and 32×32-bit multipliers are shown in Figs. 11, 12 and 13. Tables 1-2 summarize the FPGA device resources utilization for Robertson's 4×4, 6×6, 8×8, 12×12, 16×16 and 32×32-bit multipliers. FPGA resource utilization for four input look up table (LUTs), occupied slices, total equivalent gate count and delay have been gradually increased for Spartan-3 and Virtex-5 devices. The values obatined for bonded IOBs are similar to Robertson's 4×4, 6×6, 8×8, 12×12, 16×16 and 32×32-bit multipliers in Spartan-3 and Virtex-5 FPGA devices. The Virtex-5 FPGA shows less use of embedded resourses for LUTs, occupied slices and total equivalent gate count as compared to Spartan-3 FPGA. The delay in Virtex-5 is reduced remarkably, from 6.145 ns to 35.826 ns for 4×4-bit multiplier to 32×32-bit multiplier as compared to Spartan-3 from 14.958 ns to 90.720 ns for 4×4-bit multiplier to 32×32-bit multiplier. The delay value obtained for 8×8 bit is 29.674 ns for Spartan-3, which is lower than the value 34.933 ns as reported in Spartan-3 FPGA [16]. Even Virtex-5 FPGA demonstrates less value for 8×8 bit multiplier which is 10.972 ns.

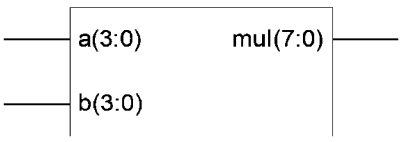

Fig. 2: The 4×4-bit Robertson's multiplier block diagram.

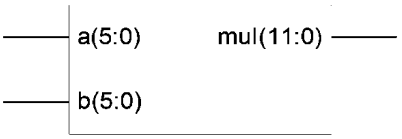

Fig. 3: The 6×6-bit Robertson's multiplier block diagram

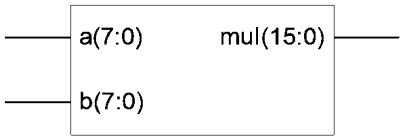

Fig. 4: The 8×8-bit Robertson's multiplier block diagram

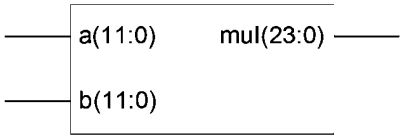

Fig. 5: The 12×12-bit Robertson's multiplier block diagram

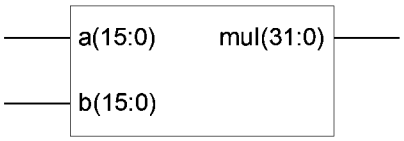

Fig. 6: The 16×16-bit Robertson's multiplier block diagram

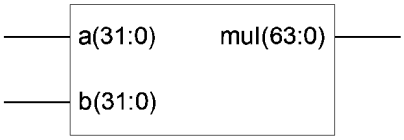

Fig. 7: The 32×32-bit Robertson's multiplier block diagram

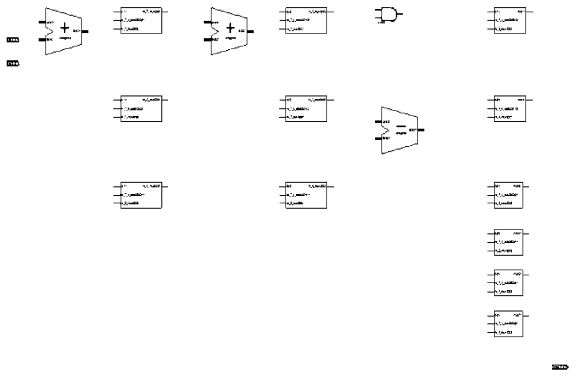

Fig. 8: The 4×4-bit Robertson's multiplier complete RTL schematic

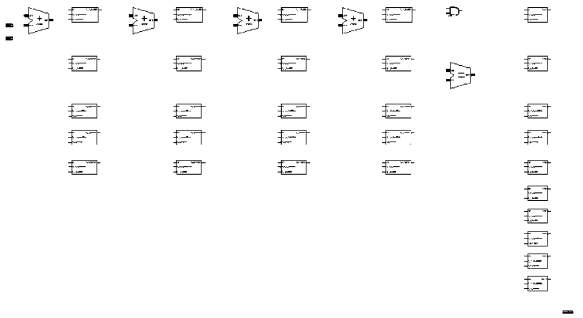

Fig. 9: The 6×6-bit Robertson's multiplier complete RTL schematic

Table 1: FPGA resource utilization for Robertson's multiplier for Spartan-3 XC3S400 (Package: pq208, speed grade:-5)

Bit Width	Four Input LUTs (7168)	Occupied Slices (3584)	Bonded IOBs (141)	Total Equivalent Gate Count	Delay (ns)
4×4	12	23	16	159	14.958
6×6	32	64	24	552	24.273
8×8	60	118	32	1032	29.674
12×12	139	274	48	2424	39.837
16×16	250	494	64	4392	49.992
32×32	1014	2014	128	18024	90.720

Table 2: FPGA resource utilization for Robertson's multiplier for Virtex-5 XC5VLX50 (Package: ff676, speed grade:-3)

Bit Width	Four Input LUTs (28800)	Occupied Slices (7200)	Bonded IOBs (440)	Total Equivalent Gate Count	Delay (ns)
4×4	10	15	16	105	6.145
6×6	24	41	24	287	9.455
8×8	36	102	32	1057	10.972
12×12	66	228	48	2395	15.114
16×16	118	402	64	4261	19.257
32×32	469	1578	128	17005	35.826

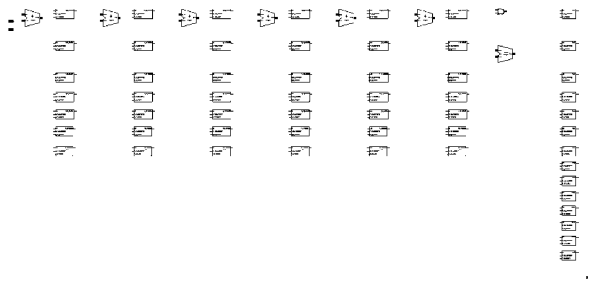

Fig. 10: The 8×8-bit Robertson's multiplier complete RTL schematic

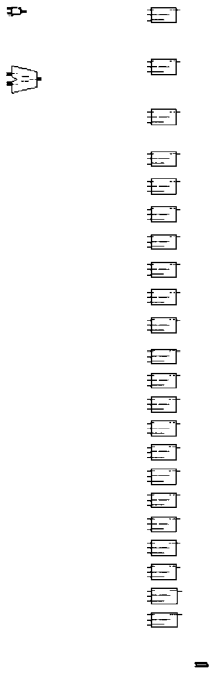

Fig. 11: The 12×12-bit Robertson's multiplier part of RTL schematic

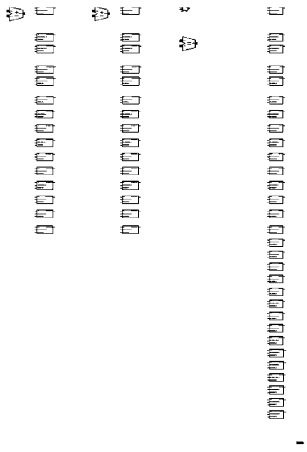

Fig. 12: The 16×16-bit Robertson's multiplier part of RTL schematic

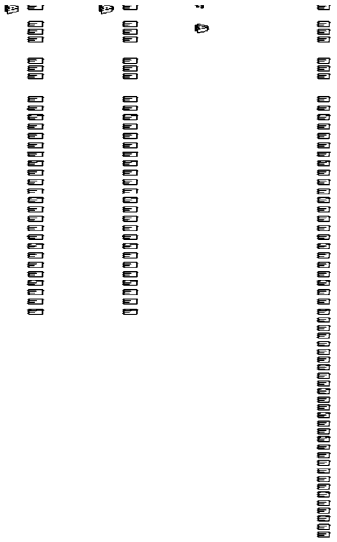

Fig. 13: The 32×32-bit Robertson's multiplier part of RTL schematic

CONCLUSION

We have presented a hardware realization of Robertson's multiplier using VHDL. The design was implemented in Xilinx Spartan-3 device XC3S400 (package: pq208, speed grade: -5) and Virtex-5 device XC5VLX50 (package: ff676, speed grade: -3) using the Xilinx ISE 9.2i design tool. FPGA resource utilization for LUTs, occupied slices, total equivalent gate count and delay have been gradually increased for Robertson's 4×4, 6×6, 8×8, 12×12, 16×16 and 32×32-bit multipliers for Spartan-3 and Virtex-5 devices. The values obatined for bonded IOBs are similar for Robertson's 4×4, 6×6, 8×8, 12×12, 16×16 and 32×32-bit multipliers in Spartan-3 and Virtex-5 FPGA devices. The Virtex-5 FPGA shows less use of embedded resourses for LUTs, occupied slices and total equivalent gate count as compared to Spartan-3 FPGA. The delay in Virtex-5 is reduced remarkably, from 6.145 ns to 35.826 ns for 4×4-bit multiplier to 32×32-bit multiplier as compared to Spartan-3 from 14.958 ns to 90.720 ns for 4×4-bit multiplier to 32×32-bit multiplier.

ACKNOWLEDGMENT

The authors extend their appreciation to the College of Applied Medical Sciences Research Center and the Deanship of Scientific Research at King Saud University for funding this research.

REFERENCES

1. Rais, M.H., 2009. Efficient hardware realization of truncated multipliers using FPGA, World Academy of Science, Engineering and Technology, 33: 741-745. http://www.waset.org/journals/waset/v33/v33-126.pdf
2. Rais, M.H. and M.H. Al Mijalli, 2011. Braun's multipliers: Spartan-3AN based design and implementation, J. Comput. Sci., 7(11): 1629-1632.
3. Rais, M.H., 2010. Hardware design and implementation of fixed-width standard and truncated 4×4, 6×6, 8×8 and 12×12-bit multipliers using FPGA, in AIP Conference Proceedings, 1239: 192-196.
4. Al-Qadi, Z. and M. Aqel, 2009. Performance Analysis of Parallel Matrix Multiplication Algorithms Used in Image Processing, World Applied Sciences Journal, 6(1): 45-52.
5. Asadi, P. and K. Navi, 2007. A New Low Power 32×32- bit Multiplier, World Applied Sciences Journal, 2(4): 341-347.
6. Juang, T.B. and S.F. Hsiao, 2005. Low-error carry-free fixed-width multipliers with low-cost compensation circuits, IEEE Transactions on Circuits and Systems II, 52(6): 299-303.
7. Al-Mijalli, M.H., 2011. Spartan-3AN field programmable gate arrays truncated multipliers delay study, Am. J. Applied Sci., 8(6): 554-557.
8. Al Mijalli, M.H., 2011. FPGA Based Truncated Multipliers: A Study of Latency in FPGA Devices, European J. Sci. Res., 60(2): 273-279.
9. Rais, M.H. and M.H. Al Mijalli, 2011. Reconfigurable Design and Implementation of Standard and Truncated Multipliers Using Spartan-3AN, Spartan-3E, Virtex-2 and Virtex-4 FPGAs, European J. Sci. Res., 60(3): 469-481.
10. Rais, M.H. and M.H. Al Mijalli, 2011. FPGA Based Fixed Width 4×4, 6×6, 8×8 and 12×12-Bit Multipliers using Spartan-3AN, Int. J. Comput. Sci. Network Security, 11(2): 61-68.
11. Rais, M.H. and M.H. Al Mijalli, 2012. Virtex-5 based Delay study and Realization of Braun's Multipliers, World Applied Sciences Journal, 18(9): 1285-1290.
12. Al Mijalli, M.H., 2012. Spartan-3A FPGA Implementation, World Applied Sciences Journal, 18(9): 1291-1295.
13. Xilinx, Spartan-3 FPGA Family Datasheet, 2008. http://www.xilinx.com/support/documentation/data_sheets/ds099.pdf
14. Xilinx, Virtex-5 FPGA Family Datasheet, 2009. http://www.xilinx.com/support/documentation/data_sheets/ds100.pdf
15. Xilinx, ISE 9.2i Design Tool, (2007). www.xilinx.com/prs_rls/2007/software/0786_ise92i.htm
16. Mishra, R.S., P. Gour and B.B. Soni, 2011. Design and Implementations of 8×8 bit Booth and 8×8 bit Robertson's multiplier algorithm on FPGA, Global Journal of Computer Application and Technology, 1(3): 399-402.