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Delay Study of Spartan-3A Field Programmable Gate Array

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Abstract: The purpose of delay study is to evaluate Spartan-3A family devices and determine the significance and the extent of delay among the devices for Braun's multipliers. Braun's multipliers hardware implementation on Spartan-3A field programmable gate array (FPGA) devices including: XC3S50A, XC3S200A, XC3S400A, XC3S700A and XC3S1400A using Very High speed integrated circuit Hardware Description Language (VHDL). The delay study is analysed using analysis of variance (ANOVA) method applying the software Statistical Package for Social Science (SPSS) with a 0.05 confidence level. Delay results comparison test show that the differences between the FPGA Spartan-3A devices are insignificant.

Key words: Braun's Multipliers · Delay Study · Field Programmable Gate Array (FPGA) · Spartan-3A

INTRODUCTION

Field Programmable Gate Array (FPGA) devices could be evaluated using delay study. Numerous multiplication operations are generally required in digital signal processing (DSP) and in its subfields. Microprocessor has been used as a mean for DSP applications, but their performances fall short for many applications. So far Application Specific Integrated Circuits (ASICs) designs were used as an alternative to microprocessors. Recent development in FPGA performance and size offer a new hardware acceleration opportunity.

A number of research efforts have so far been reported in literature in order to achieve hardware efficient realization of parallel multipliers [1-4] and their relevant delay studies [5-8].

The goal of this study is to present the extent of delay among Spartan-3A FPGA devices. For this purpose, Braun's multipliers implemented on Spartan-3A including: XC3S50A, XC3S200A, XC3S400A, XC3S700A [3] and XC3S1400A FPGA devices. The statistical evaluation effect of Braun's multipliers delays in Spartan-3A FPGA devices was carried out using analysis of variance (ANOVA) and post hoc Tukey's test applying the Statistical Package for Social Science (SPSS).

MATERIALS AND METHODS

FPGAs are programmable hardware implementation devices. FPGA configuring the hardware to perform the necessary operation for a particular design, where processing engine controlled operation by scheduling in microprocessor design. The algorithms for architecture, those require extensive amount of parallelism and speedup in computation is easily offered by FPGAs hardware implementation. The necessities of high volume require a economical electronic system which is offered by Spartan-3 FPGA [9].

Braun's Multipliers and its Mathematical Basis: Braun's multiplier is generally known as carry save multiplier and is constructed with $m\times$ (n-1) adders and $m\times n$ AND gates is shown in Fig. 1. In Braun's multiplier each product is generated in parallel with the AND gates. The row of adders produces sum of partial product added to the each partial product. The carry out shifted one bit to the left or right and then it is added to the sum generated by the first adder and the newly generated partial product. The shifting is carried out with the help of Carry Save Adder (CSA) and the Ripple Carry Adder (RCA). The RCA is used instead of CSA in the last stage of the Braun's multiplier. As a result of RCA Braun's multiplier possess a glitching problem.

The multiplication of two unsigned numbers such as,

$$Y = \sum_{i=0}^{m-1} Y_i 2^i$$

$$X = \sum_{i=0}^{n-1} X_i 2^i$$

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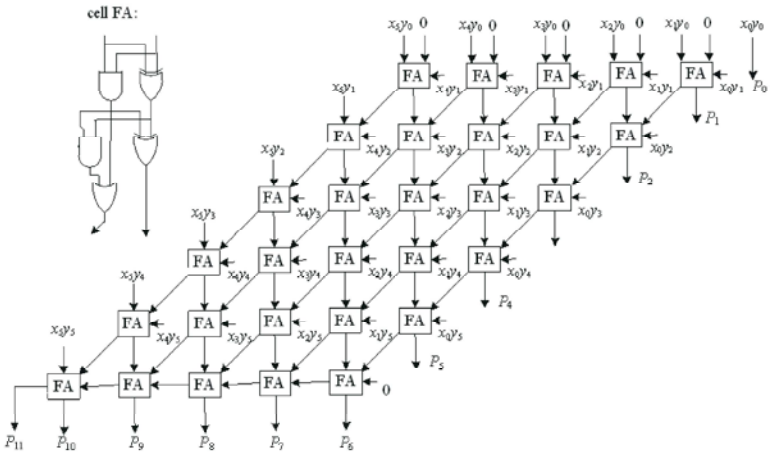

Fig. 1: The 6×6-bit Braun's multiplier architecture

We obtained following equation, which results from multiplying the multiplicand *Y* by the multiplier *X*,

$$P = \sum_{i=0}^{m-1}\sum_{j=0}^{n-1}(Y_i.X_j)2^{i+j}$$

RESULTS

Implementation and Delay: The design of Braun's multipliers is done using VHDL and implemented in a Xilinx Spartan-3A FPGA family; devices including XC3S50A (package: tq144, speed grade: -5), XC3S200A (package: ft256, speed grade: -5), XC3S400A (package: fg400, speed grade: -5), XC3S700A (package: fg484, speed grade: -5), [3] and XC3S1400A (package: fg676, speed grade: -5) using the Xilinx ISE 9.2i design tool [10]. A one-way ANOVA is applied to compare the mean delay time for five Spartan-3A FPGA devices. The delay time for these devices is calculated using four Braun's multipliers 4×4, 6×6, 8×8 and 12×12. Furthermore, the statistical analysis is done by using SPSS program.

Table 1: Statistics of latency in Braun's multipliers for FPGAs

FPGA Devices	Bit Width	Mean (ns)	Std. Deviation (ns)	Std. Error of Mean (ns)
XC3S50A	4×4	9.40	1.2042	0.5385
	6 ×6	13.04	0.5079	0.2272
	8×8	13.90	1.0149	0.4539
	12×12	20.00	0.8307	0.3715
XC3S200A	4×4	9.82	1.0710	0.4790
	6 ×6	12.22	1.0354	0.4630
	8×8	14.80	0.7348	0.3286
	12×12	19.50	0.4062	0.1817
XC3S400A	4×4	10.86	0.4278	0.1913
	6 ×6	12.24	1.0574	0.4729
	8×8	15.64	0.2074	0.0927
	12×12	19.42	0.6181	0.2764
XC3S700A	4×4	12.20	0.7106	0.3178
	6 ×6	12.56	0.4506	0.2015
	8×8	16.86	1.6196	0.7243
	12×12	20.16	2.4916	1.1143
XC3S1400A	4×4	12.66	1.0164	0.4545
	6 ×6	12.18	1.1411	0.5103
	8×8	17.66	0.6504	0.2909
	12×12	21.64	0.3847	0.1720

DISCUSSION

Table 1 summarizes the statistics of delay in Braun's multipliers for XC3S50A, XC3S200A, XC3S400A, XC3S700A and XC3S1400A Spartan-3A FPGAs.

Table 2 shows the ANOVA results on Spartan-3A including: XC3S50A, XC3S200A, XC3S400A, XC3S700A and XC3S1400A FPGA devices. There is a statistically insignificant difference at the 0.05 level in delay time for the five devices [F (4, 95) = 1.051, p = .385] compared by using ANOVA and post-hoc Tukey HSD multiple comparison tests at the 0.05 significance level. The test indicates that the mean of delay time for XC3S50A (Mean = 14.085, Standard Deviation = 4.00) is insignificantly different from the other device; XC3S200A (Mean = 14.085, Standard Deviation = 3.76), XC3S400A (Mean = 14.540, Standard Deviation = 3.45), XC3S700A (Mean = 15.445, Standard Deviation = 3.65) and XC3S1400A (Mean = 16.035, Standard Deviation = 4.059). However, there are statistically insignificant difference in mean delay times of the devices obtained, which clearly indicates that the Spartan-3A FPGA devices demonstrates equal behaviour.

Table 2: The results of multiple comparisons of delay time (ns) for five devices using the Tukey's HSD post-hoc test

					95% Confidence Interval	
(I) Devices	(J) Devices	Mean Difference (I-J)	Std. Error	Sig.	Lower Bound	Upper Bound
XC3S50A	XC3S200A	0.00000	1.19920	1.000	-3.3348	3.3348
	XC3S400A	-0.45500	1.19920	0.996	-3.7898	2.8798
	XC3S700A	-1.36000	1.19920	0.788	-4.6948	1.9748
	XC3S1400A	-1.95000	1.19920	0.485	-5.2848	1.3848
XC3S200A	XC3S50A	0.00000	1.19920	1.000	-3.3348	3.3348
	XC3S400A	-0.45500	1.19920	0.996	-3.7898	2.8798
	XC3S700A	-1.36000	1.19920	0.788	-4.6948	1.9748
	XC3S1400A	-1.95000	1.19920	0.485	-5.2848	1.3848
XC3S400A	XC3S50A	0.45500	1.19920	0.996	-2.8798	3.7898
	XC3S200A	0.45500	1.19920	0.996	-2.8798	3.7898
	XC3S700A	-0.90500	1.19920	0.943	-4.2398	2.4298
	XC3S1400A	-1.49500	1.19920	0.724	-4.8298	1.8398
XC3S700A	XC3S50A	1.36000	1.19920	0.788	-1.9748	4.6948
	XC3S200A	1.36000	1.19920	0.788	-1.9748	4.6948
	XC3S400A	0.90500	1.19920	0.943	-2.4298	4.2398
	XC3S1400A	-0.59000	1.19920	0.988	-3.9248	2.7448
XC3S1400A	XC3S50A	1.95000	1.19920	0.485	-1.3848	5.2848
	XC3S200A	1.95000	1.19920	0.485	-1.3848	5.2848
	XC3S400A	1.49500	1.19920	0.724	-1.8398	4.8298
	XC3S700A	0.59000	1.19920	0.988	-2.7448	3.9248

Table 3: FPGA resource utilization for standard Braun's multiplier for Spartan-3A XC3S1400A (Package: fg676, speed grade:-5)

Bit Width	Multipliers	Four Input LUTs (22528)	Occupied Slices (11264)	Bonded IOBs (502)	Total Equivalent Gate Count	Average Connection delay (ns)	Maximum Pin delay (ns)
4×4	Standard	32	17	16	192	1.335	4.105
6×6	Standard	75	40	24	450	0.700	2.535
8×8	Standard	133	69	32	798	1.389	4.355
12×12	Standard	295	152	48	1770	1.533	4.491

Table 3 demonstrates the implementation results of Spartan-3A XC3S1400A FPGA, which shows the same values for four input LUTs, occupied slices, bonded IOBs and total equivalent gate count, as have been observed for Spartan-3A XC3S50A, XC3S200A, XC3S400A and XC3S700A FPGAs [3]. The only difference is seen in average connection delay and in maximum pin delay. The same trend has been observed in Spartan-3A XC3S50A, XC3S200A, XC3S400A and XC3S700A FPGAs [3].

CONCLUSION

A delay study is presented of Spartan-3A FPGA based parallel architecture for standard Braun's multipliers using VHDL. The Braun's multipliers were implemented on Xilinx Spartan-3A XC3S50A (package: tq144, speed grade: -5), XC3S200A (package: ft256, speed grade: -5), XC3S400A (package: fg400, speed grade: -5), XC3S700A (package: fg484, speed grade: -5) and XC3S1400A (package: fg676, speed grade: -5) using the Xilinx ISE 9.2i design tool.

There is a statistically insignificant difference at the 0.05 level in delay time for the five devices compared by using ANOVA and post-hoc Tukey HSD multiple comparison tests at the 0.05 significance level, which indicates that the Spartan-3A FPGA devices demonstrates similar behaviour.

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