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A Novel Cascaded Multilevel Inverter Using Mcpwm with Minimum Switches

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Abstract: Multilevel inverter present attractive advantages in high power applications. A multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy sources. The proposed method is 15-level multilevel inverter which has number of modules are connected in series. Each module has one switch and one parallel connected diode. Only one switch operates at a time preventing short circuit. This method involves less number of switches associated with more number of voltage levels. The stages with higher DC link have more advantages like low commutation, reduced switching losses, increased efficiency and low input stages with more number of output levels. In this paper, a bypass diode technique is introduced to the conventional cascade multilevel inverter topology which reduces the number of controlled switches used in the system. It dramatically reduces the switches for high number of levels that reduces the switching losses; cost and low order harmonics and thus effectively reduces Total Harmonic Distortion (THD).

Key words: Cascaded multilevel inverter · H-bridge inverter · Total Harmonics Distortion

INTRODUCTION

Numerous industrial applications require high power apparatus in recent years. The utility applications require medium voltage and MW power level. For a medium voltage grid, it is troublesome to connect single power semiconductor switch directly [1, 2]. The applications of ac variable frequency speed regulations are widely popularized. High power and medium voltage inverter has recently become a research focus but there are many problems associated with conventional two level inverter. Multilevel inverter have been gained more attention for high power application in recent years which can operate at high switching frequencies while producing lower order harmonic components [3, 4]. A multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy sources. There are several topologies such as neutral point clamped or diode clamped multilevel inverter, flying capacitor based multilevel inverter, cascaded H-bridge multilevel inverter and hybrid H-bridge multilevel inverter. The main disadvantage of diode clamped multilevel inverter topology is restriction to the high power operation. The first topology introduced is the series H-bridge design [5, 6], in which several configurations have been obtained. This topology consists of series power conversion cells which form the cascaded H- bridge multilevel inverter and power levels may be scaled easily. An apparent disadvantage of this topology is the requirement of large number of isolated voltage sources. The proposed topology for multilevel inverter has high number of steps associated with low number of power switches. In addition, for producing the levels at the output voltage, a procedure for calculating the required dc voltage source is proposed.

Hybrid Multilevel Inverter: The general structure of the hybrid multilevel inverter for single phase is shown in Figure 1. Each H-bridge circuit is connected in series associated with it. Each of the circuit consists of four active switching elements that can make the output voltage as positive or negative polarity; or it can be simply zero volts depending on the switching condition of the switches in the circuit. A conventional multilevel inverter topology employs multiple/link voltage of equal magnitudes. It is fairly easy to generalize the number of distinct levels [7, 8].

The S may be number of stages or dc sources and the associated number output level can be written as follows:

$$N \text{ level} = 2S+1 \quad (1)$$

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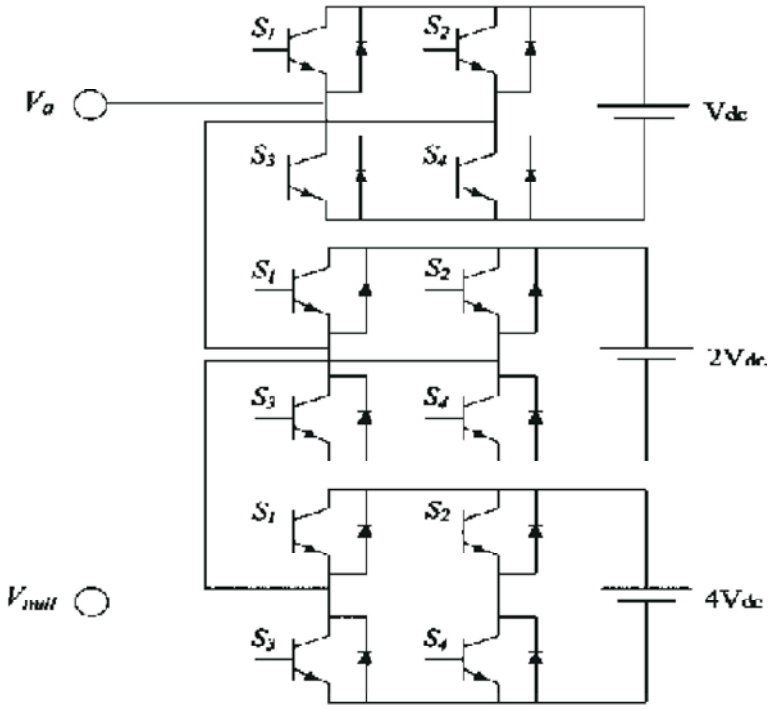

Fig. 1: Topology for Hybrid Multilevel Inverter

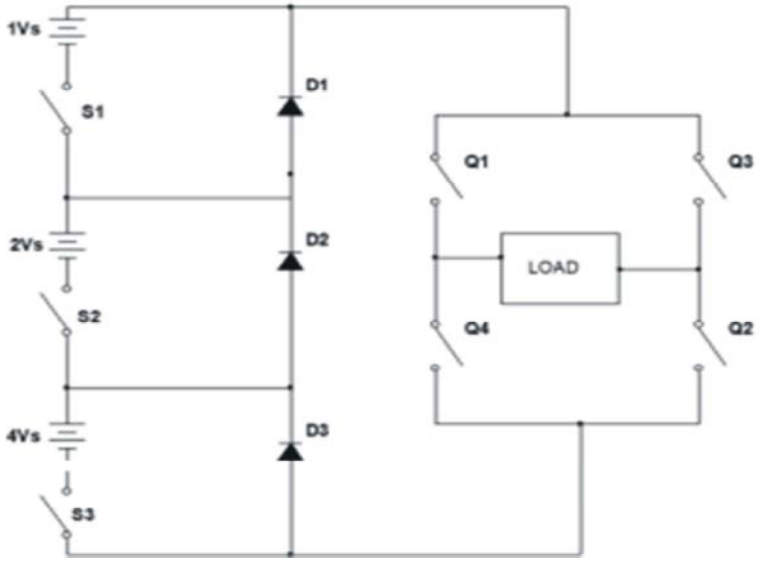

Fig. 2: Topology for Cascade Multilevel Inverter

The number of switches used in this topology is expressed as,

N switch=4 S (2)

The advantage of the hybrid multilevel inverter is modularized structure. This will enable the manufacturing process to be done more quickly and cheaply. The drawback of this topology needs a separate dc source for each of the H-bridges and involves high number of semiconductor switches.

Proposed Method

Cascaded Multilevel Inverter: The proposed multilevel inverter has a general structure of the cascade multilevel inverter is shown in Figure 2. Each of the separate voltage

Table 1: Basic Operation of Modified Hybrid Multilevel Inverter

S.NO	Intervals	On switches	Off switches	Voltage levels	Current flow path
1	I	S1	S2, S3	+1Vs	S1, D2, D3
2	II	S2	S1, S3	+2Vs	S2, D1, D3
3	III	S1, S2	S3	+3Vs	S1, S2, D3
4	IV	S3	S1, S2	+4Vs	D1, D2, D3
5	V	S1, S3	S2	+5Vs	S1, D2, D3
6	VI	S2, S3	S1	+6Vs	D1, S2, S3
7	VII	SI, S2, S3	-	+7Vs	S1, S2, S3
8	VIII	-	S1, S2, S3	0	D1, D2, D3

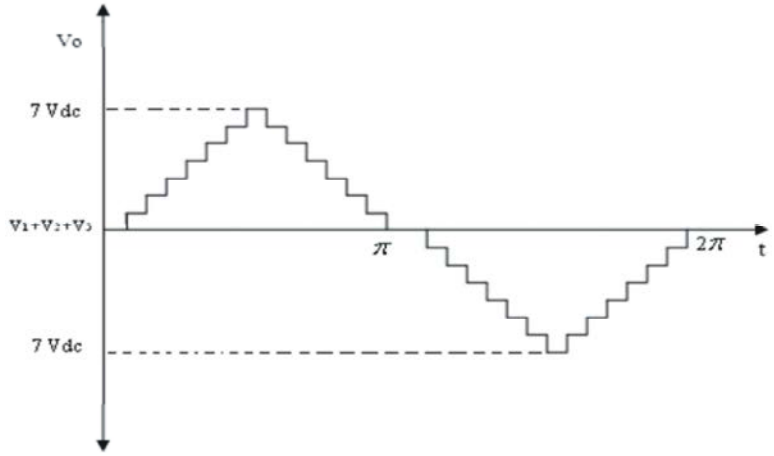

Fig. 3: Typical output waveform for Cascaded Multilevel Inverter

source (1Vs, 2Vs, 4Vs) is connected in series with other sources via a special circuit associated with it. Each stage of the circuit consists of only one active switching element and one bypass diode that make the output voltage as positive one with several levels. The basic operation of modified cascaded multilevel inverter for producing the output voltage as +1Vdc is to turn on the switch S1 (S2 and S3 turn off) and turning on S2 (S1 and S3 turn off) for producing output voltage as +2Vdc. Similarly other levels can be achieved by turning on the suitable switches at particular intervals; Table 1 shows the basic operation of proposed hybrid multilevel inverter. From the table it can be inferred that only one H-bridge is connected to get both positive and negative polarity.

The main advantage of cascaded H-bridge multilevel inverter is high number of levels with reduced number of switches.

The S number of dc sources or stages and the associated number output level can be calculated by using the equation

$$N\ level = 2S+1-1 \quad (3)$$

Voltage on each stage can be calculated by using the equation.

$$V = 2S-1.Vdc \quad (4)$$

The number of switches used in this topology is given by the equation.

$$N\ switch = S+4 \quad (5)$$

The Figure 3 shows the typical output voltage waveform of a 15-level cascaded multilevel inverter with 3 separate dc sources.

Total Harmonic Distortion (THD): The Total Harmonic Distortion block measures the Total Harmonic Distortion (THD) of a periodic signal. The signal can be voltage or current. The THD is defined as the ratio of Root Mean Square (RMS) value of the total harmonics of the signal to the RMS value of its fundamental signal. The THD value will be zero for a pure sinusoidal voltage or current. For example, for currents, the THD is defined as.

Total Harmonic Distortion (THD) = Ih / In

where Ih = I22+ I32+…+ In2), In=RMS value of the harmonic ‘n’, If= RMS value of the fundamental current.

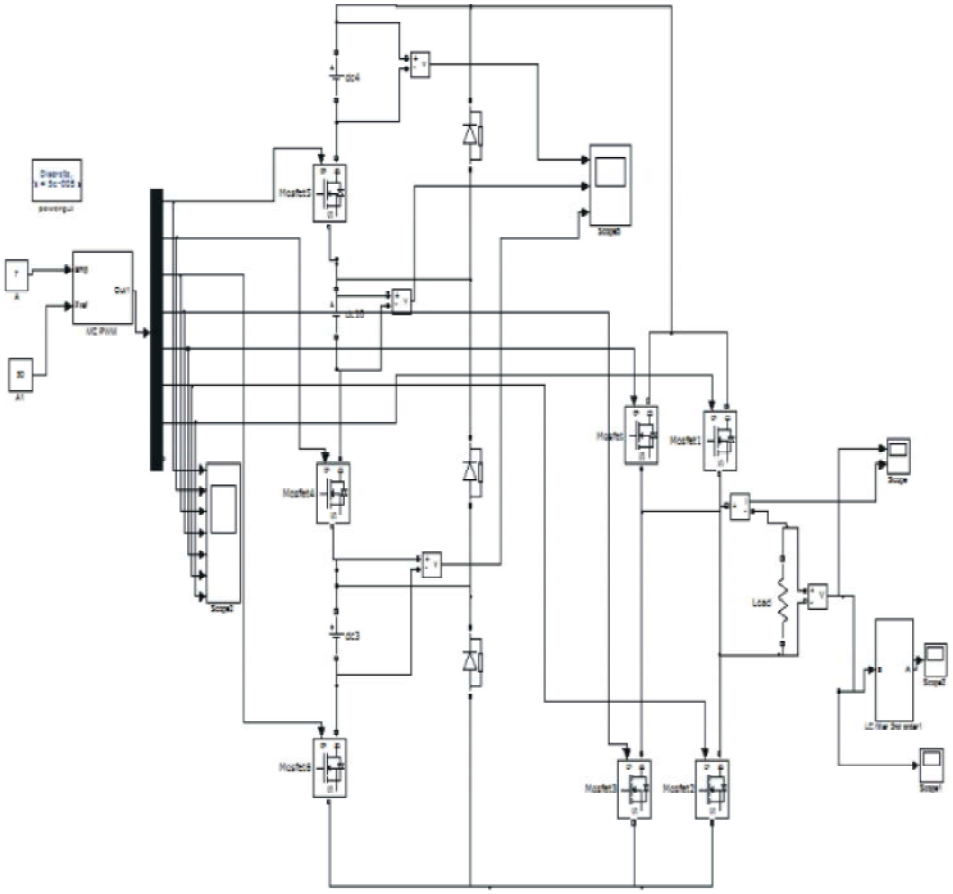

Fig. 4: Simulation Diagram of Proposed System

Simulation Models

Simulation Model of Proposed System: The simulation model of proposed system is shown in the Figure 4. The 15-level cascaded multilevel inverter has been developed using MATLAB. The proposed method is used to get sinusoidal waveform and reduced harmonics with minimum number of components. Therefore the efficiency of the cascaded multilevel inverter is increased. The low order harmonics are reduced significantly. This is used to produce the unidirectional output in both positive and negative directions [9].

RESULTS AND DISCUSSION

The simulation results and analysis of 15-level cascaded multilevel inverter with reduced number of switches is shown below. It describes the output voltage waveform and output current waveform with R load.

The output voltage for CMLI with R load is shown in the Figure 5. It has 15 levels. The cascaded multilevel inverter output waveform has different levels of voltage like 24V, 48V, 96V in both polarities. It can be achieved by selection of switching pattern. The fundamental frequency of CMLI is 50Hz.

The output current for the R load is shown in the Figure 6. It has drawn between the time and current.

The modified hybrid multilevel inverter FFT analysis is shown in the Figure 7 for R load. Analysis of THD (Total Harmonic Distortion) plays a major role in case of inverters.

Cascaded multilevel inverters with many dc sources while minimizing several harmonics. In this cascaded multilevel inverter due to their high efficiency, low switching losses and low electromagnetic interference. Overall, MCPWM is a good fitness evaluation to cascaded multilevel inverter, for flow measurement and control applications. Justification of the system shown in Table 2. From all the above discussions we can conclude that MCPWM has better harmonic minimization and fast response.

Table 2: Justification of the System

S.No	Contents	Existing system	Proposed system
1	Level of Inverter	9 level	15 Level
2	Technique	SOP	MCPWM
3	THD level	3.65	1.65
4	Efficiency	97%	98%

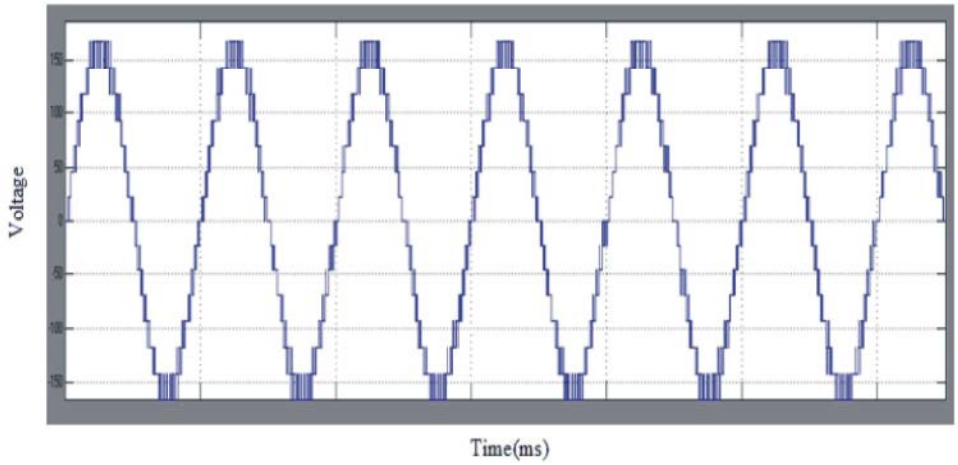

Fig. 5: Output Voltage Waveform of cascaded MLI for R-load

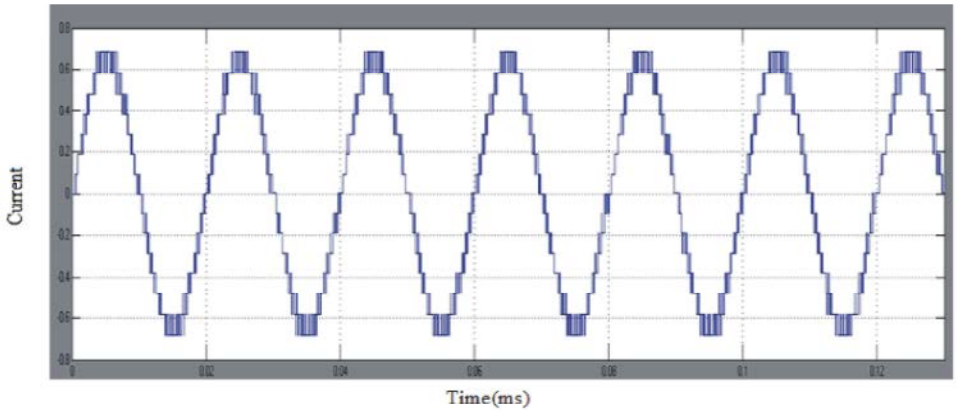

Fig. 6: Output Current Waveform of cascaded MLI with R-load

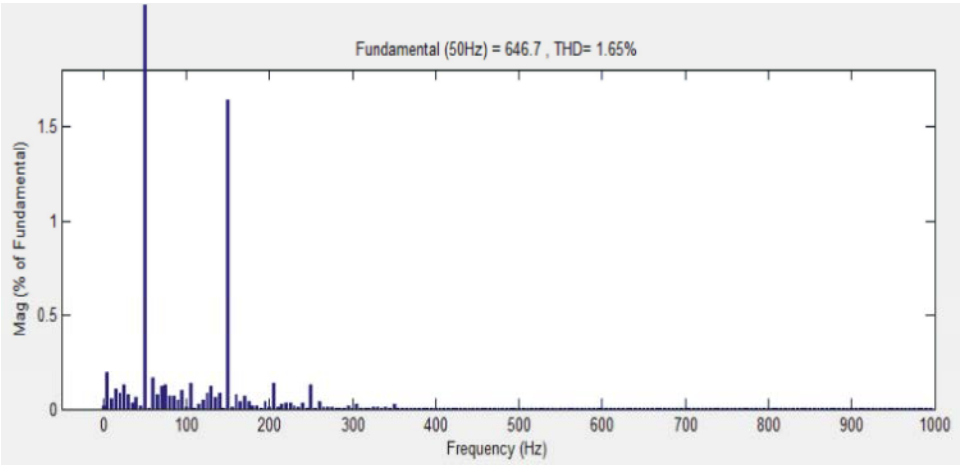

Fig. 7: Spectrum Analysis of Total Harmonic Distortion for CMLI with R-load

CONCLUSION

Cascaded multilevel inverter using MCPWM is proposed. The proposed system achieves high output voltage and reduced number of switches. MCPWM technique used here increase the efficiency and decreases the harmonics. Cascaded multilevel inverter along with MCPWM makes the system is healthier. The system of fifteen level cascaded multilevel inverter can be further enhanced to real time application and implementation of software will extend to hardware.

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