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Three Phase 15 Level Cascaded H-Bridges Multilevel Inverter for Motor Drives

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Abstract: In this paper, the structure for three phase H-bridge cascaded power converters is presented. Large electrical drives and utility application require advanced power electronics Converter to meet the high power demands. As a result, multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. It is shown that the inverter can simultaneously maintain the dc voltage level and choose a SPWM switching pattern to produce a free harmonic sinusoidal output. HCMLI using only a single dc source for each phase is promising for high-power motor drive applications as it significantly decreases the number of required dc power supplies, provides high-quality output power due to its high number of output levels and results in high conversion efficiency. The proposed multilevel converter not only achieves high power rating but also improves the performance of the whole system in terms of harmonics. In this paper the proposed inverter can output more numbers of voltage levels with the advanced switching pattern. Finally, the simulation and experimental results validate the concept of this new topology.

Key words: H-Bridge multilevel inverter · Total Harmonic Distortion · 15-Level inverters · SPWM

INTRODUCTION

Numerous industrial applications have begun to require high power application in recent years. Power electronic inverter become popular for various industrial drives and motor drive applications. The electrical industries have expanded and the variety of loads has increasingly grown. Recently, the industry has begun to apply high-voltage high-power equipment that has reached the megawatt range. Today, the direct connection of a single semiconductor switch to a system with Medium sized voltage grids will create problem. To overcome this problem, a multilevel inverter topology has been introduced as an alternative solution for medium voltage and high power situations. A multilevel inverter use renewable energy as source and can achieve high power rating. So, renewable energy sources such as solar, fuel cells and wind can be easily interfaced to a multilevel inverter structure for a high power application. The multilevel inverter concept has been used since past three decades. The multilevel inverter begins with a three-level inverter. Thereafter, many multilevel inverter topologies have been developed. However, the main concept of a multilevel inverter is to achieve high power with use of many power semiconductor switches and numerous low voltage dc sources to obtain the power conversion that lookalike a staircase voltage waveform. The dc voltage sources for multilevel inverter are given by battery, renewable energy and capacitor voltage sources. The proper switching of the power switches combines these multiple dc sources to achieve high power output voltage. The voltage rating of the power semiconductor devices depends only upon the total peak value of the dc voltage source that is connected to the device. There are different types of multilevel circuits involved to improve the efficiency of the Multilevel Inverter. The multilevel inverters are mainly classified as diode clamped, Flying capacitor inverter and cascaded multilevel inverter. The cascaded multilevel control method is very easy when compare to other multilevel inverter because it doesn't require any clamping diode and flying capacitor.

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Recently, multilevel power conversion technology has been developing the area of power electronics very rapidly with good potential for further developments. A multilevel converter not only achieves high power rating, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind and fuel cells can be easily interfaced to a multilevel converter system for a high power application.

In this paper, we are using a new topology of three phase H-bridge 15-Level inverter for producing lower harmonic distortion. The main objective of this paper is to design a efficient multilevel inverter with reduced harmonics in the output waveform using matlab/simulink. The proposed system introduces the series H-bridge design with dc sources. The higher number of output voltage levels have the ability to synthesize waveforms with a better harmonic spectrum. This will improve the efficiency of the system and reduce the harmonics present in the system. These designs can create higher power quality for a given number of semiconductor devices than the fundamental topologies alone due to a multiplying effect of the number of levels.

Previous Research: Numerous related research works are already existed in literature which based on multilevel converter of the system. Some of them are reviewed here [1-4].

Zhong Du*, et al*. [5] presented a cascaded H-bridge multilevel inverter that can be implemented using only a single dc power source and capacitors. Without requiring transformers, the proposed system allows the use of a single dc power source (e.g., a battery or a fuel cell stack). Cascaded H bridge shown that the inverter can simultaneously maintain the dc voltage level of the capacitors and choose a fundamental frequency switching pattern to produce a nearly sinusoidal output. HCMLI using only a single dc source for each phase is promising for high-power motor drive applications as it significantly decreases the number of required dc power supplies, provides high-quality output power due to its high number of output levels and results in high conversion efficiency and low thermal stress as it uses a fundamental frequency switching scheme. This paper mainly discusses control of seven-level HCMLI with fundamental frequency switching control and how its modulation index range can be extended using harmonic compensation.

Ammar Masaoud *et al*.[6] introduced a new configuration of a three-phase five-level multilevel voltage-source inverter. The proposed topology constitutes the conventional three-phase two-level bridge with three bidirectional switches. A multilevel dc link using fixed dc voltage supply and cascaded half-bridge was connected in such a way that the proposed inverter outputs the required output voltage levels. The fundamental frequency staircase modulation technique was easily used to generate the appropriate switching gate signals. To increase the number of voltage levels with fewer number of power electronic components, the structure of the proposed inverter is extended and different methods to determine the magnitudes of utilized dc voltage supplies are suggested. Moreover, the prototype of the suggested configuration is manufactured as the obtained simulation and hardware results ensured the feasibility of the configuration and the compatibility of the modulation technique is accurately noted.

Rajmadhan. D *et al*. [7] Presented the application of multilevel inverter for high power equipments in industry has become popular because of its high-quality output waveform. In this paper, a three phase 11 level was proposed with reduced number of switches. An algorithm has been generated on the basis of optimized harmonic stepped waveform technique to find out firing angle for multilevel inverter to reduce harmonic content present in output. The proposed multilevel inverter has been validated using MATLAB R2009a software and firing angle was calculated using program executed by MATLAB R2009a.

John N *et al*. [8] Introduced a new topology using a single DC power source to construct a three phase five level cascade multilevel inverter to be used as a drive for a PM traction motor. The five level inverter consists of a standard three leg inverter (one leg for each phase) and an H-bridge in series with each inverter leg, which use a capacitor as a DC source. It is shown that one can simultaneously maintain the regulation of the capacitor voltage while achieving an output voltage waveform which is 25% higher than that obtained using a standard three leg inverter by itself.

Keith Corzine *et al*. [9] implemented a general structure for cascaded power converters in which any number of H-bridge cells having any number of voltage levels are series connected to form an inverter phase leg. Equations are introduced for determining an optimal voltage ratio of dc voltages for the H-bridge cells which will maximize the number of voltage levels obtainable resulting in high power quality. Special cases of the generalized inverter are presented including novel 11-level and 15-level inverters. Laboratory measurements demonstrate the proposed inverter performance.

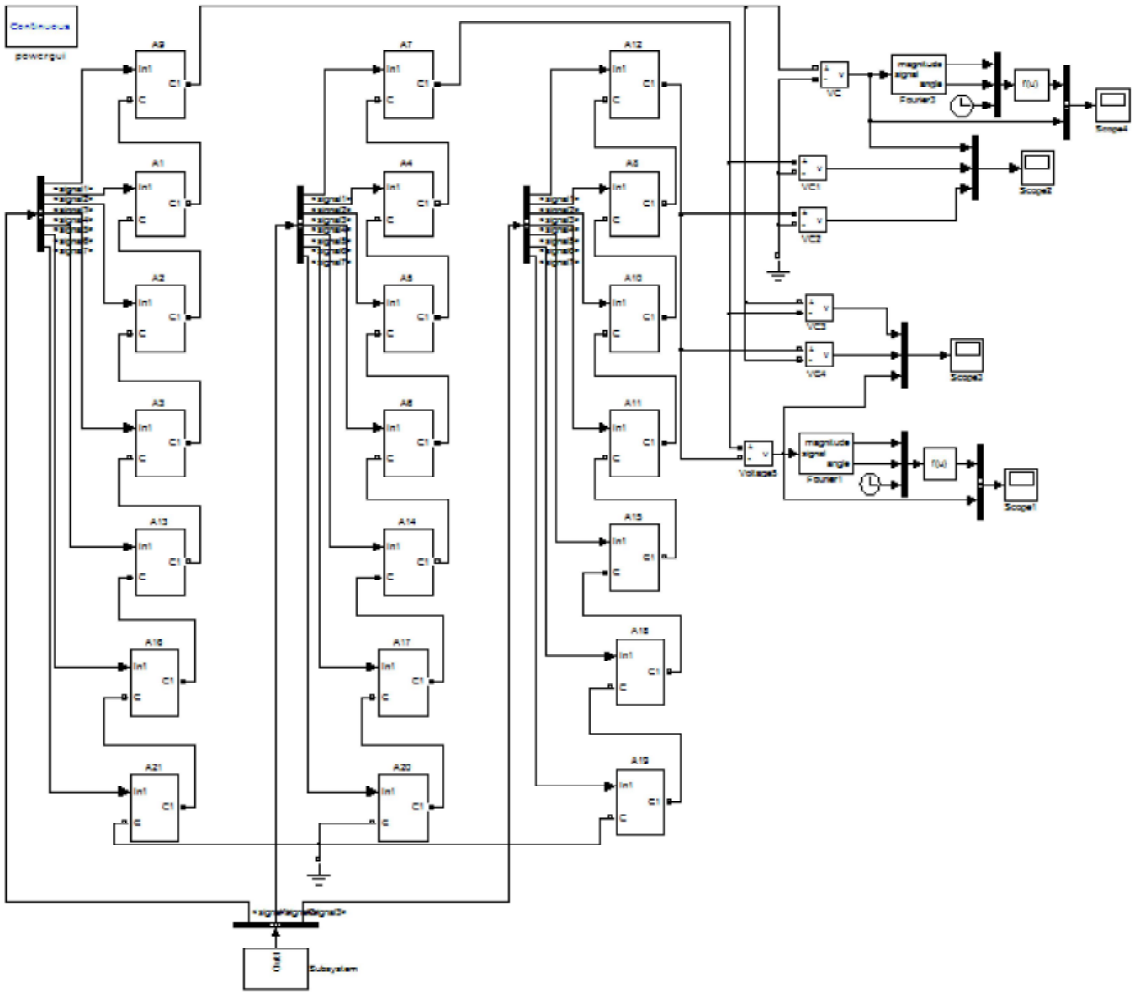

Fig. 1: Three phase 11-Level H-Bridge Cascaded multilevel inverter in MATLAB

The control goal of the HCMLI needs to maintain the balance of the dc voltage level of the capacitors while producing a nearly sinusoidal three-phase output voltage using a low switching frequency harmonic elimination method. This paper focuses on how to apply the seven-level fundamental frequency harmonic elimination method to HCMLI and extend its modulation index range and presents new findings on HCLMI control other than normal cascaded H-bridge multilevel inverters. The main advantage of this topology is that to reduce the Total Harmonic distortion present in the sinusoidal output.

Proposed Approach: The power circuit of the cascaded H-bridge multilevel inverter is illustrated in Figure 1. The inverter is composed by the series connection of power cells, each one containing an H-bridge inverter and an isolated DC source. In the particular case of asymmetric inverters these sources are not equal (V1>V2). The asymmetry of the input voltages can reduce or, when properly designed, eliminate redundant output levels, maximizing the number of different levels generated by the inverter. Therefore, this topology can achieve the same output voltage quality with less number of semiconductors, space, costs and internal fault probability than the previous topology.

A cascade multilevel inverter made up of from series connected H-bridge inverter, each with their own isolated dc bus. Each level can generate three different voltage outputs in the form of +Vdc, 0,-Vdc by connecting the dc sources to the ac output side by different combinations of the four switches. The output voltage of n level inverter is the sum of all the individual inverter outputs[10].

The simulation circuit of 15 levels Three Phase cascaded multilevel inverter using MATLAB R2009a software is shown in following Fig. 1.

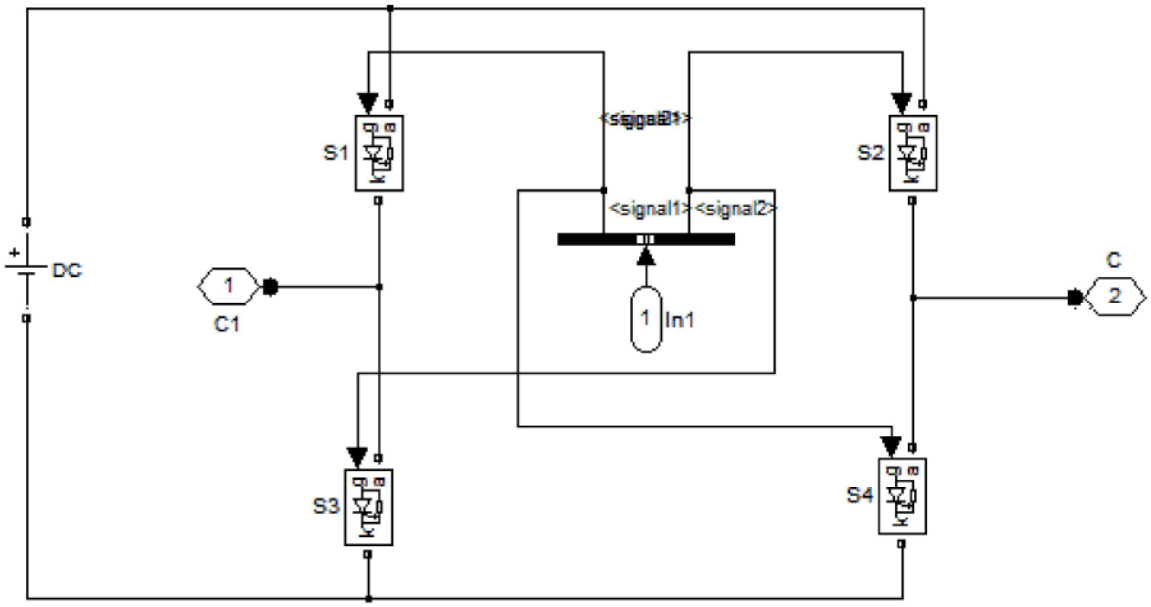

Fig. 2: Subsystem Circuit: H-Bridge multilevel inverter

Table 1: Switching Patterns for 11 levels H-Bridge inverter

	H-Bridge		
S. No	On switches	Off switches	Output Voltage Levels
1	S1,S2	S3,S4	$+6.5V_{dc}$
2	S1,S2	S3,S4	$+6V_{dc}$
3	S1,S2	S3,S4	$+5V_{dc}$
4	S1,S2	S3,S4	$+4V_{dc}$
5	S1,S2	S3,S4	$+3V_{dc}$
6	S1,S2	S3,S4	$+2V_{dc}$
7	S1,S2	S3,S4	$+1V_{dc}$
8	S1,S2	S3,S4	$0V_{dc}$
9	S3,S4	S1,S2	$-1V_{dc}$
10	S3,S4	S1,S2	$-2V_{dc}$
11	S3,S4	S1,S2	$-3V_{dc}$
12	S3,S4	S1,S2	$-4V_{dc}$
13	S3,S4	S1,S2	$-5V_{dc}$
14	S3,S4	S1,S2	$-6V_{dc}$
15	S3,S4	S1,S2	$-6.5V_{dc}$

This inverter consists of an H Bridge which consists of four separate IGBT switches and DC voltage source in each cell. Each source connected with H-Bridge circuit which consists four IGBT switches and bus that can make the output voltage for 15-Level.Only one H-bridge is connected with cells to acquire both positive and negative polarity. Each cell in the above inverter contains the subsystem of H-Bridge inverter shown in Figure-2. The subsystem circuit of each cell is shown in below.

By turning on controlled switches S1 (S2, S3 and S4 turn off) the output voltage +100Vdc (first level) is produced across the load. Similarly turning on of switches S1, S2 (S3 & S4 turn off) +2Vdc (second level) output is produced across the load. Similarly +5Vdc levels can be achieved by turning on S1, S2, S3 switches (S4 turn off) and +4Vdc levels can be achieved by turning on S1, S2, S3 & S4 as shown in below Table 1.

From the below table, it is observed that for each voltage level, among the paralleled switches only one switch is switched ON. The input DC voltage is converted into a stepped DC voltage, by the multi conversion cell, which is further processed by the H Bridge and outputted as a stepped or approximately sinusoidal AC waveform. In the H Bridge, during the positive cycle, only the switches S1 and S3 are switched on. And during the negative half cycle, only the switches S2 and S4 are switched on. The S number of DC sources or stages and the associated number output level can be calculated by using the equation as follows,

$$N_{level} = 2S+1 \quad (1)$$

For an example, if S=3, the output wave form will have seven levels (±3Vdc,±2Vdc, ±1Vdc and 0). Similarly voltage on each stage can be calculated by using the equation as given,

$$A_i = 1\ V_{dc}(1, 2, 3) \quad (2)$$

The main advantage of proposed H-bridge multilevel inverter is 15-Levels with the use of eight cells. For an example, if S=8, the output wave form will have 15-Levels

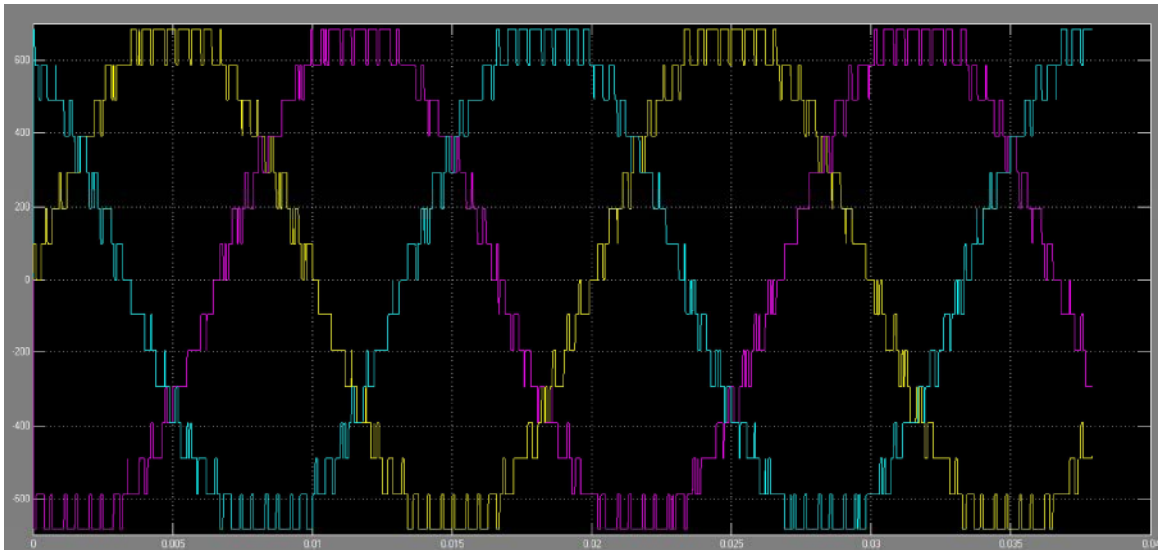

Fig. 3: Simulation results of three phase 15-level inverter related with voltage and time in MATLAB

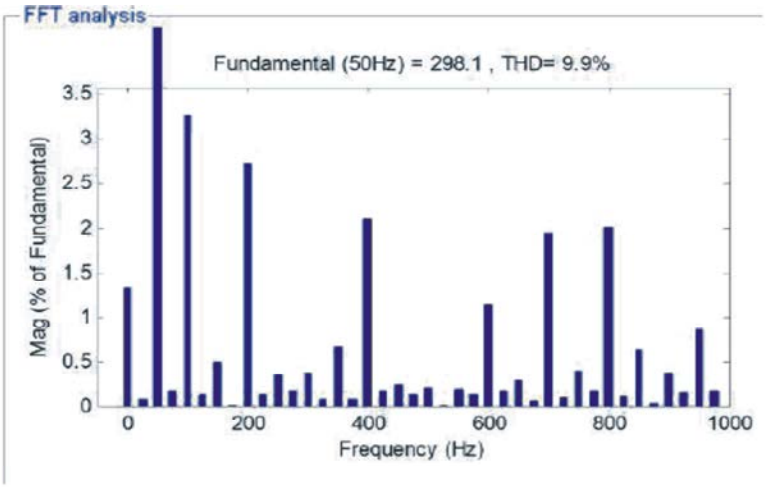

Fig. 4: FFT Analysis of three phase 15-level inverter related with Frequency& THD

(±6Vdc ±5Vdc, ±4Vdc,±3V_{dc}, ±2V_{dc}, ±1V_{dcand} 0). The number switches used in this topology is given by for each cell consists of a H- bridge uses four switches [11-17].

Simulation Results and Discussions: The Figure. 3 shown below is the simulink model of the three phase 15–Level cascaded H-Bridge Multilevel inverter using power system block set. The following parameter values are used for simulation: dc input voltage =100v (for all H bridge) f_c=2500 Hz and fm=50Hz with the modulation index of 1. The range of voltage is ±6.5V will be applied and with respect to time displayed for the proposed system. The total time scale is an 0.035ms required so step level related with the voltage the time will be changed based on the requirement.

In this proposed system of an simulation result is the output voltage and step level will be displayed with repect to time. The maximum step level of 15-Level And the corresponding voltage level for various steps displayed. The output voltage per steps with the time will be displayed. The range of voltage is upto ±6.5V can be delivered.The proposed 15-Level Three phase output is denoted in separate colors.

The FFT Analysis on output voltage waveform is shown in the Fig. 4 and Total Harmonic Distortion in MATLAB is 9.9%. It is seen that it has very low first or sixth voltage harmonics. Simulations are done for various values of m_a and the corresponding THD% are observed using FFT block and listed in Table 2.

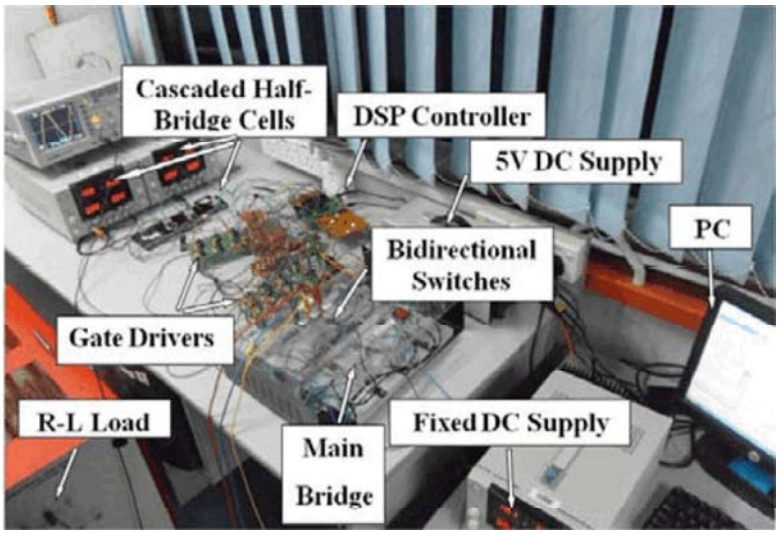

Fig. 5: Experimental setup for the proposed multilevel inverter

Table 2: Comparison of parameter values

Parameters	Existing method using 11 Level	Proposed method using 15 Level
THD	3.12%	9.9%
Voltage level	500 V	600 V
Output voltage	±5V	±6.5V
Frequency	50GHz	50GHz

To ensure the feasibility of the proposed topology, the inverter was implemented and its prototype has been manufactured. During the hardware implementation, the inverter shown in Fig. 5 was tested under Vdc = 100V for each cell. Fixed three-phase series resistive–inductive load (23Ω–3 mH/Phase) in star connection was used. For the purpose of generating the appropriate switching gate signals, a DSP controller was used. The fundamental frequency f = 50 Hz SPWM modulation technique was employed. In Fig. 5, the prototype of the proposed inverter is shown. It consists of the following components: personal computer, TMS320F28335 DSP controller, fixed dc voltage supply, conventional six-switch bridge, three bidirectional switches, two half-bridge cells, 13 gate drivers powered by 5 V dc supply and fixed three-phase (*R* - *L*) load. The type of semiconductors used for the power circuit is provided in Table I.

The following parameter values are used for simulation: dc input voltage =100v (for all H bridge) f_c =2500 Hz and fm=50Hz.Gating signals for level shifted carrier wave arrangements are simulated for 15-Levels MLI. Simulations are done for various values of m_a and the corresponding THD% are observed using FFT block and listed in Table 2.

CONCLUSION

Three phase cascaded H-bridge multilevel inverters from seven levels to 15-Levels have been simulated using Matlab/simulink. The H-bridge multilevel inverter consists of the four numbers of switches in each cell. The THD decreases to increase the number of levels, some lower or higher harmonic contents remain dominant in each. For purpose of minimizing THD%, a selective harmonic elimination pulse width modulation technique can be implemented. The future scope is to determine the switching techniques of a multilevel inverters then to reduce the harmonic content in the output voltage of the multilevel inverters for motor drive applications.

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