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A New Low Power Dynamic Full Adder Cell Based on Majority Function

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Abstract: A new low power dynamic CMOS one bit full adder cell is presented. In this design the time consuming XOR gates are eliminated. It is based on Majority Function. This new cell is compared with two widely used dynamic adders as well as other conventional and recently proposed architectures. It is implemented in two level dynamic CMOS with zipper technique and the number of transistors, chip area and switching activity is significantly reduced.

Keywords: CMOS VLSI design . low power . full adder . majority function . CPL . TFA . TGA

INTRODUCTION

Addition is one of the fundamental arithmetic operations. It is used extensively in many VLSI systems such as microprocessors and application specific DSP architecture. In addition to its main task, which is adding two numbers, it is the nucleus of many other useful operations such as, subtraction, multiplication, address calculation, etc [1-6].

Building low power VLSI system has emerged as significant performance goal because of the fast technology in mobile communication and computation. The advances in battery technology have not taken place as fast as the advances in electronic devices. So the designers are faced with more constraint; high speed, high throughput and at the same time, consuming as minimal power as possible.

Different CMOS logic styles have evolved for the development of cell libraries. They are likely to perpetuate the ability to further reduce the cost-per-function and improve the performance of integrated circuits. With the lowering of threshold voltage in ultra deep submicron technology, lowering the supply voltage appears to be the most eminent means to reduce power consumption. However, lowering supply voltage also increases circuit delay and degrades the drivability of cells designed with certain logic styles. Recently, clustered voltage scaling (CVS) and dual voltage supply (dual-VS) schemes have been proposed to maintain the chip throughput by selectively lowering the supply voltage for non-critical sub-circuits [7],[8]. For such techniques to be effective, it is imperative that the performances of the basic cells dominating the critical path be characterized in the target technology and application environment over various ranges of supply voltage.

The goal to extend battery life span of portable electronics is to reduce the energy expended per arithmetic operation, but Low Power consumption does not necessarily result in low energy dissipation. To execute an arithmetic operation, a circuit can consume very low power by clocking at extremely low frequency but it may take a very long time to complete the operation. We measure the energy consumption by the product of average power and worst case delay (power-delay-product).

As mentioned before several logic styles have been used in the past to design full adder cells. Some of these logic styles are listed below [9]:

1. Classical designs of full adder which normally use one logic style for the whole full adder design. One example of such design is the standard static CMOS full adder [10], which is shown in Fig. 1(a). This full adder is based on regular CMOS structure with conventional pull-up and pull-down transistors providing full-swing output and good driving capabilities. The main drawback of static CMOS circuits is the existence of the PMOS block, because of its low mobility compared to the NMOS devices. Therefore, the PMOS devices need to be sized up to attain the desired performance. The input capacitance of a static CMOS gate is large because each input is connected to the gate of at least a PMOS and a NMOS device. This is another reason for speed degradation of static CMOS gates.
2. Another conventional adder, shown in Fig. 1(b) is the Complementary Pass Transistor Logic (CPL)

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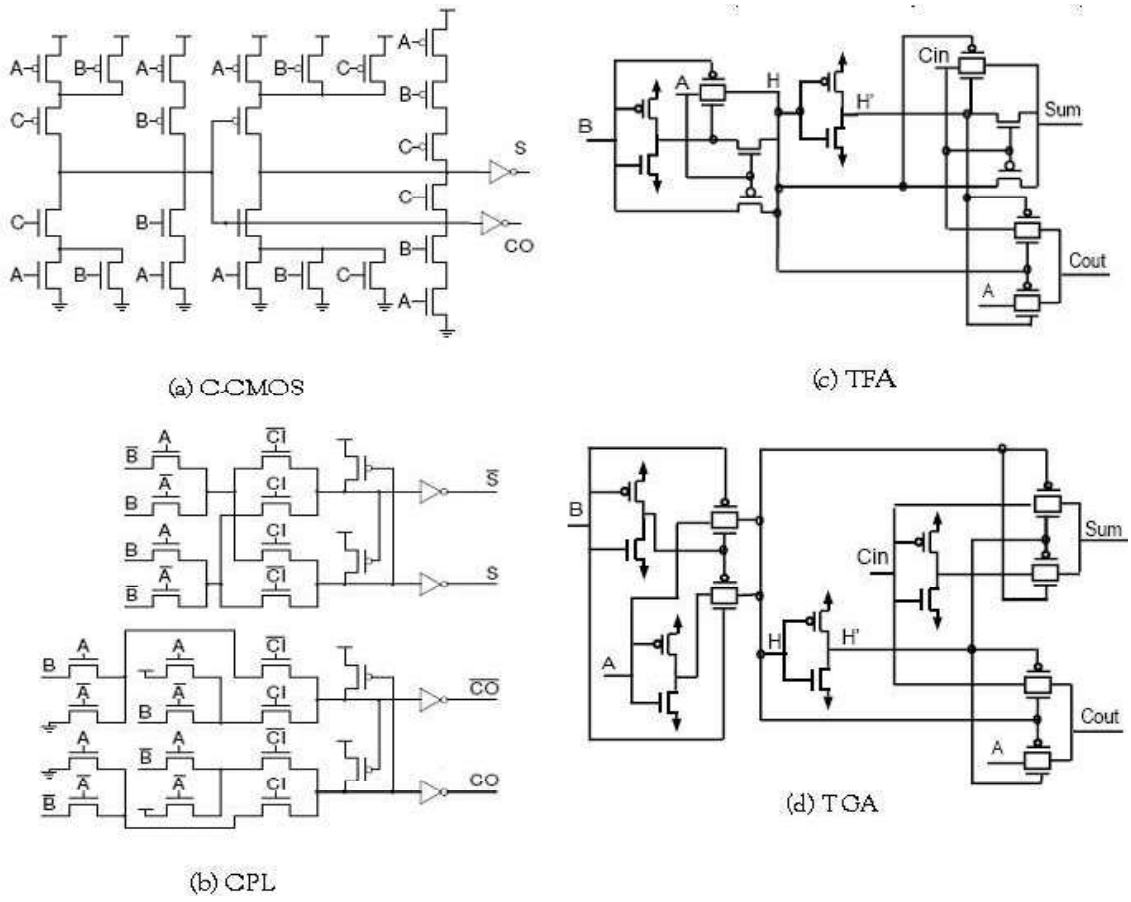
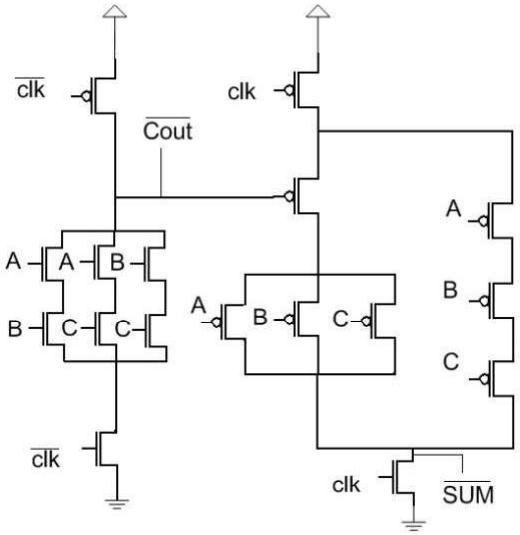


Fig. 1: Full adder cells of different logic styles. (a) C-CMOS, (b) CPL, (c) TFA, (d) TGA

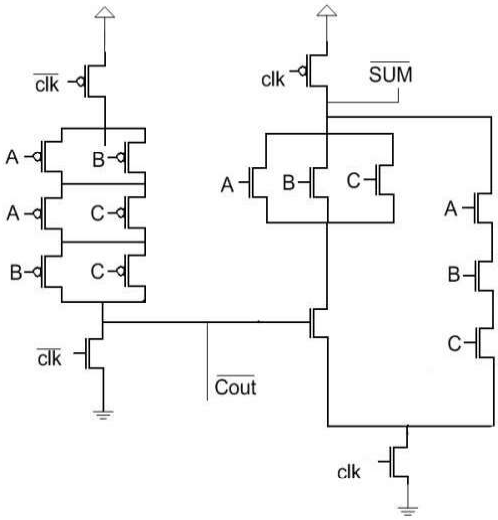
[10]. It provides high-speed, full-swing operation and good driving capabilities due to the output static inverters and fast differential stage of cross-coupled PMOS transistors. But due to the presence of a lot of internal nodes and static inverters, there is a large power dissipation.

3. Two other full adder designs include Transmission Function Full Adder (TFA) [11] and Transmission Gate Full Adder (TGA) [12]. These designs are based on transmission function theory and transmission gates, respectively. These adders, shown in Fig. 1(c), (d) are inherently low power consuming and they are good for designing XOR or XNOR gates. The main disadvantage of these logic styles is that they lack driving capability. When TGA or TFA are cascaded, their performance degrades significantly.
4. The remaining adder designs, which are not shown in this paper, use more than one logic style for their implementation. We call them Hybrid logic design style. Examples of adders built with this design style are DB cell, NEW 14-T [13] and Hybrid pass logic with static CMOS output drive full adder [14] and NEW-HPSC [15]. These designs exploit the feature of different logic styles to improve the performance of the circuit. Most of these adders lack driving capabilities in fan-out situation and the performance of these circuits degrade drastically when they are cascaded.

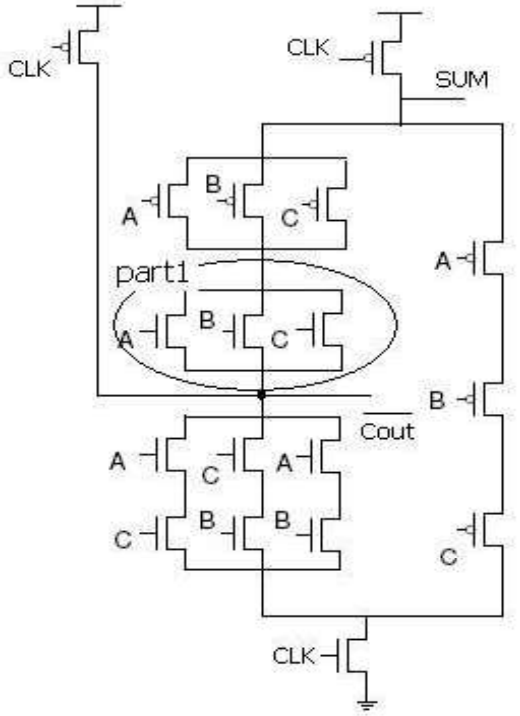
As mentioned, the main drawback of static logic style is the lack of performance, but in dynamic CMOS logic style which provides a high speed of operation this drawback is eliminated. Dynamic CMOS logic style provides high performance because this logic is constructed with only high Mobility NMOS transistors. Also due to the absence of the PMOS transistors, the input capacitance is also lower. The main disadvantage of dynamic logic style is power dissipation. In this paper we present a new low power dynamic adder cell which is built with the fewer transistors. This reduction of the transistors has been gained by new technique in designing NAND, NOR and the Majority Function. In order to maintain the performance of the circuit, this new technique is combined with modification of threshold voltages of specific transistors



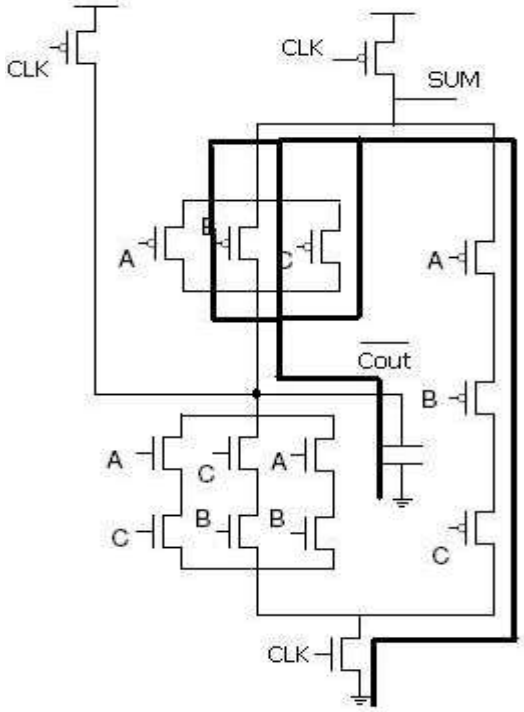
2 (a) (NP)



2 (b) (PN)



2(c) (Multi Output Dynamic Logic)



2(d) (Discharging in the absence of part1)

Fig. 2: Conventional dynamic full adder

MATERIALS AND METHODS

Conventional dynamic full adder: Several variants of Dynamic CMOS logic styles have been used to implement 1-bit full adder cell. The main advantages of these logic styles are: high driving capability, low input capacitance and high speed operation due to their characteristics, but the main drawback in these logic styles is Power-dissipation due to the higher switching activity than the static logic designs.

The NP complementary dynamic CMOS full adder [16] is shown in Fig. 2(a). It is based on regular dynamic CMOS designing in two level, with Zipper (NP) technique. The advantage of NP complementary dynamic CMOS style is its performance, but power consumption is high. The PN complementary dynamic

CMOS full adder is shown in Fig. 2(b). It is implemented in two level dynamic CMOS logic style with PN technique.

The Multi Output dynamic logic [17] is shown in Fig. 2(c). As shown in figure, the portion named part1, which has three transistors connected in parallel way is added to the whole circuit for keeping the charge of the $\overline{C_{out}}$ while the three input A, B and C_{in} have logic '0'. As we can see in the absence of these three transistors, the load capacitance of $\overline{C_{out}}$ will be discharged by the path shown in Fig. 2(d) and the functionality of the circuit will be ruined. This design uses one Clock signal, which is in contrast to NP and PN complementary designs that use two complementary clock signals, but the speed of this circuit is reduced due to the PMOS transistors used in its design. The other disadvantage of this implementation is that this circuit is not Full Swing, because discharging the load capacitance of SUM is done through PMOS transistors.

In the next section we will present a new technique for designing Majority Function and subsequently designing a Low Power Dynamic CMOS full adder.

New dynamic full adder cell with majority function: The Majority Function is a logic circuit that performs a Majority vote to determine the output of the circuit. In order to implement the full adder circuit with Majority Function, we review how the circuit of the full adder could be designed.

The full adder operation can be stated as follows: given the three input A, B and C_{in}, it is desired to calculate two 1-bit outputs SUM and C_{out}. Table 1 illustrates the truth table and the logic equations of full adder cell are shown in Equation (1) and Equation (2).

$$C_{out} = AB + AC + BC$$

$$Sum = \overline{C_{out}}\ (A + B + C) + ABC$$

As previous equations show C_{out} can be implemented with three inputs Majority Function as shown in Fig. 3(a) and if we invert the output of the circuit, $\overline{C_{out}}$ is produced with Majority Not Function circuit as shown in Fig. 3(b).

The new design of three input Majority Not Function, NAND and NOR with pre-charge dynamic CMOS circuit is shown in Fig. 4 (a). It uses three input capacitances in order to implement different Functions with unique circuit implementation. As shown, the number of transistors is reduced leading to lower power dissipation. The three inputs Majority Not Function which is implemented with pre-discharge dynamic CMOS circuit is shown in Fig.4 (b).

Table 1: Truth table of full adder cell

A	B	C_{in}	C_{out}	SUM	Majority function
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	1
1	0	0	0	1	0
1	0	1	1	0	1
1	1	0	1	0	1
1	1	1	1	1	1

Table 2: Implementing NAND, majority Not function and NOR (pre-charge)

A	B	C_{in}	NAND	Majority NOT Function	NOR
0	0	0	MN1= OFF	MN1= OFF	MN1= OFF
0	0	1	MN1= OFF	MN1= OFF	MN1= ON
0	1	0	MN1= OFF	MN1= OFF	MN1= ON
0	1	1	MN1= OFF	MN1= ON	MN1= ON
1	0	0	MN1= OFF	MN1= OFF	MN1= ON
1	0	1	MN1= OFF	MN1= ON	MN1= ON
1	1	0	MN1= OFF	MN1= ON	MN1= ON
1	1	1	MN1= ON	MN1= ON	MN1= ON

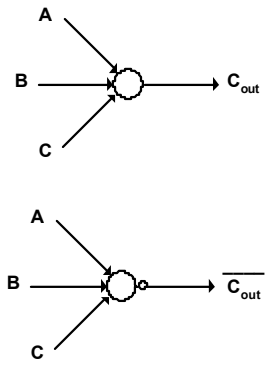
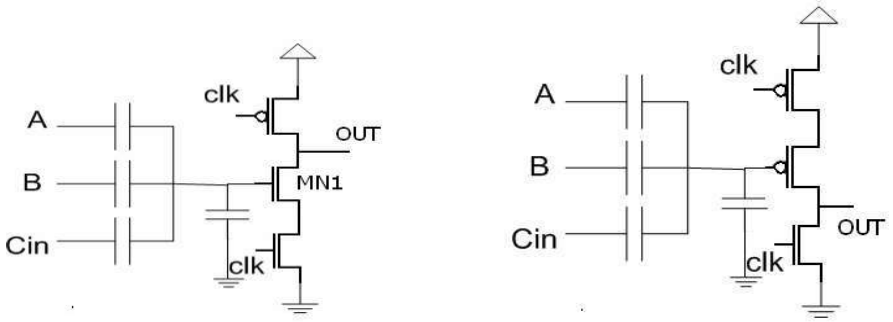


Fig. 3: Logic gates for (a) Majority Function, (b) Majority Not Function

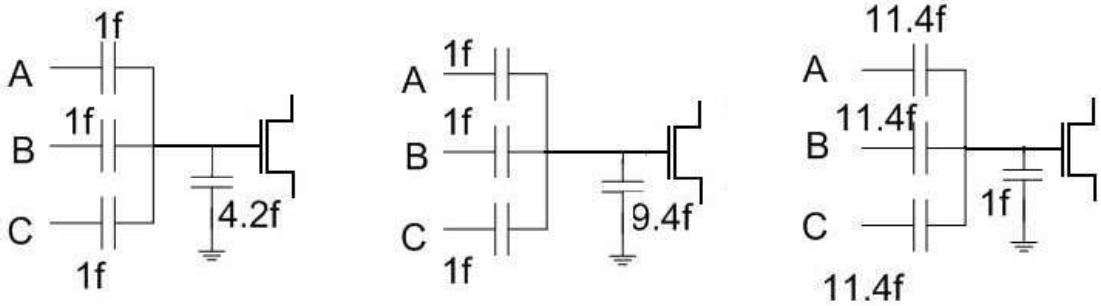
In order to make the circuit shown in Fig. 4(a) working as a Majority Not Function, transistor MN1 must be turned on ($V_{gs}>V_{th}$) when at least two out of the three inputs are high, but if the transistor turns on when one of its input goes high, the NOR function is implemented and for implementing NAND function, transistors MN1 must be turned on whenever all the inputs are high. Table 2 demonstrates how these three functions could be implemented with this new design.

As we can see, all these function could be designed by selecting the correct values for input capacitances. The values of input capacitances for building Majority not Function, NAND and NOR is shown in Fig. 5.



4(a) Majority Not Function, NAND, NOR (pre-charge) 4(b) Majority Function (pre-discharge)

Fig. 4: Dynamic CMOS



5(a) Majority not Function 5(b) NAND 5 (c) NOR

Fig. 5: Values of input capacitances for (a) Majority not Function, (b) NAND, (c) NOR (pre-charge)

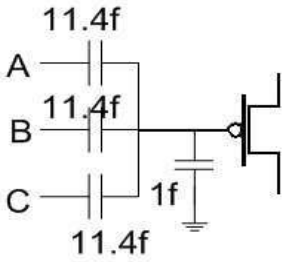


Fig. 6: Majority Not Function

In order to make the pre-discharge circuit (Fig. 4(b)) working as a Majority Not Function, the threshold voltages of PMOS transistor is reduced to-0.9 V and the values of input capacitances is selected accurately as shown in Fig. 6, the PMOS transistor with modified V_{th} is shown with thick lines for the gate. This reduction in V_{th} influenced the performance of the circuit, but on the other side the lower power dissipation is gained and as we show in the next section, the energy consumed per switching activity is better. Table 3 illustrates the implementation of Majority Not Function with the pre-discharge dynamic CMOS circuit.

In our first attempt for designing Low Power full adder cell, the Majority Not Function is used for implementing $\overline{C_{out}}$ with pre-discharge dynamic circuit shown in Fig. 6 and in the next level of the full adder circuit, the $\overline{SUM}$ is implemented with Zipper (PN) technique as shown in Fig. 7. By using this technique the number of transistors is reduced from 17 to 12 transistors, this degradation causes a great reduction in

Table 3: Implementing majority Not function (pre-discharge)

A	B	C_{in}	Majority NOT Function
0	0	0	MP1= ON
0	0	1	MP1= ON
0	1	0	MP1= ON
0	1	1	MP1= OFF
1	0	0	MP1= ON
1	0	1	MP1= OFF
1	1	0	MP1= OFF
1	1	1	MP1= OFF

Table 4: Values of input capacitances, gate capacitances and threshold voltage

Transistors	Input capacitances	Gate capacitance	V_{th}
PMOS (MP1)	11.4 f	1 f	-0.9 V
NMOS (MN1)	11.4 f	1 f	0.332 V
NMOS (MN2)	1.00 f	9.4 f	0.332 V

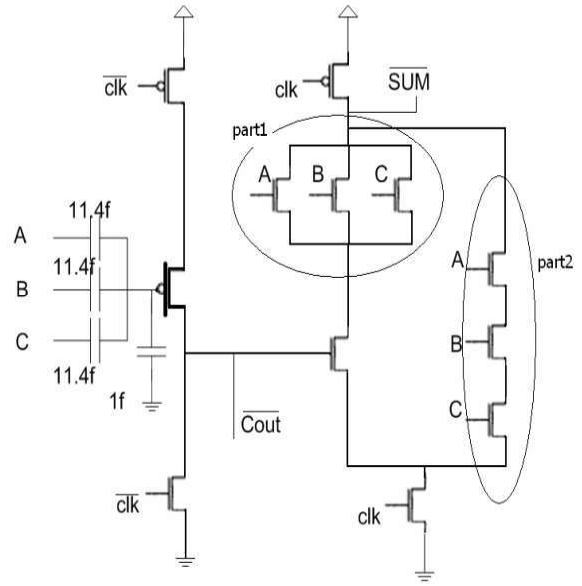


Fig. 7: Dynamic Full Adder cell based on Majority Not Function in two-level Zipper (PN) technique

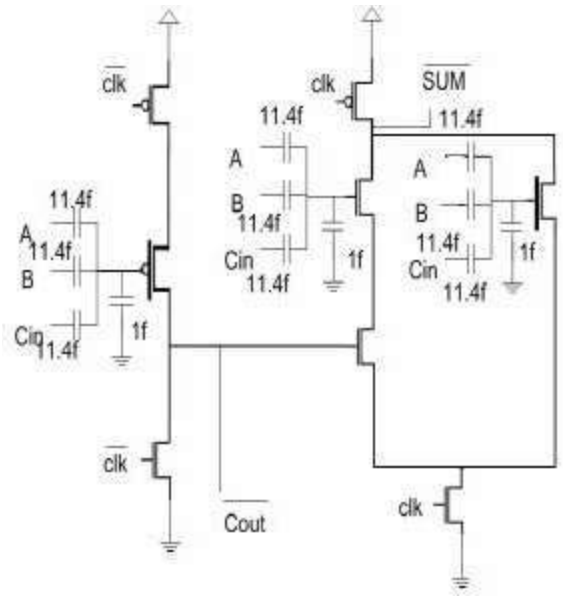


Fig. 9: Full Adder cell based on Majority Not Function in two level Zipper (PN) technique with nine equal input capacitances

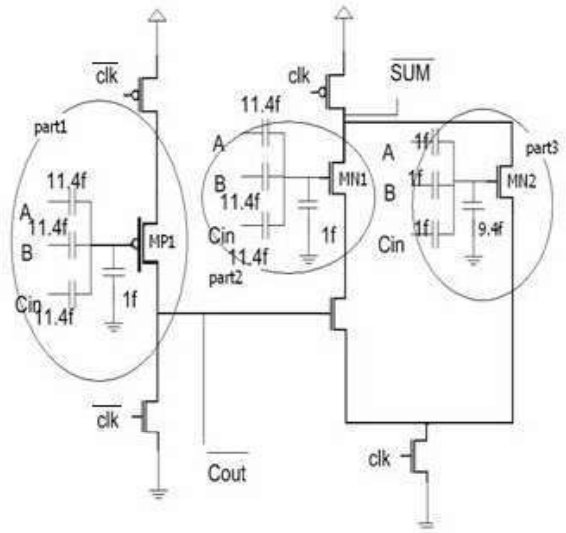


Fig. 8: Dynamic Full Adder cell based on Majority Not Function in two level Zipper (PN) technique with nine input capacitances

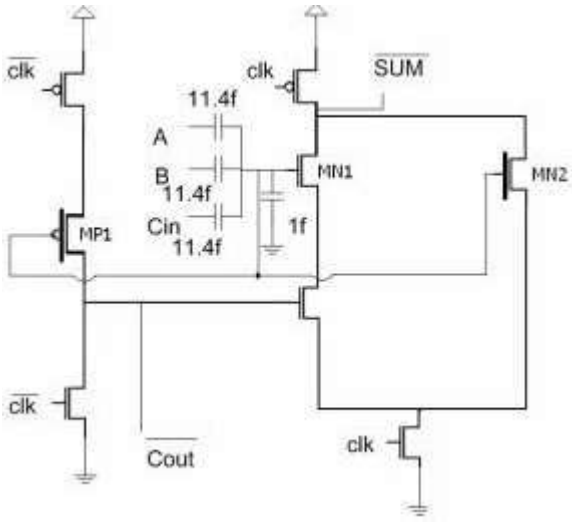
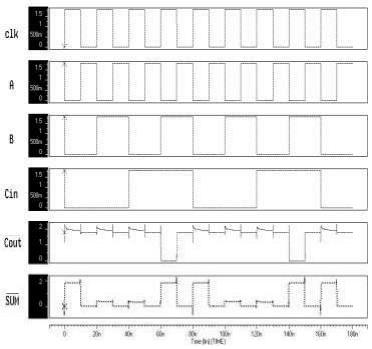


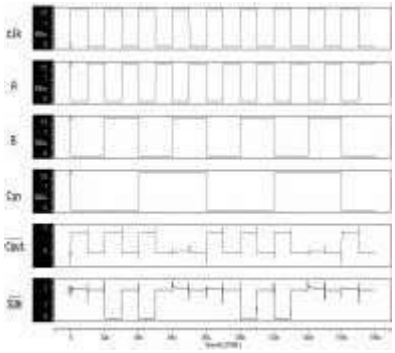
Fig. 10: Full Adder cell based on Majority Not Function in two level Zipper (PN) technique with three equal input capacitances

power consumption, but in order to have a better Power-Delay-Product (PDP), the circuit is changed due to the new design of NOR and NAND function. As we can see Part1 of the circuit shown in Fig. 7 could be substituted with the circuit shown in Fig. 5(c) and Part 2 of the circuit is substituted with the circuit shown in Fig. 5(b), so in the second approach the whole full adder cell is implemented with 8 transistors and 9 input capacitances in Zipper (PN) dynamic circuit. Fig. 8 illustrates this new dynamic full adder. Table 4 demonstrates the values of input capacitances, the values of gate capacitances and the threshold voltages of three transistors shown in Fig. 8.

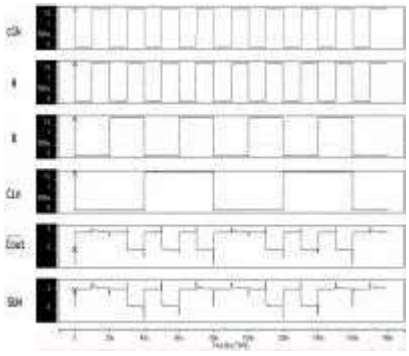
This design is a new low power design of full adder circuit in dynamic mode, but as we can see 9 input capacitances influence the speed of the circuit. In order to maintain the performance of the circuit, we have to reduce the number of the input capacitances. So in the next step we attempt to use equal values for input



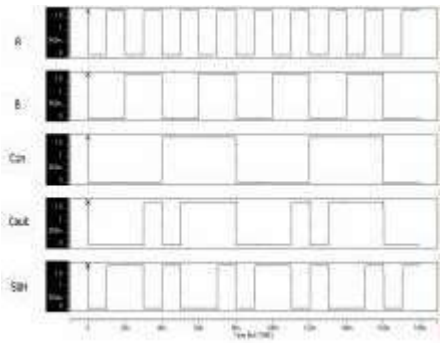
11-(a) NP_C_CMOS



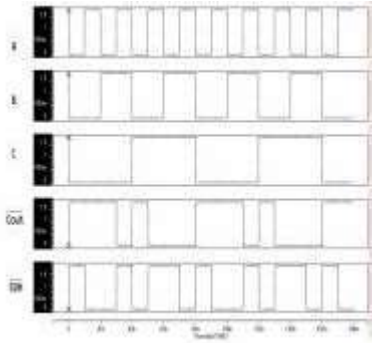
11(b) PN_C_CMOS



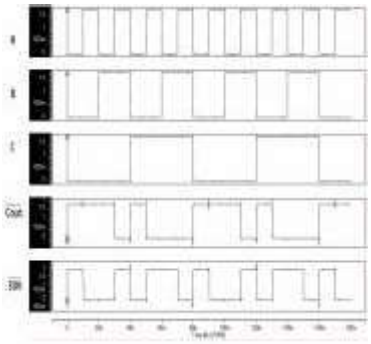
11(c) MODL



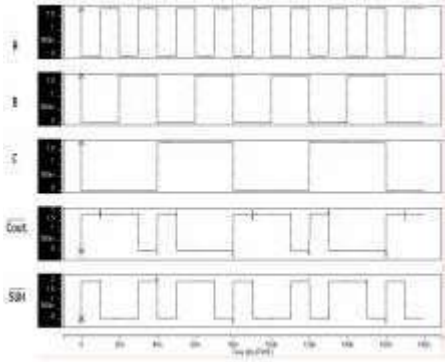
11(d) C_CMOS



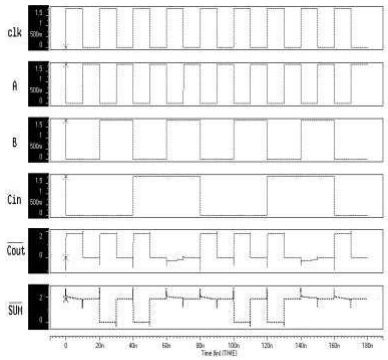
11(e) CPL



11(f) TFA



11(g) TGA



11(h) Proposed circuit (8T)

Fig. 11: The output waveform of (a)NP_C_CMOS, (b)PN_C_CMOS, (c) MODL, (d) C_CMOS, (e)CPL, (f)TFA, (g) TGA, (h) proposed circuit (8T). Frequency of the clock is 100 MHz with a supply voltage of 1.8 V

Table 5: Values of input capacitances, gate capacitances and threshold voltage (proposed circuit)

Transistors	Input Capacitances	Gate Capacitance	V_{th}
PMOS (MP1)	No need for	Additional Capacitance	-0.9 V
NMOS (MN1)	11.4 f	1 f	0.39 V
NMOS (MN2)	No need for	Additional Capacitance	1.25 V

Table 6: Simulation results for the proposed full adder in 0.18 um Technology at 100 Mhz and 1.8 V, Vdd

DESIGN	Power (uw)	Delay(ns)	PDP(fJ)
C-CMOS	2.7473	0.1331	0.3657
CPL	4.0134	0.1298	0.5209
TFA	3.0357	0.1325	0.4022
TGA	3.0660	0.1345	0.4124
NP_C_CMOS	3.1823	0.1299	0.4133
PN_C_CMOS	3.2129	0.1286	0.4132
MODL	3.5692	0.1975	0.7049
8T(proposed)	1.1855	0.1663	0.1971

capacitances in all three parts shown in Fig. 8. In order that part 3 in Fig. 8 works properly with input capacitances in part 1 and part 2, the threshold voltage of NMOS transistor in part3 has to be increased up to 1.25V. This circuit is shown in Fig. 9, transistors with modified V_{th} are shown with thick lines for the gates. This reduction in number of the input capacitances results in better performance but the effect of the modified V_{th} is still remained. Finally in this situation three input capacitances can be used for all three parts instead of 9 input capacitances and the delay of the circuit is reduced due to the lower input capacitances, meanwhile the power consumption of the circuit is low, leading to have a better Power-Delay-Product. This new 8 transistors (8T) dynamic full adder is shown in Fig. 10. Table 5 illustrates the values of input capacitances, the values of gate capacitance and the threshold voltages of three transistors shown in Fig. 10.

RESULTS AND DISCUSSION

The four Dynamic full adders: NP_C_CMOS, PN_C_CMOS, proposed full adder with Majority Function (8T), conventional Multi Output Dynamic Logic (MODL) and four static full adders: C_CMOS, TFA, TGA, CPL are all simulated using 0.18um CMOS process. The threshold voltage of the NMOS and PMOS transistors are around 0.39 and 0.42V, the supply voltage is 1.8V and the frequency (clock rate) is 100 Mhz. HSPICE circuit simulator is used for simulation. The output waveform of each full adder is shown in Fig. 11.

By optimizing the transistor sizes of full adders considered, it is possible to reduce the delay of all adders without significantly increasing the power consumption and transistor sizes can be set to achieve minimum PDP. All adders were design with minimum transistor sizes initially and then simulated.

Comparison of full adders designed to achieve minimum PDP is discussed below, three subsections refer to DELAY, POWER and PDP.

Delay comparison: The values of delay obtained for considered value of VDD (1.8V) for all dynamic full adders are shown in Table 6. It is apparent that amongst the existing dynamic full adders, the NP and PN complementary dynamic CMOS full adder has the smallest delay, because the threshold voltages of their transistors have not been modified and due to their dynamic characteristics, high performance is supported. It is shown that among the static full adders C_CMOS is the fastest. As we can see the performance of the PN_C_CMOS circuit is better in comparison with new 8T design. The 8T dynamic full adder is 23% slower than PN complementary dynamic CMOS full adder, but this degradation is compensated with its improvement in power dissipation and as we will see this design has better PDP. The MODL is the slowest circuit, because of using PMOS transistors in its structure.

Power comparison: Average power dissipation of all the full adders is shown in Table 6. The CPL adder dissipates the most power because of its dual-rail structure and high number of internal nodes in its design.

TFA and TGA have lesser transistor count in comparison to CPL, but due to the lack of drivability, additional buffers are required at each output, which increase their short circuit power as well as switching power. The MODL, NP_C_CMOS, PN_C_CMOS dissipates the most power because of their dynamic characteristics and their transistor count. Among the existing full adders, 8T has the lowest power dissipation. The 8T adder dissipates the least power because of its transistors count and as shown in Table 6, the improvement of power dissipation is 57% in comparison with C_CMOS.

PDP comparison: The PDP is a quantitative measure of the efficiency of the tradeoff between power dissipation and speed and is particularly important when low power operation is needed. The values of PDP, evaluated under 1.8 V supply voltage, are summarized in Table 6. As shown in Table 6, The 8T has the best PDP in comparison with the others. The PDP improvement of 8T dynamic full adder is 46% in

comparison with C_CMOS. As we can see the delay degradation in 8T is compensated with the improvement in its power dissipation, leading to a better PDP.

CONCLUSION

A new dynamic full adder cell based on Majority Function is proposed. Although conventional dynamic style suffers from the excessive power dissipation, this new design enjoys low power and high performance. A widely comparison to the state of the art designs cited in the VLSI literature illustrates a significant improvement in terms of power dissipation and Power-Delay product (PDP) parameter. The number of transistors used is significantly reduced resulting in a great reduction in switching activity. Besides, due to its dynamic characteristic, short circuit current is eliminated. This considerable reduction in power dissipation as well as some techniques to enhance the speed of the design leads to the best PDP.

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