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Analysis of Leakage Power Reduction in Low Power Bio Instrumentation Amplifier

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Abstract: In day today life the biomedical instruments play very important role in bio signal acquisition. The bio instrumentation amplifiers are the most sensational part in bio instruments like electromyography, electrocardiography andimplantable pacemaker. Power dissipation is the challenging factor in design of bio instruments for signal recording. Thus there is requirement of bio amplifiers with low power consumption. In this project, ultra low power bio amplifier is designed with self biasing technique for bio medical application. However, with the continuous trend of technology scaling, leakage power is becoming a main contributor to power consumption. In order to reduce the leakage power in bio amplifier, the circuit is analysed with leakage power reduction techniques like sleepy keeper and feedback approach in folded cascode bio amplifier. The Bio amplifier is designed with high gain, better slew rate at 130nm technology. The proposed bio amplifier consumes less power compared to other existing two stage folded cascode and Folded cascode CMOS bio amplifiers.

Key words: Bio Amplifiers · Cacosde · Leakage Power · Slew rate · Sleepy keeper · High gain

INTRODUCTION

Now a day, Bio medical instruments play a vital role in modern bio signal monitoring, recording and processing. The most commonly monitored bio-potential signals are electrical activity produced by skeletal muscles, electrical activity of the heart and electrical conductance of the skin, these signals are recorded with the help of the devices such as Electromyography (EMG), Electrocardiography (ECG or EKG) and galvanic skin response respectively. These devices are used to monitor the signals continuously and use bio-amplifier as their major component. Biomedical signal has very weak amplitude and low frequency, usually of few Millis volts or less and the Frequency below 1 KHz. While using high power there is more loss of power supply as signal has to be to record continuously.Designing a low power bio medical instruments is a challenging task. In normal signal acquisition system incudes electrodes/transducers, instrumentation amplifier, analog to digital converter, filter and display monitor. The electrodes are used to sense the signals inside the humans and these signals are amplified using amplifiers which mainly involve the bio amplifiers for further signal processing. Such bio potential signal value is very weak as compared to the noise floor and imperfection of the commonly used operational amplifiers (OPAs). These instrumentation amplifiers are bio-amplifier. Earlier the bio-amplifier is designed in many techniques. These techniques are designed with the use of low power CMOS, but those techniques have some disadvantages and do not get the targeted values as they expected. The disadvantages of those techniques are low CMRR, low Gain. Even though when there is an increase in Gain it leads to increase in the noise also the accuracy is not better. To improve the parameters such as gain, CMRR, PSRR, Bandwidth and supply voltage we need a new design technique. Designing an instrumentation amplifier with CMOS using folded cascode amplifier suitable for Bio medical application with increased gain, increased CMRR as specified for a good instrumentation amplifier. The Bio amplifiers used are generally designed using CMOS. In the modern CMOS technology there occurs problem in power leakage though the other parameters are up to satisfaction. Thus leakage reduction technique is required to reduce the power leakage such that it suits for the low power instruments [1].

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Leakage Power Reduction in Bioamplifier: Various folded cascode operational Transconductance amplifiers using different techniques such as self cascode of folded cascode operational Transconductance amplifier, two stage folded cascode CMOS op-amp etc. These techniques are discussed and the various leakage reducing methods are studied.

Two Stage Folded Cascode Cmos Opamp: Folded Cascode OTA is better operational amplifier architecture. Firstly, OTA designer occupies small overhead and folded structure allows a low supply voltage to systems where is embedded andlow current consumption. Secondly, the PMOS differential pair that converts the input voltage to current deals less noise compared with a NMOS differential pair [2].

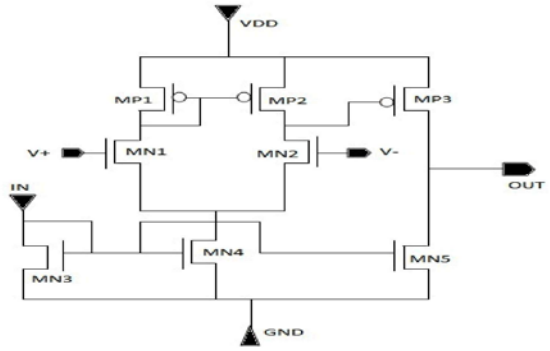

Fig. 1: Schematic of folded cascode CMOS opamp

In addition, the folded cascode transistors structure deals to OTA amplifier good gain and higher output impedance; this is depend on dynamic parameters and which are improved by the cascade transistors structure. Finally, the folded cascode structure improved the excursion of common mode input range (CMR); it is compared with other structures such as telescopic OTA. The output voltage swing of Folded Cascode OTA structure is improves [3].

Folded Cascode OTA Topology: The input stage provides the gain of the operational amplifier. Due to the greater mobility of a NMOS device, PMOS input differential pair presents a lower Transconductance than a carrier NMOS pair. NMOS transistor has been chosen to ensure the largest gain required [4].

We opt for a folded cascode op-amp due to its large gain and high bandwidth performances. This circuit presents the strategy design of folded cascode OTA in the three operation modes of transistor: weak inversion,

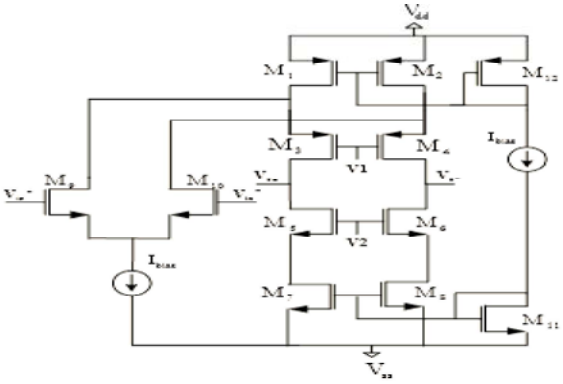

Fig. 2: Schematic of folded cascode topology

strong inversion and moderate inversion. So the goal to reach high gain and large bandwidth has been fulfilled but the leakage power is not reduced.

Folded Cascode OTA Using Self Cascode: A self cascode structure is used in low voltage design. The advantages in using self cascode structure is that it high output impedance.

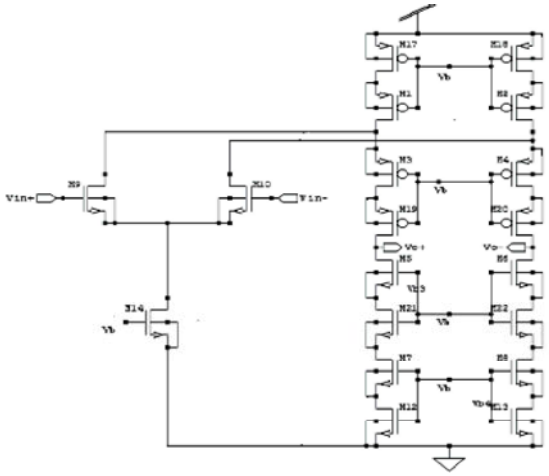

Fig. 3: Schematic of folded cascode OTA using self cascode

At input terminals self cascode is not used, but in the whole circuit self cascode is used because this whole circuit works as load. In this circuit each transistor is split into two so that upper transistors are working in saturated region while other is in linear region to work this circuit properly [5]. The regular cascode structures are avoided as their use increases the gain of the structure, but decreases the output signal swing. Self cascode is the new technique, which does not require high compliance voltage at output nodes. It is useful in low-voltage design.

The main drawback of this circuit is it produces more power leakage [6].

Low Power Reduction Technique: The power may be of two types' static power and dynamic power. Static power essentially consumed power when the transistor is not in the process of switching. Dynamic power is power consumed while the inputs are active. When inputs have ac activity, capacitances are charging and discharging and the power increases as a result. The dynamic power includes both the ac component as well as the static component.

The rapid growth in semiconductor technology through the use of deep-submicron processes has led the feature sizes to be shrinking; thereby integrating extremely complex functionality on a single chip. In the ever increasing market of mobile hand-held devices used all over the world today, the battery-powered electronic system forms the backbone. To maximize the battery life, the tremendous computational capacity of portable devices such as notebook computers, personal communication devices (mobile phones, pocket PCs, PDAs), hearing aids and implantable pacemakers has to be realized with very low power requirements [7]

It has been shown that as the technology scales down below 100nm which is the shrinking of feature size of transistor, the channel length decreases, thereby increasing the amount of leakage power in the total power dissipated. As we can see as the technology is moving towards lower nanotechnology the sub-threshold leakage increases thereby affecting the battery life. Thus there were various technique developed to deal with this problems [8].

Leakage Reduction Technique in Folded Cascode: The Sleepy and the feedback leakage reduction techniques are the two methods that are implemented in the Folded cascode using self cascode amplifier [7].

Sleepy Approach: Folded cascode using self cascode is modified with the introduction of leakage reducing technique such as the sleepy approach and feedback approach. In the Folded cascode using self cascode along with sleepy approach is designed by adding an PMOS in between the pull up network and v_{dd} supply and an NMOS is added in between the pull down network and the v_{ss}. the input to both PMOS and NMOS are provided in the form of pulse waveform.

Feedback Method: This method is also used for leakage reduction in Folded cascode using self cascode. This method includes an additional PMOS parallel to the NMOS in the pull down network and an additional NMOS parallel to the PMOS in the pull up network. The additionally added PMOS and NMOS base are connected to the outputs o1 and o2 respectively in the format of the feedback and they are connected parallel to the existing PMOS and NMOS with the same Pulse signal as the biasing. In sleep mode, this NMOS transistor is the only source of VDD to the pull-up network since the sleep transistor is off. An additional single PMOS transistor placed in parallel to the pull-down sleep transistor is the only source of GND to the pull-down network.

The leakage reduction in the sleepy technique is much perfect than the feedback approach by the analysis method and the simulation result of the existing Folded cascode method along with sleepy approach is done by using the HSPICE software and the parameters re measured using the cosmoscope and result analysis are made as a comparative tabulation that provides an clear idea about the best method that well suits for the leakage reduction in the low power application.

Leakage Reduction in Folded Cascode with Self Biasing: The Folded cascode design is modified in such a way that the external biasing is avoided and self biasing is provided for each MOSFETs. The leakage reduction techniques are also included in the modified folded cascode using self cascade [9].

Sleepy Method: This is same as the Folded cascode with external biasing, the only change is the biasing signal provided externally. The biasing is provided internally as self biasing. The biasing input to the Mosfet M3 is provided internally by connecting gate to the source side of the Mosfet.

Feedback Method: In this method, a small change in the biasing input to M3 which is provided internally by connecting gate to the source. The circuits are designed with the folded cascode with self cascode along with leakage reduction using two methods that includes the sleepy approach and feedback leakage reduction and also folded cascode with self biasing including the sleepy and the Feedback method of leakage reduction [10].

Simulation and Result Analysis: Earlier these circuits are designed using various CMOS technology. Here we are going to use 130nm CMOS technology using the software HSPICE. The circuits, two stage folded cascode amplifiers, Folded cascode with self cascode, folded cascode CMOS op amp are simulated and their corresponding results are discussed below.

Simulation Steps: The comparative analysis of the various tcchiques are tabulated which implies the various technologies used for the design, their supply voltage, slew rate and power consumption. There does not involves the study of the power leakage that occurs while the supply voltage is reduced.This resultanalysis deals mainly with the power leakage problem that occurs and the methods implemented to reduce the leakage power [11].

From the below, the analysis of the bio amplifiers with self biasing it is found that the gain for the folded cascode using self cascode with self biasing is 95.25dB which is 2.32% more than the two stage folded cascode opamp with self biasing and is 33.3 % more than the Folded cascode CMOS opamp. Thus the best circuit is chosen as the folded cascode using self cascode with self biasing [12].

Table 1: Performance analysis of various Bio amplifiers

Parameters	Folded cascode CMOS opamp		Two stage folded cascode CMOS opamp		Folded cascode using self cascode	
Technology	350nm	130nm	180nm	130nm	180nm	130nm
Supply voltage	2V	1.8V	1V	1.8V	1.8V	1.8V
Slew rate	3.3v/μs	1.851v/ms	196v/μs	1.082v/ms	16.3v/μs	1.537v/ms
Power consumption	6.35µW	0.6nW	263µW	0.44nW	1.038µW	0.086nW
Gain	67dB	63dB	67.7dB	95dB	60.96dB	90.75dB

Table 2: Leakage power analysis and delay analysis of various design techniques

Parameters	Folded cascode CMOS opamp	Two stage folded cascode CMOS opamp	Folded cascode using self cascode
Leakage power	1732pW	497.9pW	3.812pW
Delay	1.9µs	3.469ms	9.6µs

Table 3: Performance Analysis of self biasing amplifiers in 130nm technology

Parameters	Folded cascode CMOS opamp self biasing	Two stage folded cascode CMOS opamp self biasing	Folded cascode using self cascode self biasing
Average power	162.3pW	27.71pW	0.2170pW
Peak power	0.059µW	2.70µW	0.01732µW
Bandwidth	7.3459KHZ	8.3829KHz	7.6176KHZ
Frequency	50	50Hz	50.011Hz
Slew rate	1.7533v/ms	1.0826v/ms	1.3522v/ms
Delay	0.0192ms	3.46ms	0.0115ms
Gain	60dB	92.3dB	95.25dB

Table 4: Comparative Analysis of Folded cascode and its self biasing Folded cascade

Parameters	Folded cascode using self cascode	Folded cascode using self cascode with self biasing
Average power	0.86nW	0.2170nW
Leakage power	3.812pW	25.35pW
Peak power	16.3 μw	0.1732µW
Bandwidth	78.01KHZ	7.6176KHz
Frequency	50.011Hz	50.011Hz
Slew rate	1537.9	1352.2
Delay	0.009ms	0.0113µs
Gain	90.75dB	95.25dB

Table 5: Performance analysis of Folded cascode with sleepy and feedback leakage reduction techniques

Parameters	Folded cascode using self cascode	Using sleepy keeper	Using feedback
Average power	0.8608nW	0.8241nW	0.7109nW
Leakage power	3.812pW	2.385pW	1.302pW
Peak power	16.3 μw	16.9 μw	16.3 μw
Bandwidth	78.01	72.72	76.02
Frequency	50.01Hz	50.1Hz	50.1Hz
Slew rate	1.5379v/ms	1.568v/ms	1.3509v/ms
Delay	9.6µs	9.06µs	9.7µs
Gain	90.75dB	90.7dB	90.75dB

Table 6: Performance analysis of Folded cascode using self biasing with sleepy and feedback leakage reduction techniques

Parameters	Folded cascode using self cascode with self biasing (This work)	Using sleepy keeper	Using feedback
Average power	0.2170nW	0.2641nW	0.2309nW
Leakage power	25.35pW	23.85pW	23.02pW
Peak power	0.1732µW	0.135 μw	0.163 μw
Bandwidth	7.6176KHz	7.372KHz	7.802KHz
Frequency	50.011Hz	50.1Hz	50.1Hz
Slew rate	1.3522v/ms	1.5698v/ms	1.3509v/ms
Delay	0.0113µs	1.9µs	2.9µs
Gain	95.25dB	95.7dB	95.2dB

Proposed Folded Cascode with Self Cascode with Leakage Reduction: The various leakage reduction techniques are induced in the Folded cascode with self cascode opamp. And their bandwidth, delay, transient analysis and AC analysis are obtained using HSPICE software and COSMOSCOPE. The leakage can be reduced by sleepy approach and Feedback approach.

CONCLUSION

In this paper, ultra low power bio amplifier is designed with self biasing technique for bio medical application. The circuit of folded cascode CMOS opamp, folded cascode using self cascode, two stage folded cascode CMOS opamp are designed and simulated using HSPICE software and various parameters are measured using COSMOSSCOPE. By simulation, different parameters of the existing system such as average power, peak power, delay, bandwidth, frequency, slew rate and gain are measured and the best circuit is found out. Implementing the leakage reduction technique and comparing the parameters, it is found that the gain for the folded cascode bio amplifier is increased by 33.3% when designed at 130nm technology than at 180nm technology. The same amplifier with self biasing technique produces increased gain of 5.2% than in normal external biasing. This folded cascode is found to be good and in addition leakage reduction of sleepy approach is implemented in this amplifier that decreases the leakage power by 37.4%. In the case of feedback approach in comparison with the original folded cascode bio amplifier the leakage power is decreased by 45.4%.Thus by analysis it is concluded that the folded cascode amplifier with feedback technique is suitable for low power bio medical instruments.

REFERENCES

1. Yu-Ming Hsiao, Miin-Shyue Shiau, Kuen-Han Li, Jing-Jhong Hou, Heng-Shou Hsu, Hong-Chong Wu andDon-Gey Liu, 2013. Design a Bioamplifier with High CMRR″, Hindawi Publishing Corporation VLSI Design Volume 2013, Article ID 210265, 5 pages
2. Toihria, I. and T. Tixier, *2015.* Improved PSRR and Output Voltage Swing Characteristics of Folded Cascode OTA, International Journal of Electronics and Electrical Engineering, Vol. 3, Issue 4, August – 2015.
3. Akshy goel and Gurmohan Singh. 2013. A Novel Low Noise High Gain CMOS Instrumentation Amplifier for Biomedical Applications", International Journal of Electrical and Computer Engineering (IJECE) Vol. 3, No. 4, August 2013, pp. 516~523 ISSN: 2088-8708.
4. Daoud, H. Dammak, S. Bensalem, S. Zouari and M. Loulou, 2008. Design of Folded Cascode OTA in Different Regions of Operation Through gm/ID Methodology, International Journal of Electrical and Electronics Engineering 1:3 2008.

5. Swati kundra, Priyankha Soni and Rhohaila Naaz, 0000. Folded cascode OTA using self cascode technique, International Journal of Electrical and Electronics Engineering.
6. Ruchiyata Singh and A.S.M. Tripathi, 2014. A new approach for delay and leakage power reduction in CMOS VLSI circuits, International Journal of Advance Research In Science And Engineering, IJARSE, Vol. No.3, Issue No.5, May -2014.
7. Khushboo Kumari1, Arun Agarwa, Jayvrat, Kabita Agarwa, 2014. Review of Leakage Power Reduction in CMOS Circuits, American Journal of Electrical and Electronic Engineering, 2014, Vol. 2, No. 4, pp: 133-136 .
8. Jin-Yong Zhang, Lei Wang1 and Bin Li, 2009. Design of low-offset low- power CMOS amplifier for biosensor application, J. Biomedical Science and Engineering, pp: 538-542.
9. Sonu Mourya, Pankaj Naik and Priyanka Sharma, 2013. Designing Of Current Mode Instrumentation Amplifier For Bio-Signal Using 180nm CMOS Technology, International Journal of Engineering Research & Technology (IJERT), Vol. 2 Issue 4, April – 2013.
10. Chung-Yu Wu and Chia-Shiung Ho, 2015. An 8-Channel Chopper-Stabilized Analog Front-End Amplifier for EEG Acquisition in 65-nm CMOS, IEEE Asian Solid-State Circuits Conference, November 9-11, 2015 / Xiamen, Fujian, China
11. Vighnesh Rudra Das, Donald Y.C. Lie and Tam Nguyen, 2014. A Fully Integrated Low Noise CMOS Instrumentation Amplifier Design for Low-Power Biosensors, IEEE Conference paper, August - 2014.
12. Qinwen Fan, Student Member, IEEE, Fabio Sebastiano, Student Member, IEEE, Johan H. Huijsing, Life Fellow, IEEE andKofi A. A. Makinwa, Fellow, IEEE(2011), "A 1.8 W 60 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ Capacitively-Coupled Chopper Instrumentation Amplifier in 65 nm CMOS for Wireless Sensor Nodes", *IEEE Journal of solid-state circuits*, vol. 46, no. 7, July – 2011.