World Applied Sciences Journal 34 (6): 760-769, 2016
ISSN 1818-4952

DOI: 10.5829/idosi.wasj.2016.34.6.22

Design and Development Multilevel Inverterwith Different Modulation Index (MI) Based on Super Capacitor (SC) for Harmonic Reduction

Mohammed Rasheed, Rosli Omar and Marizan Sulaiman

Universiti Teknikal Malaysia Melaka, Faculty of Electrical Engineering, Industrial Power, 76100 Hang Tuah Jaya, Durian Tunggal, Melaka, Malaysia

Abstract: This paper presents a study on a three-phase five level Cascaded H-bridge multilevel inverter (CHBMLI) based on Newton-Raphson (NR) technique controller for optimization and non-optimization technique for harmonic reduction. The proposed system comprises of a DC source made up of super capacitor (SC) and the three phase five-level Cascaded H-bridge multilevel inverter (CHBMLI), with the controller based on Newton-Raphson (NR). The switching angle of the (CHB-MLI) with different modulation index MI has been calculated for optimization and non- optimization technique. The created source code programming is then stored in Digital Signal Processing (DSP) TMS320F2812. Experimental step-up has been conducted, whose results confirm the effectiveness of the proposed system in reducing Total Harmonic Distortion (THD) of the (CHBMLI) output.

Key words: Cascaded H-bridge Multilevel Inverter (CHBMLI) · (MI) · Digital Signal Processing (DSP) TMS320F2812 · Newton-Raphson (N.R)

INTRODUCTION

An inverter is used to convert DC power generated from solar modules into AC power. This inverter, known as PV inverter, is an important element and heart of a PV system that functions to convert solar energy into electricity. Improving the output waveform of the inverter reduces its respective harmonic content and hence the size of the filter used and the level of electromagnetic interference (EMI) generated by the inverter's switching operation [1][2]. In recent years, multilevel inverters have become more attractive to researchers and manufacturers, owing to their advantages over conventional PWM inverters. Multilevel inverter concept is used to reduce the harmonic distortion in the output waveform without decreasing the inverter power output. It has several advantages, such as to lower switching frequency and switching losses, lower voltage device evaluation, lower harmonic distortion, increase power quality waveform, higher efficiency and reduce electromagnetic interference (EMI) and interface of renewable energy sources such as photovoltaic PV to the electric power grid [3]. Nowadays, three common topologies of multilevel inverter have been proposed, which are diode-clamped, flying capacitors (FCs) and cascaded H-bridge (CHB). Diode-clamped photovoltaic uses a single dc source rather than multiple sources. Meanwhile, flying capacitor type consists of serial connection of capacitor clamped switching cells. Cascaded H-bridge inverter is a versatile type, which can be serial or parallel connected and also consists of a series of H-bridge cells to synthesize a required voltage from several separate DC sources recoverable from batteries, fuel cells, renewable energy or ultra-capacitor [4][5]. Multilevel boost inverter consists of cascaded H-bridge for hybrid EV (HEV) and electric vehicle (EV) applications implemented without the use of inductors. Currently available power inverter systems for HEVs use in Dc-Dc boost converter to boost the battery voltage for a traditional three-phase inverter have been presented in [6]. Multilevel inverter using cascaded H-bridge inverter with separated dc source (SDCSs) are utiluzed in single phase structure. The output voltage of 5-level cascaded H-bridge multilevel inverter with different switching angle based on Newton-Raphson method is used for angle optimization had been developed by [7]. The harmonic elimination pulse width modulation (SHE-PWM) control pulses are obtained by switching method. A cascaded H-bridge multilevel inverter using iterative Newton-

Corresponding Author: Mohammed Rasheed, Universiti Teknikal Malaysia Melaka, Faculty of Electrical Engineering, Industrial Power, 76100 Hang Tuah Jaya, Durian Tunggal, Melaka, Malaysia. Email: mohamed_tchno@yahoo.com

Raphson (NR) and genetic algorithm (GA) techniques can be used to reduce THD. [8]. Pulse-width modulation (PWM) in multilevel inverter is used to convert DC voltage from battery storage to supply AC loads. Adaptive neuro fuzzy inference (ANFIS) is used to predict the optimum (MI) and switch angles required for a 5-level cascaded H-bridge inverter with improved inverter output voltage [9][10]. Cascaded 5-level inverter is implemented by solving Particle Swarm Optimization (PSO) method non-linear equations through the use of PSO algorithm [11]. OptimizedHarmonic Elimination Stepped Waveform (OHESW) technique to control 7-level output voltage used in a standalone PV. In addition, the Newton-Raphson (NR) method is applied in solving equations to produce the least total harmonic distortion [12]. In this study, multilevel inverter had been adopted and 5-level diode-clamped inverter output voltage was produced by the inverter based on (SC) and battery investigation with PV power plant as experimented by [13][14]. Third Harmonic Injection PWM (THIPWM), or 3-level inverter with performance dynamic integration of (SC) and battery was proposed by [15]. This paper presents a model that employs the Newton Raphson (NR) method to control the three-phase cascaded H-bridge 5-level inverter based on (SC) as storage. Digital Signal Processing (DSP) TMS320F2812 hardware was implemented in the 5-level cascaded H-bridge inverter. The DSP was tested to determine if it is able to verify the retrieved Newton Raphson (NR) control in term of THD.

Cascaded H-Bridge Inverter (CHBI): A three phase 5-level cascaded H-Bridge in a multilevel inverter is shown in Fig 1. It consists of five levels of 8 switches and the three phases share a common Dc bus. Fig 2 shows the output voltage for 5-level (CHB-MLI).

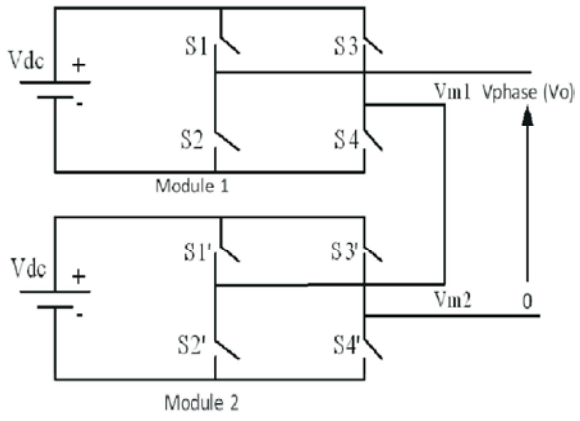

Fig. 1: Phase A: 5-level cascaded H-bridge multilevel inverter [16].

The complementary switch pairs for phase 'A' are (*S1*,*S1*'),(*S2*,*S2*'),(*S3*,*S3*'),(*S4*,*S4*'). These were similar for B and C phases, whereby the cascaded H-Bridge was used to carry full load current. Converting a multi-level of five (*m*-1) level requires control signals, where *m* is the number of voltage levels. Thus, in this implementation, the controller of five, four control signals were required. Sine wave voltage was produced through a series of H-bridge inverters connected to a multilevel converter architecture, based on a series of inverters which consist of three phases of H-Bridge. Each cell is supplied by the converter from the DC source. The structure is related to the level of five inverters that consist of 8 switches in one leg, which gates cascaded H-bridge in three-phase inverter with arm 2*N*+1. A three phase (CHB-MLI) is illustrated in Fig. 2.

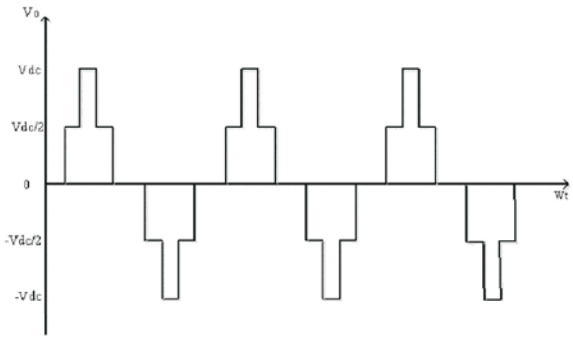

Fig. 2: Output voltage waveforms of a 5-level Cascaded H-Bridge

The switching angles can be optimized by adjusting them to reduce the total harmonic distortion. Compared to flying capacitor or diode imposed, the development of inverter is cheaper. This is because, multi-level inverters are very small in term of the number of its components.

Inverter Analysis Based On Newton-Raphson (N.R) Method: The Fourier series for the total output voltage of (CHB-MLI) is described in Equation (1). Two-source circuits contain only odd-numbered harmonic and is

$$V_o = \frac{4V_{dc}}{\pi}\sum_{n=1,3,5,7,9,\ldots}^{\infty}[\cos(N\theta_1) + \cos(N\theta_2)]\frac{\sin(n\omega_0 t)}{n} \quad (1)$$

The (MI) is the ratio of the amplitude of the fundamental frequency component of to the amplitude of the fundamental frequency component of a square wave of amplitude, which is 2(). The expression in Equation (2) describes

$$m_i = \frac{V_1}{2(4V_{dc}/\pi)} \quad (2)$$

For the two separate dc source inverter, harmonic N can be eliminated by using delay angles, as

$$\cos(N\theta_1) + \cos(N\theta_2) = 0 \quad (3)$$

Newly formed equation derived from Equation (1) for simultaneous solution is required to eliminate Nth harmonic and meet a specified (MI), becoming

$$\cos(\theta_1) + \cos(\theta_2) = 2m_i \quad (4)$$

These harmonic Equations (3) and (4) are transcendental equations. Solving these simultaneous equations requires an iterative numerical method. Newton-Raphson technique is a method that can be employed to solve Equations (5) and (6).

$$x_1 + x_2 = 2m_i \quad (5)$$

$$(4x_1^3 - 3x_1) + (4x_2^3 - 3x_2) = 0 \quad (6)$$

Based on Equations (1) to (5), a source code had been created using C language for optimization and non-optimization and then stored in Digital Signal Processor (DSP) TMS320F2812.

Controller Development Using Digital Signal Processor (DSP) TMS320F2812: Based on the method as mentioned above, the source code was created using C programming and stored in Digital Signal Processor (DSP) TMS320F2812. The main frequency of the processor was 150 MHz, as shown in Fig. 3. TMS 320F2812 controllers integrate a complete set of control system capabilities, such as Pulse Width Modulation (PWM) generation, time sampling, sensor capture, analog to digital conversion (ADC) and data storage into a single device and reduction of system cost, board space and system complexity.

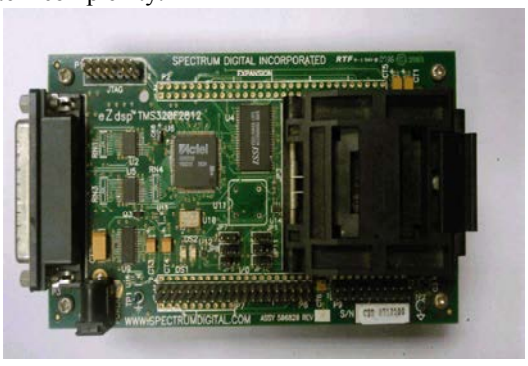

Fig. 3: DSP TMS320F2812.

The DSP was modeled from eZdspTM F2812 based on the Texas Instruments TMS320F2812 DSP produced by Spectrum Digital Incorporated and was to verify the control algorithms proposed for the proposed DVR. The TMS320F2812 was selected as it has a 32-bit CPU performing at 150 MHz [Processors, 2006]. Among its interesting features, which prove to be very beneficial in this research, is the 12-bit A/D module handling 16 channels and two on-chip event manager peripherals, which provide a broad range of functions and particularly useful in applications of control. The architecture of the TMS320F2812 DSP from Texas Instruments is summarized in the diagram in Fig. 4.

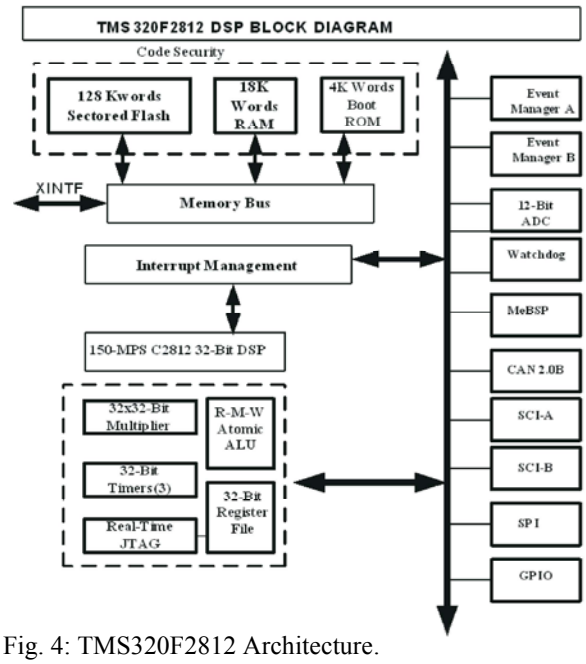

Fig. 4: TMS320F2812 Architecture.

SC As an Energy Storage: A basic circuit configuration and its components of SC is shown in Fig. 5. [17].

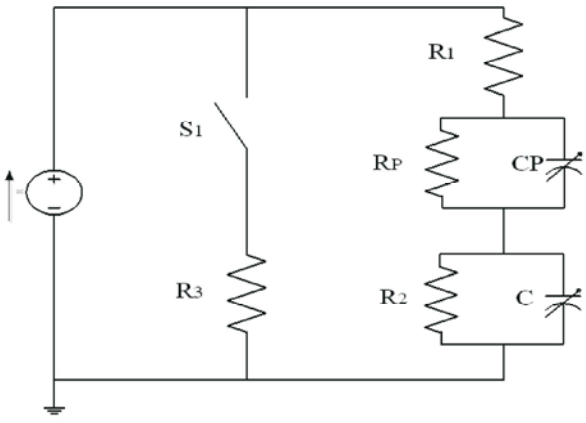

Fig. 5: The Basic Circuit Model of the (SC) (EPOCS).

In this study, the design integrates SC instead of battery because of it is insufficient to supply real power charge and discharge conditions. SC uses circuit RC connected series formed by a capacitor constant and a resistance constant. The capacitance and serial resistance of the (SC) are dependent on frequency, temperature and voltage. (SC) can be supplied to high voltage charge, thus discharge can be neglected since the frequency, temperature and voltage are constant and high performance SC prototype can reduce THD. Capacitance C is responsible for the most important phenomenon in the circuit. Resistance R2 that is connected in parallel with the capacitor is meant to represent the self-discharge effect. Series resistance R1 represents the losses during charge and discharge. These losses occur due since the conducting element in the (SC) has a resistance, thus the connection is not ideal. The over-voltage protection provided by R3 and the switch controlling its connection to the circuit are necessary to prevent damage to the capacitor elements by balancing the voltage level. The voltage balancing is needed, otherwise the voltage in one separate cell can increase higher than the others, resulting in gassing or explosion. Voltage difference occurs when one cell has a lower capacitance than the others, since those results in more energy being stored. Resistance Rp and capacitance Cp are included in the circuit to model some of the fast dynamics in the behavior of the SC.

$$R1 = \frac{\Delta u}{\Delta i} \tag{7}$$

$$R3 = \frac{\Delta t}{-\ln\left(\frac{V_A}{V_*}\right)C} \tag{8}$$

$$u(t) = \int \frac{i(t)}{C} dt \tag{9}$$

A simple circuit initial model testing can be done by connecting a capacitance and resistance in parallel with a resistance in series. This base circuit can show the basic function of the SC[18][17]. By adding more components until the circuit as described in Fig. 4 is achieved, the accuracy of the model can be improved. The control block relays the switch that connects the resistance balancing R3 to the circuit [19].The value of capacitance can be calculated in two different ways. The first methodis to look at the voltage derivative during charging of the SC. The relation between capacitance is

$$i(t) = C\frac{d}{dt}u(t) \tag{10}$$

The relation between capacitance can be calculated for different parts of the voltage curve. When highcurrents are used, other effects than the capacitance can affect the voltage level. These effects can cause the value of calculated capacitance to be incorrect [20].

Experimental Setup: The experimental setup comprised of 5-level CHB-MLI SC as a storage and DSP TMS320F2812, as shown in Fig. 6. The proposed CHB-MLI was interfaced with DSP TMS320F2812 to get the output voltage waveform of 5-level CHB-MLI. The DSP TMS320F2812 target board was used to generate the switching signal for the proposed inverter based on SC. The TMS320F2812 board control generates pulse for the switching signal for the proposed inverter. Two source programming codes based on Newton Raphson controller had been created for optimization andNon-optimization of CHB-MLI with different MI. The voltage output of the five-level multilevel inverter was 300 volts with frequency 50Hz. The gate drive for 5-level three-phase cascaded H-bridge multilevel inverter was designed with combination of gate drive circuit. This gate drive had been tested using DSP TMS320F2812 implementation based on coding to get the output waveform from IGBT.

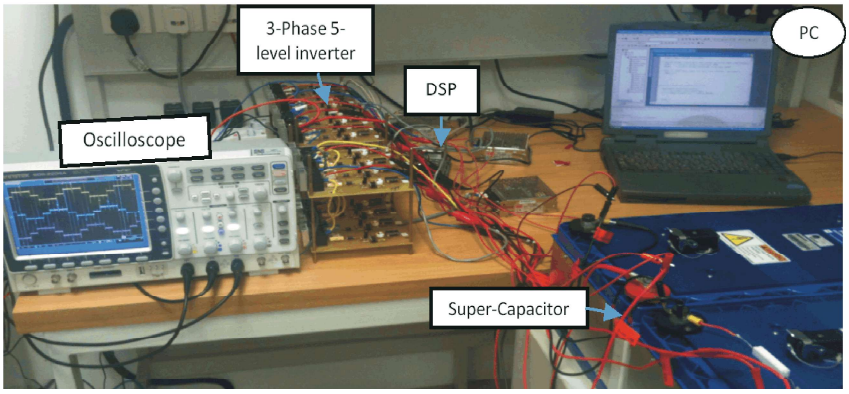

Fig. 6: Prototype of 5-Level Cascaded H-Bridge Inverters.

Result of Optimized 5-Level CHB-MLI: In case of optimization technique, a source code had been created using C programming and stored into DSP TMS320F2812. The DSP was then interfaced with CHB-MLI. The SC as an energy storage was applied to CHB-MLI. In the source code programming, one cycle of duration of time is equal to 0.02s with MI equal to 0.84. The switching angles were θ_1= 17.06° and θ_2= 43.53° at upper and lower switches of CHB-MLI. Fig. 7 to Fig. 12 show the timing diagram of phase A, B and Phase C. Each phase comprised of switches S_1 S_2 S_3 andS_4 and S_5 S_6 S_7 andS_8 for the upper switches and lower switches. From Fig. 7 to Fig. 12, it can be noted that the upper and the lower switches for each phase had equal switching period.

Fig. 7: Upper Switches: Timing Diagram for S1, S2, S3 and S4 for Phase A with MI=0.84 for θ1=17.060°, θ2=43.530°.

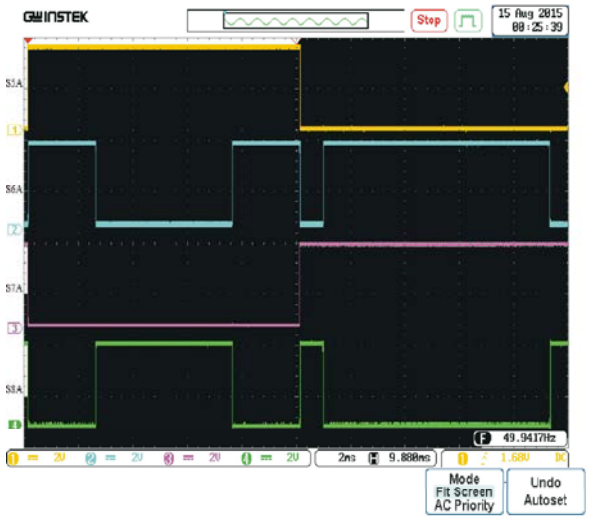

Fig. 8: Lower Switches: Timing Diagram for S5, S6, S7 and S8 for Phase A with MI=0.84 for θ1=17.060°, θ2=43.530°.

Fig. 9: Upper Switches: Timing Diagram S1, S2, S3 and S4 for phase B with MI=0.84 θ1 =17.060°, θ2=43.530°.

Fig. 10: Lower Switches: Timing Diagram S5, S6, S7 and S8 for Phase B with MI=0.84 for θ1 =17.060°, θ2 =43.530°.

Fig. 11: Upper Switches: Timing Diagram S1, S2, S3 and S4 for Phase C with MI=0.84 for θ1=17.060°, θ2 =43.530°.

Fig. 12: Lower Switches: Timing Diagram S5, S6, S7 and S8 for Phase C With MI=0.84 for $\theta 1=17.06^0$ $\theta 2=43.53^0$.

Figure 13 shows the optimization voltage output waveform of 5-level CHB-MLI for Phase A, Phase B and Phase C, respectively. The optimization voltage output waveforms for each phase of CHB-MLI based on (MI) was equal to 0.84 were very smooth due to accurate calculation of switching angles. Fig. 14 shows the harmonic spectrum of optimization voltage output waveform of CHB-MLI with THD value equal to 15.5%.

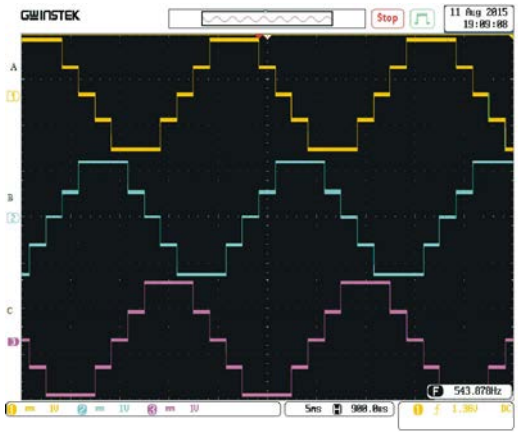

Fig. 13: Output Voltage 5-Level Cascaded Multilevel Inverter MI=0.84.

Figure 15. shows the optimization current output waveform of 5-level CHB-MLI for Phase A, Phase B and Phase C, respectively. The optimization current output waveforms for each phase of CHB-MLI was very smooth due to accurate calculation of switching angles. Fig.16 shows the harmonic spectrum of optimization current output waveform of CHB-MLI with THD value equal to 3.9% based on (MI) and equal to 0.84.

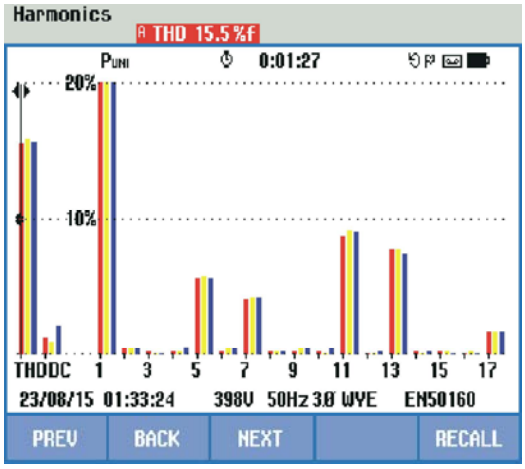

Fig. 14: FFT Analysis Output Voltage 5-level inverter MI=0.84

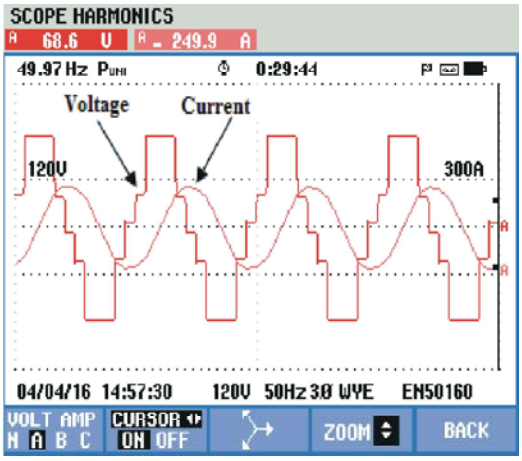

Fig. 15: Optimization Current Output Wave form of 5-Level CHB-MLI with MI=0.84.

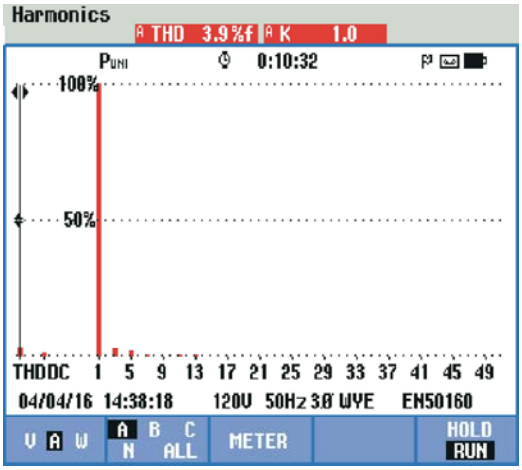

Fig. 16: Optimization Harmonic Spectrum of Current Output Waveform of CHB-MLI with MI=0.84.

Result of Non-Optimized 5-Level CHB-MLI: Similar with optimization technique, a source code for non-optimization was also created with MI set to 0.58 andswitching angles set to θ_1=,and θ_2=77.94^0. The upper and lower switches Timing Diagram for Phase A, Phase B and Phase C with MI=0.58 for θ_1= and θ_2=77.94^0 can be seen from Fig 17 to Fig 22.

Fig. 17: Upper Switches: Timing Diagram for S1, S2, S3 and S4 for Phase A with MI=0.58 for θ1=17.955^0, θ2=77.948^0.

Fig. 20: Lower Switches: Timing Diagram S5, S6, S7 and S8 for Phase B with MI=0.58 for θ1=17.955^0, θ2=77.948^0.

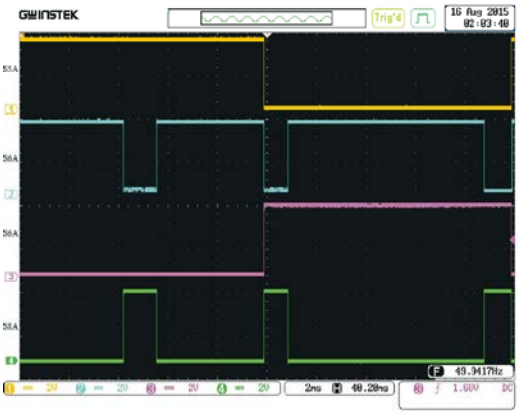

Fig. 18: Lower Switches: Timing Diagram S5, S6, S7 and S8 for Phase A with MI=0.58 for θ1=17.955^0, θ2=77.948$_0$.

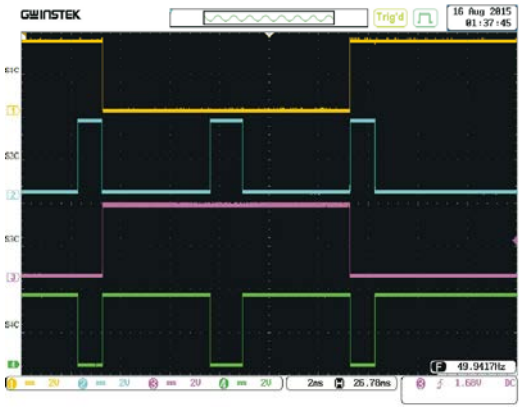

Fig. 21: Upper Switches: Timing Diagram S1, S2, S3 and S4 for Phase C with MI=0.58 for θ1=17.955^0 θ2=77.948^0.

Fig. 19: Upper Switches: Timing Diagram S1, S2, S3 and S4 for Phase B with MI=0.58 for θ1=17.955^0 θ2=77.948^0.

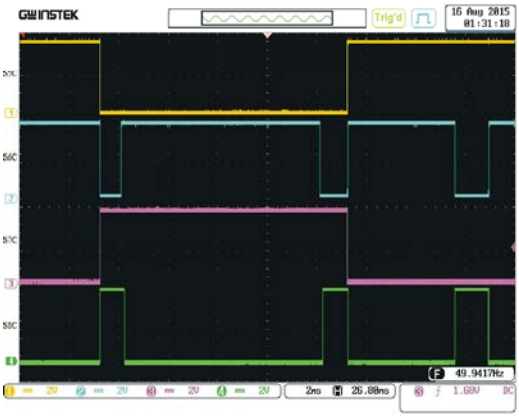

Fig. 22: Lower Switches: Timing Diagram S5, S6, S7 and S8 for Phase C With MI=0.58 for θ1=17.955^0, θ2=77.948^0.

The obtained waveform of the five level CHB-MLI Fig. 23 shows the non-optimization voltage output waveform of 5-level CHB-MLI for Phase A, Phase B and Phase C, respectively. The non-optimization voltage output waveforms for each phase of CHB-MLI based on MI equal to 0.58 were not smooth due to inaccurate calculation of switching angles. Fig. 24 shows the harmonic spectrum of non-optimization voltage output waveform of CHB-MLI with THD value equal to 31.2%.

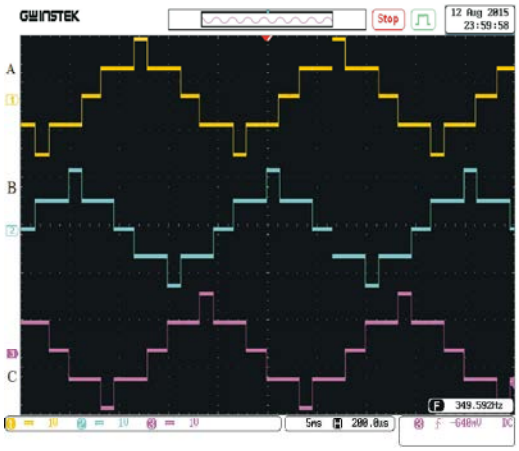

Fig. 23: Output Voltage of Non-Optimized 5-Level Cascaded Multilevel Inverter Ma=0.58.

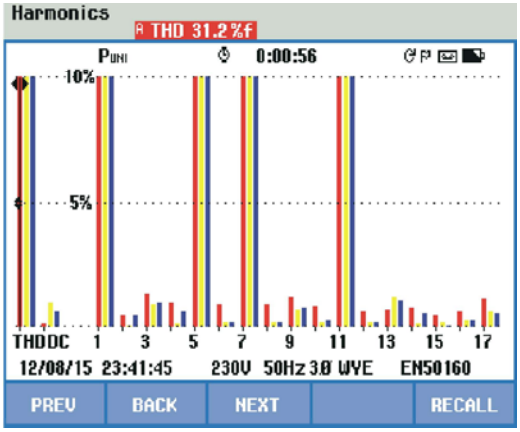

Fig. 24: FFT Analysis Output Voltage of Non-Optimized 5-level inverter Ma=0.58.

Figure 25 shows the non-optimization current output waveform of 5-level CHB-MLI for Phase A, Phase B and Phase C, respectively. The non-optimization current output waveforms for each phase of CHB-MLI were very smooth due to accurate calculation of switching angles. Fig. 26 shows the harmonic spectrum of non-optimized current output waveform of CHB-MLI with THD value equal to 8.2%. based on (MI) equal to 0.58.

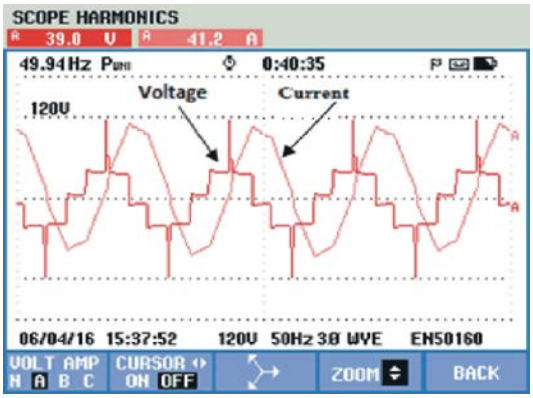

Fig. 25: Non-Optimized Current Output Waveform of 5-Level CHB-MLI with MI=0.58.

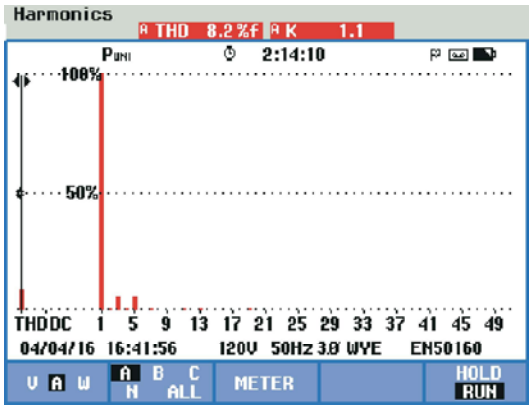

Fig. 26: Non- Optimized Harmonic Spectrum of Current Output Waveform of CHB-MLI with MI=0.58.

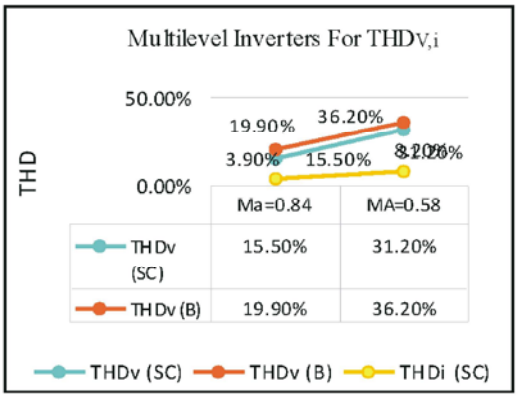

Fig. 27: Comparison between Super-Capacitor (SC) and Battery for different (MI) of 5-Level Inverter for Harmonic Reduction.

Figure 27 presents the comparison between (SC) and Batteryof (MI) inverters to control total harmonic distortion for voltage and current. The THD measurement for five level of three phase CHB-MLI with different (MI) can be observed as shown in Table.1.

Table 1: THD Measurement for the System.

MI	THD Current	H_i3^{rd}	H_i5^{rd}	THD Voltage
0.84	3.9%	2.2%	1.7%	15.5%
0.58	8.2%	6.2%	6.2%	31.2%

CONCLUSION

A three-phase 5-level CHB-MLI based on SC as a storage has been developed and tested. The source codes using C language based on NR controller for optimization and non-optimization have been created and stored in DSPTMS320F2812. This controller is then interfaced with the proposed prototype of CHB-MLI. A test on the proposed hardware with its controller shows that the voltage and current output waveform of the CHB-MLI are capable to reduce harmonic, which meets IEC standard. Thus, the proposed prototype of CHB-MLI based on SC as a dc energy source has been successfully created and has achieved the objective of this study.

ACKNOWLEDGMENT

The authors wish to thank Universiti Teknikal Malaysia Melaka (UTeM) for Fellowship award and Ministry of Higher Education, Malaysia (MOHE) for supporting this research under the grant FRGS/2/2014/TK/FKEF/01/F00238.

REFERENCES

1. Sangeetha, B. and K. Geetha, 2014. Performance of multilevel shunt active filter for smart grid applications, Int. J. Electr. Power Energy Syst., 63: 927-932.
2. Rosli. Omar, Mohammed. Rasheed, Ahmed. Al-janad, Marizan Sulaiman and Zulkifilie. Ibrahim, 2014. Harmonic Reduction Comparison in Multilevel Inverters for Industrial Application, 63(3): 570-578.
3. Omar Abdel-Rahima, Haitham Abu-Ruba and Abdellah Kouzouc Texas, 2013. Nine-to-Three Phase Direct Matrix Converter with Model Predictive Control for Wind Generation System, Energy Procedia, 42: 173-182.
4. Sanchez Reinosoa, C.R., M. De Paula, D.H. Milone and R.H. Buitrago, 2012. Photovoltaic Inverters Optimisation, Energy Procedia, 14: 1484-1489.
5. Ilhami Colak, Ramazan Bayindir and Ersan Kabalci, 2010. Design and Analysis of a 7-Level Cascaded Multilevel Inverter with Dual SDCSs, SPEEDAM 2010 Int. Symp. Power Electron. Electr. Drives, Autom. Motion, pp: 180-185.
6. Zhong Du, Burak Ozpineci, Leon M. Tolbert and John N. Chiasson, 2009. DC - AC Cascaded H-Bridge Multilevel Boost Inverter With No Inductors for Electric / Hybrid Electric Vehicle Applications, IEEE Trans. Ind. Appl. VOL. 45, NO. 3, MAY/JUNE 2009, 45(3): 963-970.
7. Rosli omar, Afiqah Sabari and Marizan Sulaiman, 2015. Harmonic Reduction of Cascaded H-Bridge Multilevel Inverter Based on Newton-Raphson, International Journal of Recent Technology and Engineering (IJRTE) 10(3): 6569-6580.
8. Aman Parkash1 S.L. Shimi and S. Chatterji, 2015. Harmonics Elimination in Cascade Multilevel Inverters Using Newton-Raphson and Genetic Algorithm Harmonics Elimination in Cascade Multilevel Inverters Using Newton- Raphson and Genetic Algorithm," IJSRD - International Journal for Scientific Research & Development no. July, pp: 0-4.
9. Sumithira, T.R. and A. Nirmal. Kumar, 2013. Elimination of Harmonics in Multilevel Inverters Connected to Solar Photovoltaic Systems Using ANFIS?: An Experimental Case Study, Journal of Applied Research and Technology, 11: 124-132.
Engineering, E., 2013. New Cascaded H-bridge Multilevel Inverter with Improved Efficiency, 2(4): 1263-1271.
10. Gobinath, K., S. Mahendran and I Gnanambal, 2013. New Cascaded H-bridge Multilevel Inverter with Improved Efficiency, 2(4): 1263-1271.
11. Baharuddin Ismail, Syed Idris Syed Hassan, Rizalafande Che Ismail, Abdul Rashid Haron and Azralmukmin Azmi, 2014. Selective Harmonic Elimination of Five-level Cascaded Inverter Using Particle Swarm Optimization, International Journal of Engineering and Technology (IJET), 5(6): 5220-5232.
12. Krismadinataa, Nasrudin Abd Rahima, Hew Wooi Pinga and Jeyraj Selvaraja, 2013. Elimination of Harmonics in Photovoltaic Seven-level Inverter with Newton-raphson Optimization, Procedia Environ. Sci., 17: 519-528.
13. LI,2, P., Ph. Degobert, B. François and B. Robyns, 2008. Multi-Level Representation for the Control Design of a Super Capacitor Storage System for a Microgrid Connected Application Key words, International Conference on Renewable Energies and Power Quality (ICREPQ'16).
14. Venus, V. and K. Ramani, 2013. Implementation of SVPWM technique based diode clamped five-level inverter direct integration scheme for photovoltaic systems, 2013 IEEE Int. Conference. Emerg. Trends Comput. Commun. Nanotechnol., ICECCN, 1: 420-425.

15. Jianwei Ma, 2 Shanshan Chen, 2014. 'The Research of Super Capacitor and Battery Hybrid Energy Storage System with the THIPWM," Sensors & Transducers, 165(2): 150-154.
16. Karuppanan, P. and Kamala Kanta Mahapatra, 2011. Cascaded Multilevel Inverter based Active Filter for Power Line Conditioners using Instantaneous Real-Power Theory, India Int. Power Electron., 769008: 1-6.
17. Data sheet for super capacitor from EPCOS with Part No.: B48621-S0203-Q288.
18. Mohammed, Rasheed, Rosli. Omar and Marizan. Sulaiman, 2015. Harmonic Reduction in Multilevel Inverter Based on Super Capacitor as a Storage, TELKOMNIKA Indonesian Journal of Electrical Engineering no. December, pp: 520-530.
19. Ahmed Al-janad, Rosli Omar, M. Rasheed, Z. Ibrahim and M.H.A. Mustapha, 2014. Analysing Performance of Super-capacitor and Battery in Low Voltage Electrical, 61(1): 99-106.
20. Stephan Buller, Marc Thele and Rik W.A.A. De Doncker and Eckhard Karden, 2005. Impedance-Based Simulation Models of Supercapacitors and Li-Ion Batteries for Power Electronic Applications, pp: 742-747.