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Large Signal Modeling of DC-DC Converter with Multiplier Cells for High Voltage Generation

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Abstract: This paper presents the large signal model of a transformerless DC-DC Converter with Cockcroft – Walton Multiplier (CWM) circuit for high voltage DC generation. State space approach to each mode of operation is defined and constructed the proposed large signal model of the DC-DC boost converter with Multiplier cells. This model can be used to analyze the circuit and design a control module. Transfer function of the proposed model is obtained and the value of capacitance is optimized for critical damping. Variation of output voltage with duty ratio is also plotted through large signal modeling. The stability of the circuit for the designed parameters under open loop is analyzed using Pole-Zero plot.

Key words: DC-DC Converter · Large Signal Modeling · Cockcroft Walton Multiplier Circuit · Pole-Zero Plot · Duty Cycle · State Space Approach

INTRODUCTION

The natural resources in the world is reducing fast and there is a requirement of more renewable energy sources since demand for power is continuing to be on an increasing trend [1, 2]. Among the available renewable energy sources, photovoltaic (PV) sources are cheap and abundant [3]. But the voltages generated in these sources are quite low in magnitude and cannot be utilized for many applications. Boost converters can be used to increase the voltage from lower level to higher level [4, 5]. Transformers are normally not preferred well in modern converter circuits due to the high leakage inductance produced by the windings. Moreover, the switches in the converter circuits become burdened with more stress especially during turn off instant. This requires higher voltage rating switches and the entire system become expensive. In addition, the complex design of high frequency transformer leads to transformerless boost converters [6].

Cascaded boost converters are very simple and robust in structure. High voltage gain can be obtained by diode-inductor or diode-capacitor modules. The proposed system replaces the transformer with a voltage multiplier circuit and operates in CCM, thereby reduces the switching losses and switching stress.

The Average signal model of the proposed system is constructed for the analysis and control purpose.

Proposed System: Cockcroft Walton Multiplier is the combination of diodes and capacitance used for generating very high dc voltage from a low voltage AC. A DC- AC boost converter in connection with Cockcroft Walton multiplier circuit gives simplest and easiest way to produce high DC voltage [7]. The absence of transformer in the circuit leads to low voltage rated switches and capacitors [8]. This circuit can be extended to any number of stages for high output voltage. The input to the CWM circuit is fed from a DC to AC converter as shown in Figure 1.

The converter circuit consisting of four IGBT switches (Sa_1, Sa_2, Sb_1, Sb_2) in which two are working independently under same frequencies. Sa_1 (Sb_1) and Sa_2 (Sb_2) are operating in complementary mode. The main disadvantage of CWM circuit is its high ripple at low frequency (50Hz to 60Hz) inputs. This circuit can be used in particle accelerators, x-ray machines, television sets, photocopiers, insulation test and electrostatic coating.

Sa_1, Sa_2 helps in boosting operation by controlling inductor energy and Sb_1, Sb_2 provides ac supply to the input of CWM circuit. Sb_1 and Sb_2 work under high frequency so that the size of inductor and capacitor can be reduced.

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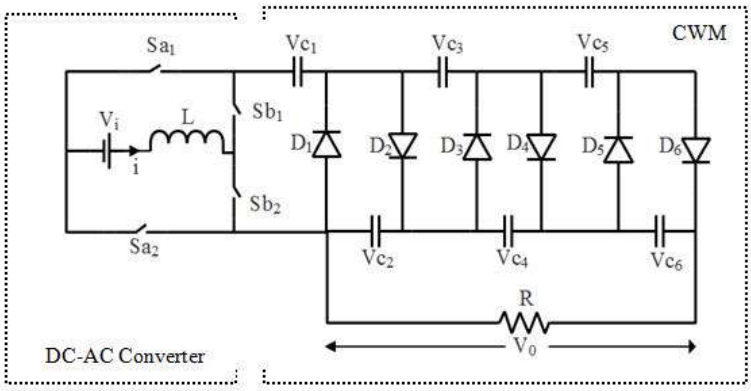

Fig. 1: DC-DC Converter with 3 stage Cockcroft Walton Voltage Multiplier Circuit

Average Large Signal Model: The proposed system works in four different modes. The assumptions considered for the operation of the circuit are

- Power loss in all the circuit elements is Nil.
- Voltage across all the capacitors except first capacitor is same.

Large signal model is developed for each mode of switching operation having different states. Hence the proposed averaged large signal model is constructed for the entire circuit.

The mathematical model of the circuit can be expressed in terms of state space equations [8] are given in equation 1 and 2

$$\dot{x} = AX + Bu \tag{1}$$

$$y = CX + Du \tag{2}$$

The state variables (x_0, x_1..... x_6) taken for the circuit shown in figure 1 are (i, Vc_1….. Vc_6). The equation 3 gives the state variable matrix.

$$X = \begin{bmatrix} x_0 \\ x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \end{bmatrix} = \begin{bmatrix} i \\ V_{c1} \\ V_{c2} \\ V_{c3} \\ V_{c4} \\ V_{c5} \\ V_{c6} \end{bmatrix} \tag{3}$$

where ‘i’ is the source current through inductor and Vc_1, Vc_2, Vc_3, Vc_4, Vc_5 and Vc_6 are the capacitor voltages across C_1, C_2, C_3, C_4, C_5 and C_6 respectively. The input matrix ‘U’ is given by the equation 4.

$$U = \begin{bmatrix} V_i \\ I_z \end{bmatrix} \tag{4}$$

V_i is the input voltage and i_z is the load disturbance current. Load disturbance is considered for variable load conditions.

The output matrix, ‘Y’ of the proposed circuit contains the variables ‘V_o’, the output load voltage and input current ‘i’ described by equation 5.

$$Y = \begin{bmatrix} V_o \\ i \end{bmatrix} \tag{5}$$

Mode of Operations:

Mode 1 (Sa_1 and Sb_1 are ON, Sa_2 and Sb_2 are OFF): The mode of operation shown in figure 2, the switches Sb_1 is ON for a duration of $T_1/2$ and ON for both Sa_1 and Sb_1 for d•($T_1/2$), where T_1 and T_2 are the switching time period of Sb_1 and Sa_1 respectively and‘d’ is the duty ratio of the switch Sa_1 during positive conducting period. The pulse waveforms for all switches are shown in Figure 3, simulated by MATLab, considering horizontal axis as time.

For the duration of ‘$dT_1/2$’, the inductor will charge with current ‘i’ shown in figure 2(a) and C_2, C_4 and C_6 (even capacitors) will discharge to load as shown in figure 2 (b). All other capacitors are in floating stage.

State space constants A, B, C and D of mode 1 are derived from the figure 2. From figure 2(a)

$$\dot{x}_0 = \frac{V_i}{L} \tag{6}$$

and from figure 2(b)

$$\dot{x}_2 = -\frac{x_2}{RC} - \frac{x_4}{RC} - \frac{x_6}{RC} - \frac{I_z}{C} \tag{7}$$

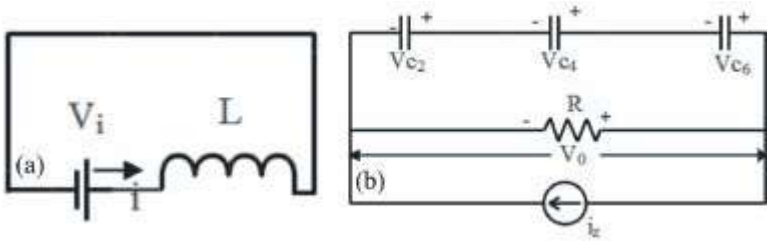

Fig. 2: Mode 1 operation

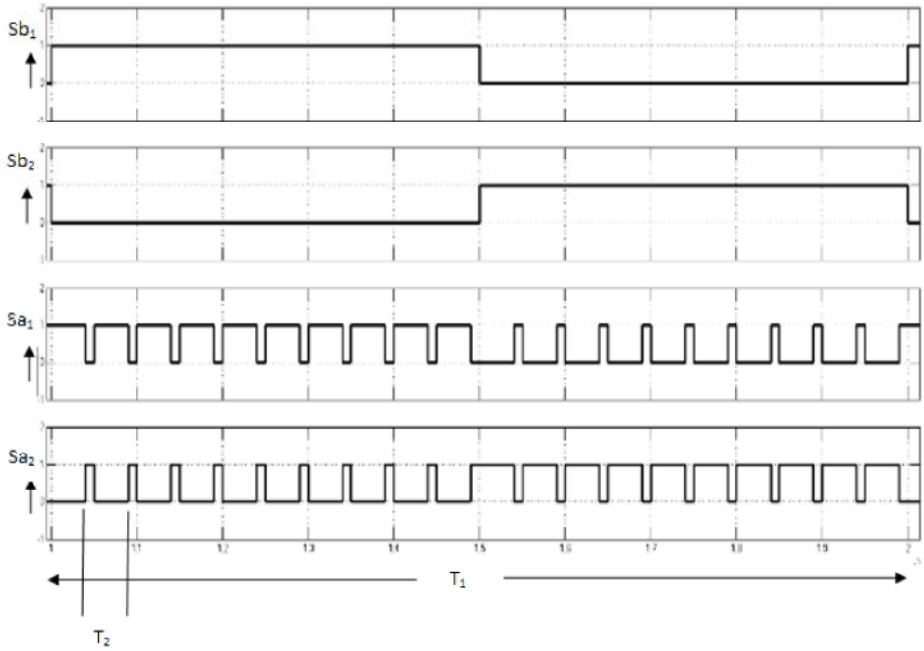

Fig. 3: Switching pulses to the proposed converter

Similarly,

$$\dot{x}_4 = \dot{x}_6 = -\frac{x_2}{RC} - \frac{x_4}{RC} - \frac{x_6}{RC} - \frac{I_z}{C} \quad (8)$$

The equations (9) and (10) are constructed from the equations (6), (7) and (8) describes the state space model of mode1.

$$\dot{X} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{RC} & 0 & \frac{-1}{RC} & 0 & \frac{-1}{RC} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{RC} & 0 & \frac{-1}{RC} & 0 & \frac{-1}{RC} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{RC} & 0 & \frac{-1}{RC} & 0 & \frac{-1}{RC} \end{bmatrix} \begin{bmatrix} x_0 \\ x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & 0 \\ 0 & \frac{-1}{C} \\ 0 & 0 \\ 0 & \frac{-1}{C} \\ 0 & 0 \\ 0 & \frac{-1}{C} \end{bmatrix} \begin{bmatrix} V_i \\ I_z \end{bmatrix} \quad (9)$$

$$\begin{bmatrix} V_o \\ i \end{bmatrix} = Y = \begin{bmatrix} 0 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} [X] \quad (10)$$

The state matrix represents A_1, input matrix as B_1 and output matrix as C_1 are considered for further explanation.

Mode 2 (Sa_2 and Sb_1 are ON, Sa_1 and Sb_2 are OFF): Both the switches are ON for a duration of ((1-d)/2) T_1. Three different states of operations are considered with respect to the conduction of Diodes. State Space is separately constructed for each state and averaged for getting Mode 2 space model.

State A: D_6 is conducting; the condition for conduction is $Vc_5 > Vc_6$ and $Vc_3 > Vc_4$. Capacitors C_2, C_4 and C_6 are charging by the incoming current towards CWM circuit and Capacitors C_1, C_3 and C_5 are discharging. The circuit for conduction is shown in Figure 4.

State B: D_4 is conducting; the condition for conduction is $Vc_5 = Vc_6$ and $Vc_3 > Vc_4$. Capacitors C_2 and C_4 are charging, C_6 supply the load current and

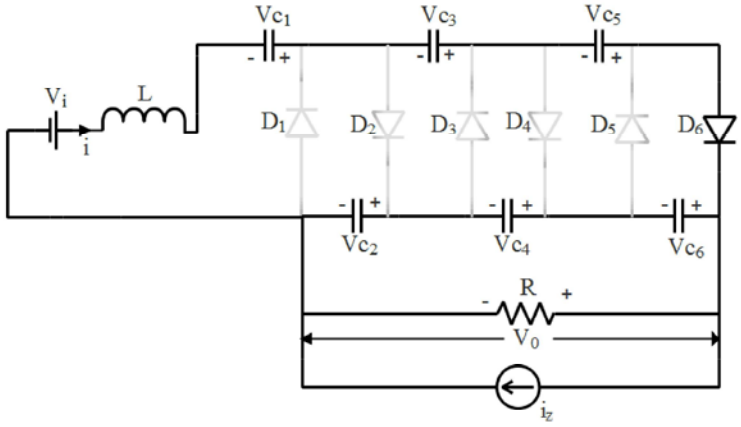

Fig. 4: Mode 2, State A Operation

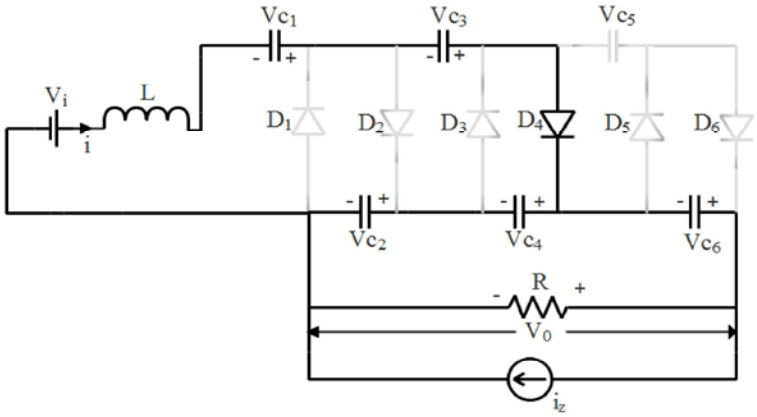

Fig. 5: Mode 2, State B Operation

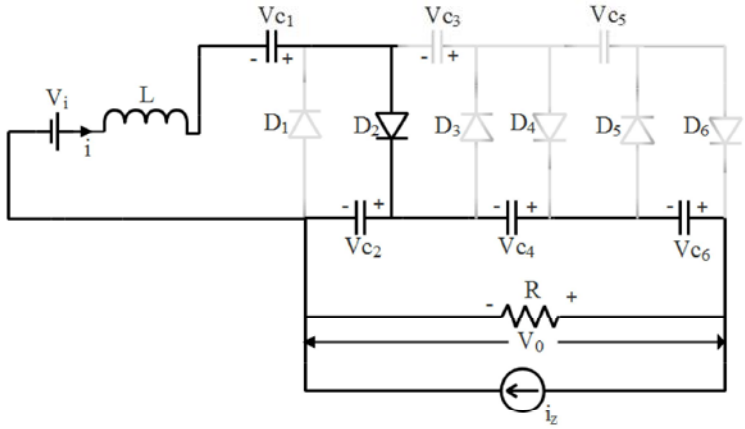

Fig. 6: Mode 2, State C Operation

the capacitors C_1 and C_3 are discharging. Capacitor C_5 is in floating stage. The circuit for conduction is shown in Figure 5.

State C: D_2 is conducting; the condition for conduction is $Vc_5 = Vc_6$ and $Vc_3 = Vc_4$. Capacitor C_2 is charging, C_4 and C_6 supply the load current and the capacitor C_1 is discharging. Capacitors C_3 and C_5 are floating. The circuit for conduction is shown in Figure 6.

Let the State Matrices for the states A, B, C are A_2', A_2'', A_2''' respectively. Similarly, Input matrices are considered as B_2', B_2'', B_2''' and output matrices are C_2', C_2''

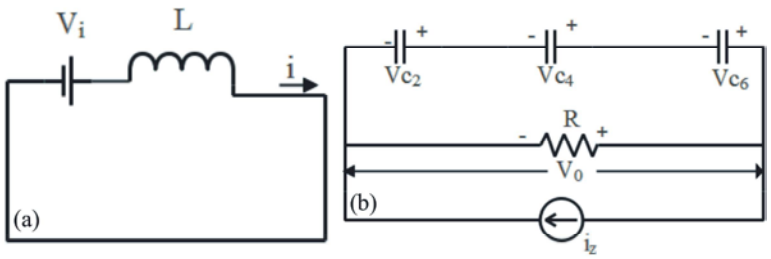

Fig. 7: Mode 3 operation

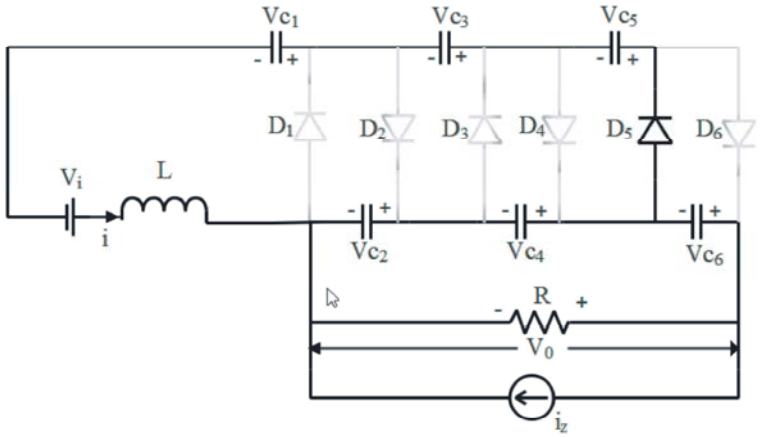

Fig. 8: Mode 4, State A Operation

and C2'''for state A, B and C. The average value of A_2, B_2 and C_2 for mode 2 are obtained by the equations (11), (12) and (13).

$$A_2 = \frac{A_2' + A_2'' + A_2'''}{3} \quad (11)$$

$$B_2 = \frac{B_2' + B_2'' + B_2'''}{3} \quad (12)$$

$$C_2 = \frac{C_2' + C_2'' + C_2'''}{3} \quad (13)$$

Mode 3 (Sa_2 and Sb_2 are ON, Sa_1 and Sb_1 are OFF): All diodes are turned OFF and the inductor is charged from dc input source during this time period as shown in Figure 7(a)**.** C_2, C_4 and C_6 (even capacitors) will supply to load as shown in Figure 7 (b). All other capacitors are in floating stage.

The state matrix A_3, input matrix B_3 and output matrix C_3 are calculated for the above mode of operation.

Mode 4 (Sa_1 and Sb_2 are ON, Sa_2 and Sb_1 are OFF): Three different states of operations are considered with respect to the conduction of Diodes. State Space is separately constructed for each state and averaged for getting Mode 4 space model.

State A: D_5 is conducting; Capacitors C_1, C_3 and C_5 are charging by the incoming current towards CWM circuit and Capacitors C_2 and C_4 are discharging. C_6 supplies the load current. The circuit for conduction is shown in Figure 8.

State B: D_3 is conducting; Capacitors C_1 and C_3 are charging, C_4 and C_6 supply the load current and the capacitor C_2 is discharging. Capacitor C_5 is in floating stage. The circuit for conduction is shown in Figure 9.

State C: D_1 is conducting; Capacitor C_1 is charging, Capacitors C_2, C_4 and C_6 supply the load current and the capacitor C_3 and C_5 are in floating mode. The circuit for conduction is shown in Figure 10.

Let the State Matrices for the states A, B, C are A_4', A_4'', A_3''' respectively. Similarly, Input matrices are considered as B_4', B_4'', B_4''' and output matrices are C_4', C_4'' and $C_4'''$for state A, B and C. The average value of A_4, B_4 and C_4 are obtained by the equations (14), (15) and (16).

$$A_4 = \frac{A_4' + A_4'' + A_4'''}{3} \quad (14)$$

$$B_4 = \frac{B_4' + B_4'' + B_4'''}{3} \quad (15)$$

$$C_4 = \frac{C_4' + C_4'' + C_4'''}{3} \quad (16)$$

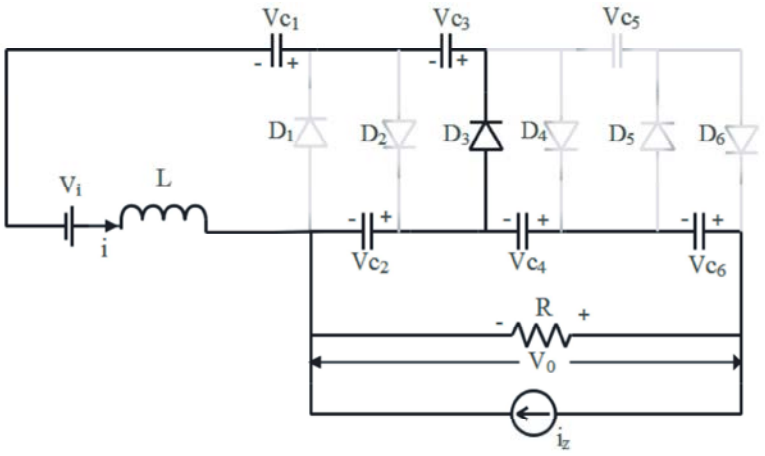

Fig. 9: Mode 4, State B Operation

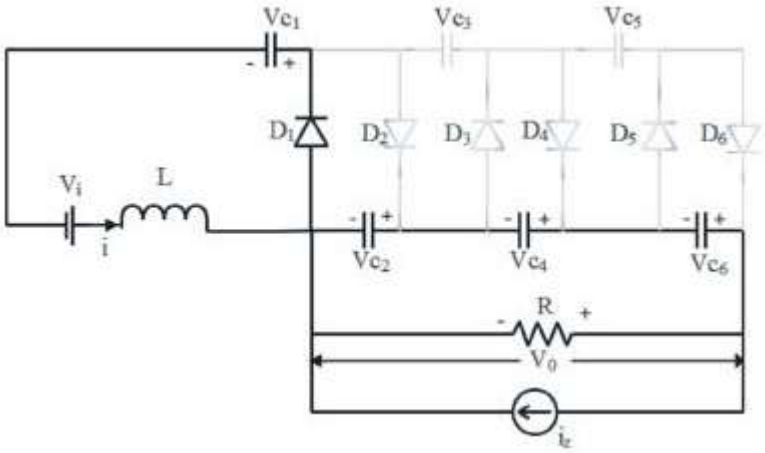

Fig. 10: Mode 4, State C Operation

RESULTS

The average value of A, B and C is constructed from the equations (17), (18) and (19)

$$A_{av} = A = (A_1 + A_3)\frac{d}{2} + (A_2 + A_4)\left(\frac{1-d}{2}\right) \quad (17)$$

$$B_{av} = B = B_1\frac{d}{2} + B_2\frac{(1-d)}{2} + B_3\frac{D}{2} + B_4\frac{(1-d)}{2} \quad (18)$$

Similarly,

$$C_{av} = C = C_1\frac{d}{2} + C_2\frac{(1-d)}{2} + C_3\frac{d}{2} + C_4\frac{(1-d)}{2} \quad (19)$$

The proposed State Space Model of the circuit is constructed and shown in equations (20) and (21)

$$\dot{X} = \begin{bmatrix} 0 & 0 & \frac{-(1-d)}{6L} & 0 & \frac{-(1-d)}{6L} & 0 & \frac{-(1-d)}{6L} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{(1-d)}{6C} & 0 & \frac{-1}{RC} & 0 & \frac{-1}{RC} & 0 & \frac{-1}{RC} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{(1-d)}{6C} & 0 & \frac{-1}{RC} & 0 & \frac{-1}{RC} & 0 & \frac{-1}{RC} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{(1-d)}{6C} & 0 & \frac{-1}{RC} & 0 & \frac{-1}{RC} & 0 & \frac{-1}{RC} \end{bmatrix} \begin{bmatrix} x_0 \\ x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & 0 \\ 0 & \frac{-1}{C} \\ 0 & 0 \\ 0 & \frac{-1}{C} \\ 0 & 0 \\ 0 & \frac{-1}{C} \end{bmatrix} \begin{bmatrix} V_i \\ I_z \end{bmatrix} \quad (20)$$

$$Y = \begin{bmatrix} 0 & 0 & 1 & 0 & 1 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} [X] \quad (21)$$

Transfer function of the proposed circuit V_o/V_i (Audio Susceptibility) and V_o/i_z (Output Impedance) is calculated, considering R= 1000Ω, L= 150mH, C= 470µF and d= 0.8 is shown in equations (22) and (23). The Figure 11 depicts different damping

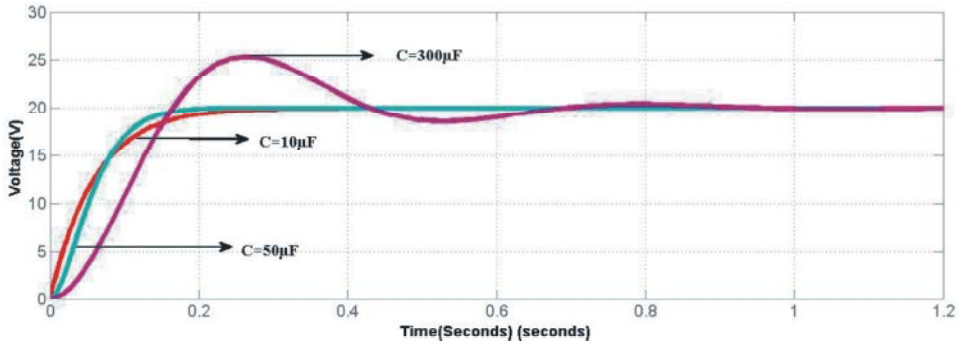

Fig. 11: Variation of Output voltage with Capacitance value

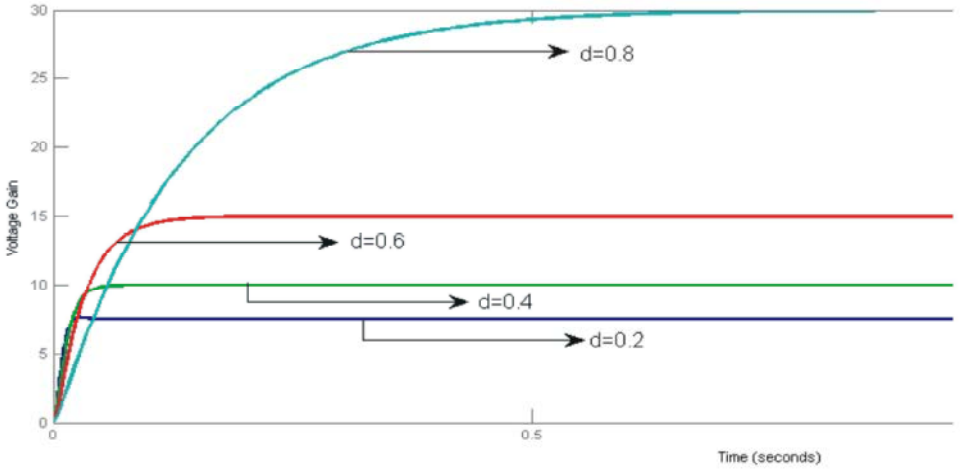

Fig. 12: Variation of Voltage Gain with duty Cycle

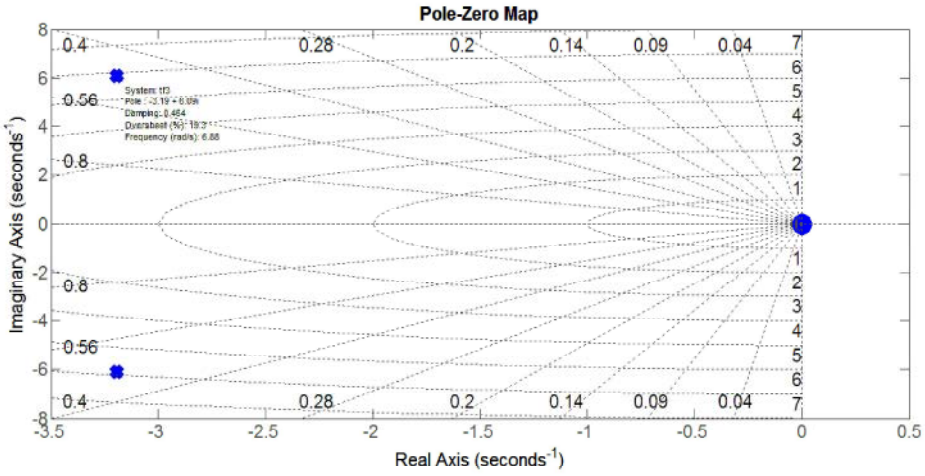

Fig. 13: Pole zero plot of the proposed circuit

conditions of the output voltage with the variations in capacitance. The capacitance of value 50µF gives critical damping.

$$\frac{V_o}{V_i} = \frac{1418\,S^2}{S^4 + 6.383S^3 + 47.28S^2} \quad (22)$$

$$\frac{V_o}{i_z} = \frac{-6383S^3 + 4.364\times10^{-12}\,S^2}{S^4 + 6.383S^3 + 47.28S^2} \quad (23)$$

The variations in the voltage gain with duty cycle obtained from the transfer function are described in Figure12. The plot is well satisfying the equation (23).

$$G = \frac{2n}{1-d} \quad (23)$$

The same equation is derived using time domain analysis which shows better performance compared to other conventional boost converters [9]. The simulated results for the circuit also gives the same results under ideal conditions.

The pole-zero plot shown in Figure 13 gives the open circuit stability of the circuit. The poles are located (-3.1915+6.0906i and -3.1915-6.0906i) in the left half of S plane gives the exponential decay of the unwanted signals and disturbance to meet the stability condition. The rate of decay depends on the location of poles away from the imaginary axis. The pole-zero plot serves a good aid to design the components and parameters of the circuit and also for the study on disturbance or decaying properties considering the stability approach.

CONCLUSION

The proposed large signal model of the DC-DC converter with Cockcroft Walton Multiplier cell is constructed through the state space approach. All the different mode of operation is separately considered for state matrix, input matrix and output matrix. The averaged state space model is framed and analyzed with the simulated model. Good agreement between the proposed model and simulation gives the validity of the approach. The proposed model gives stabile operation and verified with S domain Analysis.

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