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A Modified Topology for Three Phase Asymmetric Multilevel Inverter

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Abstract: Motive behind this work is to accomplish the stable operation of asymmetric cascaded multilevel inverter (ACMLI) and development of distributed energy resources by photovoltaic's cell. Photovoltaic energy is one of the extensively used renewable energy. To obtain maximum efficient output voltage, ACMLI for voltage progression has been proposed. Three phase 27 level ACMLI with PV sources is considered in this paper. Peak levelinverter is used by whichresolutionisimprovedandtheharmonic content is reduced to a great extent. Prime objective behind this proposal is to decrease the number of switching devices used and a low complex design when compared with a conventional multi- level inverter. This structure considerably reduces utilization of switches, driver circuit, reduced design size and cost. Validity and the efficiency of MLI are confirmed by simulation. A prototype of the ACMLI is developed to validate the theoretical and simulation results.

Key words: Asymmetric cascaded multilevel inverter · ARM Core controller · Photovoltaic Source · Ternary voltage progression

INTRODUCTION

Multilevel inverter requiresnumerous DC sources. It attracts for immense number of renewable energy as a source requirement. Since last decades, renewable energy harvesting is increasing to meet an energy demand. With the increase in demand, RES are gaining more attention, particularly solar energy produced through photovoltaic (PV) isacquiring more attention[1-5]. Compare to other renewable sources, solar is the most considerable sources because it's widely available, modular, cost free, clean and more reliable. For high voltage- great efficiency operation, MLI has attainedwidespread acceptance. With increasing the output level of inverter, more or less a nearwaveform for sinusoidal magnitude can be formed and the advantages are improved by decreasing the number of harmonic content. The different types of MLI are diode clamped, flying capacitor, cascaded MLI [6].

Cascade multilevel inverter (CMLI) is latest and widespread type of soft conversion technique that blends a anticipated output voltage from more than a few levels of DC voltages as inputs. The need of the MLI has paved way as explanation to obtain the improved high converter output voltage beyond the predefined voltage restrictions of traditional semiconductor. The traditional sinusoidal waveform is produced more conventionally with step by step order which reduces the disturbances or harmonics produced in the output. They are broadly used in workplaceswhere they use electrical motors likeBLDC motor, alternating power supply, high operation converters and drive systems, etc. Number of voltage levels compiled together gives MLI output waveform. The cascaded has disadvantage, it requiresdistinct DC input sources still circuit design is not complex and sharing of voltage doesn't arise any disturbance. Application for the givenCMLIusing RES is reviewed in [5] and [6]. Due to extensive advantages, the CML inverter bridge has been extensivelyapplied to the applications as High Voltage DC, SVC, stabilizer, high power motor drive [6-7].

Owing to this advantage, the ternary MLI is built with PV cell to alleviate the problem of increasing the demand of separate DC sources. Input to the proposed prototype is obtained from PV modules. Prominence of proposed design is attributed by its characteristics than other two types of PLI's, clamped diode's and alignment of capacitors clamped. The CMLIis anarrangement of multiple H- Bridge units. It is a low cost solution in non-high voltage applications. When proper control techniques are implemented, level of output voltage increases which yields nearly sinusoidal waveform. It gets

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more advantages as the level increases to maximum. Furthermore, ACMLI use uneven number of DC sources as it improves the modularity of the system [8-12]. Many researchers have worked hard to pave way for a conventional topology for ML converters by reducing number of active elements compared to traditionalML converters. This topology consists of series linked additionalML converter blocks. The major disadvantage associated with the circuit isdue to the use bulky capacitor. Unfortunately, when the number of bridges is increased modulation techniques fail to serve the purpose, apart from this, a large number of auxiliary bridges have to be employed and large capacitor banks need to be included [13].

An effort has been made to locate the performance of the ACMLI in the works [14].From earlier mentionsswitches operate at the peak output voltage since a complex interface transformer needs to be used for high-voltage applications. The uses of transformer increase the cost and make the structure complicated. Also, these designs are not flexible. In this proposed method, solar source is used as sources that produce increased levels of outputand serving the applicationswith the less use of power electronic components. Compare to the traditional topology it provides increased number of output levels with reduced number of elements, improved efficiency and reduction of output harmonics due to multi step sinusoidal output voltages. The majority of electric power transmissions ware three-phase and MLI is the common topology used extensively.

In this paper, a three phase geometric voltage progression with photovoltaic cell is proposed. The terrible problem of CMLI design can be outplayed using this proposed method. In addition, the power components are minimized with improved number of output levels. However, the projected method uses less number of bridgescompare to the traditional hybrid CMLI. The complexity and the harmonics of the output waveform are reduced. Section II, illustrate the photovoltaic cell system modeling. In section III, projected topology is well explained in terms ofworking principles, voltage steps and DC supply selection. Section IV and V, brings out with a brief simulation and experimental results.

PV System Modelling

Principle of Operation of Solar Cell: Demand for renewable energyis gaining consistentattention about 27-30% per annum. Energy to the photo voltaic panel is radiant energy from the sun. It is vital as maximum amount of energy produced can be obtained and utilized. In has

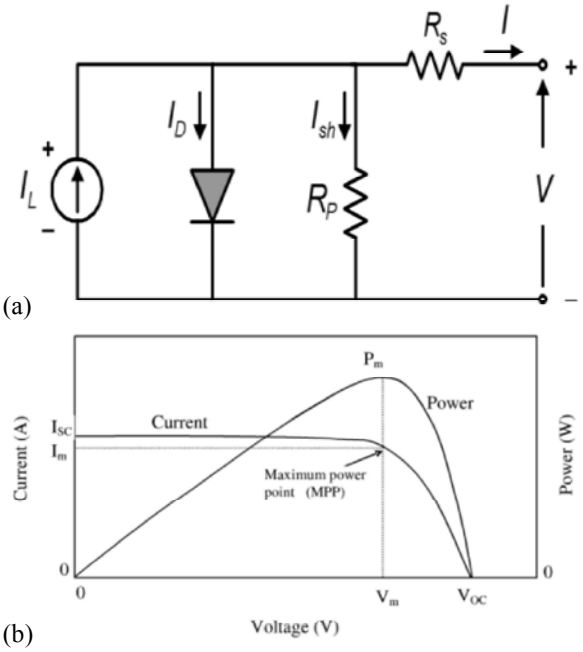


Fig. 1: a. Equivalent circuit of a solar cell; b Electrical Characteristics of PV cell

a capability to provide the energy that can sustain the requirement of the whole world. PV will have a front role in electricity generation and this RES is continually renewed.Photovoltaic arraysare compiled by many PV modules designed as a pre-wired, field- installable unit. A photo voltaic array is acomprehensive power-generating unit, consisting of many modules and panels. Arrangement of many arrays in solar cells converts solar energy into consumable quantity of direct electricity (DC). The arrangement of cells is such that series connection will improve output voltage and parallel connection will improve current. The solar cells are connected in series to form a PV module, which are then interlinked in series and parallel to form an array. The solar cells consist of semiconductor material that operates similar to PN diode. A typical PV cell produces 0.6 volts of electricity. When the solar cells are exposed to light, electron-hole pairs are generated. These are separated due to the influence of electric fields of the PN junction. Therefore current produced will be proportional to the light intensity. Fig.1(a) shows the equivalent circuit of a PV cell and Fig.1(b) shows the electrical characteristic of PV cell.

Characteristics of Solar Cell: TheI-V and P-V features of the solar cells are nonlinear. The physiognomies of the solar cell vary crucially with both cell temperature and irradiance. The physiognomies of solar cell are shown in

Fig.1(b). The basic parameters of the solar cell are open circuit voltage (Voc), short circuit current (Isc), fill factor and efficiency.

The short circuit current can be expressed as

$$(Voc = 0) = ??????? \quad (1)$$

The open circuit voltage can be expressed as

$$(Isc = 0) = ?????? \quad (2)$$

$$V_{oc} = \frac{nkT}{q}\ln\left(\frac{I_L}{I_o} + 1\right) \quad (3)$$

where,

I_L - Photo current
I_o - Overload current of the diode
q - charge of electron [1.609 x 10-19 C]
k - Boltzmann constant [1.38x10-23 J/K]
Tc - Operating temperature of the cell (K)
n - Ideality factor

Ternary Topology

Generalised H-bridge Cascaded Topology: A CMLI compilesof a series of H bridges in every phase. To obtain a three level output an H-Bridge topology needs a mono DC source with four MOSFET switches. Output voltage can have different three values $+V_{dc}$, $-V_{dc}$ and zero liable on the trigger pulses given to the switches. To deliver enormous number of output levels without increasing the inverter count, AMLI can be used. DC-voltage sources can be selected in a factor of 2 or 3 according to geometric progression. From the proposed voltage progressiontechnique, ACMLI output is obtained.Ternary progression, also called order-3 have DC voltages V_{dc1} =1V then V_{dc2} =3V …. $V_{dc\ min}$ = $V_{dcN}=3^N$ V and this progression have amplitude of DC voltages in the ratio 1: 3: 9:27.. 3^N, advantage of this topology is that the control schemes and protection requirements of every bridge are flexible. Increasing the count of levels offers more steps; hence, the output voltage has improved resolution and the better traditional sinusoidal output voltage can be achieved.

Modeling of Proposed Inverter Topology: For every full bridge inverter,the output voltage is given by

$$V_{0i} = V_{dc}\,(k_{1i}\text{-}k_{3i}) \quad (4)$$

Input DC current is

$$I_{dci} = I_a(k_{1i}\text{-}k_{3i}) \quad (5)$$

I =1, 2, 3… (Shows the count of full bridge inverters employed). $I_a$is the output current of the new hybrid inverter. k_{1i} and k_{3i} are the switches in the upper half of each full bridge inverter. Now the output voltage of every phase of the multilevel hybrid inverter is given by

$$V_{on} = \sum_{i=1}^{n} V_{oi} \quad (6)$$

Proposed Topology: The PV array is linked to the Cascaded H-Bridge as input sources. The arrangementfamiliarized in this work is an ACMLI that uses different DC Sources. The general function of this MLI is the same as that of the other two inverters. ACMLI provides improved output voltage levels without changing the number of full bridge units. As depicted in Fig. 2. Asymmetric cascaded H-bridge inverter circuit is proposed in the work.

In the suggested model, ternary DC voltage progressions of unequal DC sources of ACMLI are used. This is themaximumprevalent unequal voltage progression with an amplitude of DC voltage having a ratio of 1:3:9:27:81....3N and the maximum output voltage reaches $((3^N\text{-}1)/2)\ V_{dc}$. The Asymmetric Cascaded H- Bridge consists of 3-bridges, to generate 27 level output for the DC Sources of 9:3:1 ratio. The output waveform has 27 levels as ±13Vdc ……±1Vdc and zero. By different combinations of the 12 switches, S1-S12, each inverter level can generate three different voltage outputs, $+V_{dc}$, $-V_{dc}$ and zero. Let the output of H bridge-1 be denoted as $V_1(t)$,that of the H bridge-2 as $V_2(t)$ and that of the H bridge-3 as $V_3(t)$.Hence the output voltage is given by

$$V(t) = V_1(t) + V_2(t) + V_3(t) \quad (7)$$

As per the patterns given in the switching Table 2, driving pulses for the H-bridges are developed. The produced gate pulses are set to every switch in accord with the established pattern as shown in Table I. Similarly the negative half will be generated to obtained 27 level output voltage. For N such cascade inverters, one can achieve the following distinct voltage levels

$$n = 3^N, \text{ if } V_{dc,j} = 3^{j-1}V_{dc},\ j = 1, 2, \ldots, N \quad (8)$$

The maximum output voltage of this N cascaded multilevel inverter is

$$V_{o,MAX} = \sum_{j=1}^{N} V_{dc,j} \quad (9)$$

$$V_{o,MAX} = \left(\frac{3^N - 1}{2}\right)V_{dc} \quad (10)$$

if $Vdc,j = 3^{j-1} Vdc$, $_j = 1, 2, \ldots, N$.

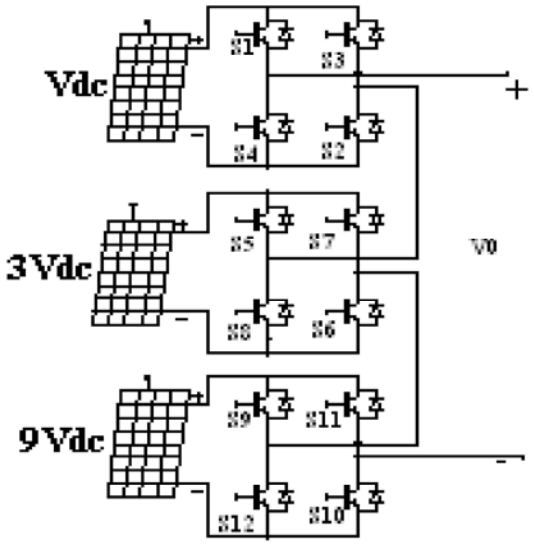


Fig. 2: Ternary Asymmetric Cascaded multilevel inverter

Table I: Performance parameters of ternary topology

Parameters	Asymmetric Inverter (Ternary)	Required components
Number of level	3^N	27
Number of Switches	4N	12
Number of DC source	N	3
$V_{0,Max[pu]}$	$(3^N-1)/2$	13

Table II: Switching state for one h-bridge cell

State	Switches States $S_1 S_2 S_3 S_4$	V_0
1	On On Off Off	$+V_{dc}$
2	Off Off On On	$-V_{dc}$
3	Off On Off On	0

Table I summarizes the number of levels, switches, DC sources and maximum output voltage for asymmetrical cascaded multilevel inverter.

Objective of this proposed work is to apply three phase MLI with the renewable energy resources for a high power application.

Simulation Results: The following result shows the quality of waveform obtained by the ternary MLI. To see the performance of the proposed system; simulations are performed by MATLAB SIMULINK. SIMULINK is used to simulate the driving pulse to the model. The driving pulses are generated as shown in Table III with separate subsystem. The inputs sources are given by means of PV cell, which are connected in series to get the required voltage to the three H-bridges. Fig. 4. Illustrates the driving signal for four switches in first leg. An output voltage for H bridge is shown in Fig 5. The structure of the three phase model as shown in Fig 6 is obtained by

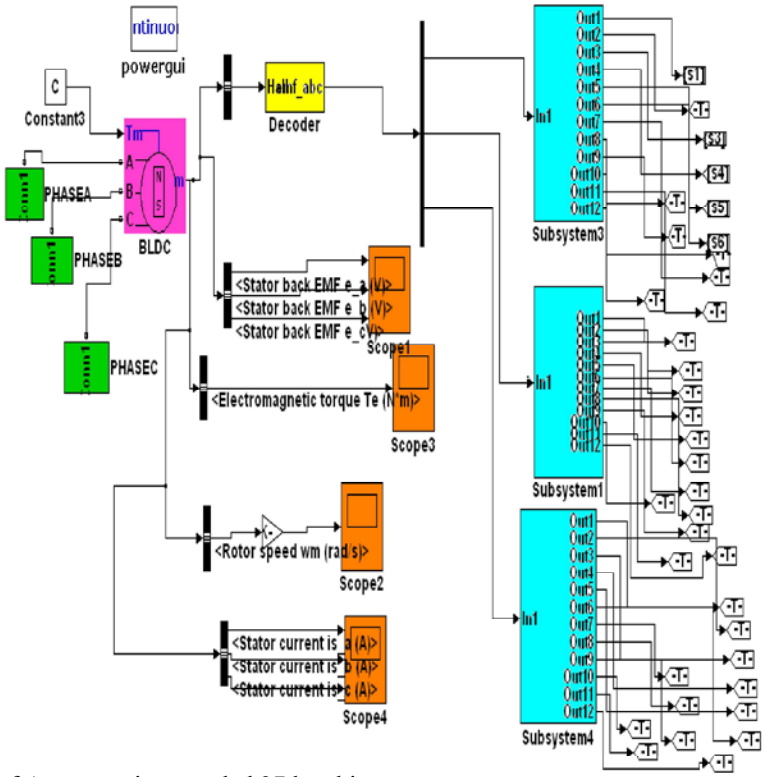


Fig. 3: Simulink model of Asymmetric cascaded 27 level inverter

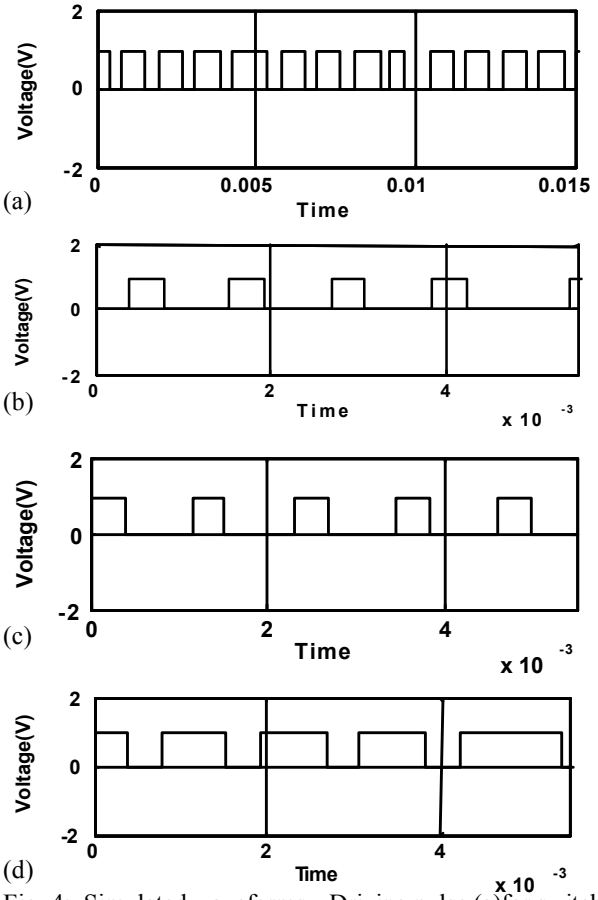


Fig. 4: Simulated waveforms – Driving pulse (a)for switch S_1 (b)for switch S_2 (c)For switch S_3 (d)for switch S_4.

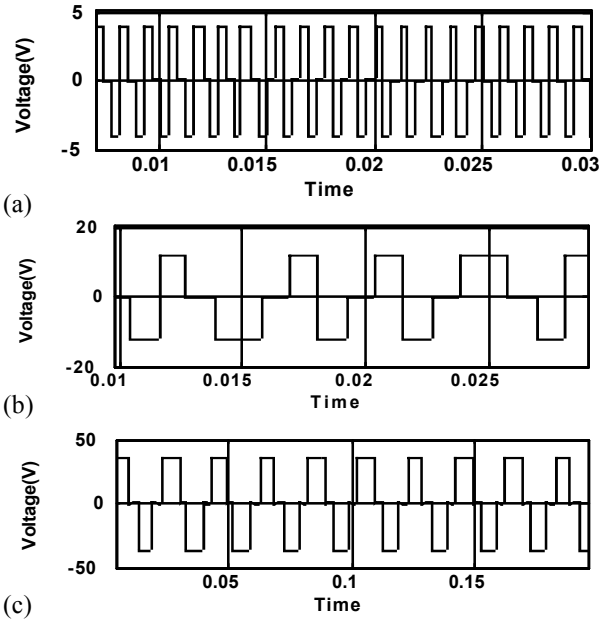


Fig. 5: Simulated output waveforms (a)for first H-bridge (b) for second H-bridge (c) for third H-bridge

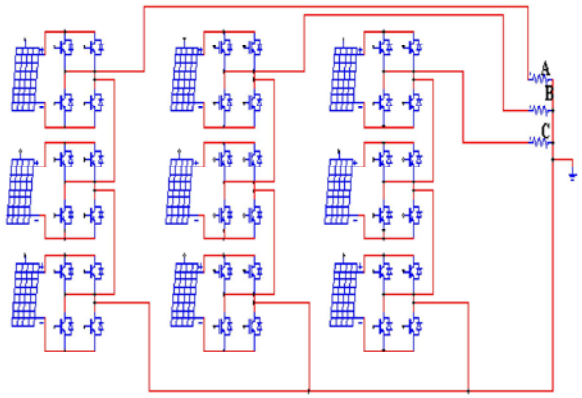


Fig. 6: Simulink structure of Three phase asymmetric MLI

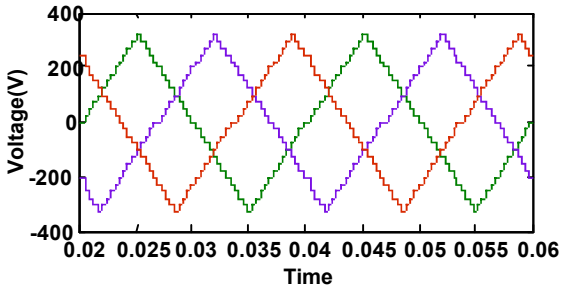


Fig. 7: Three phase output waveform of asymmetric MLI

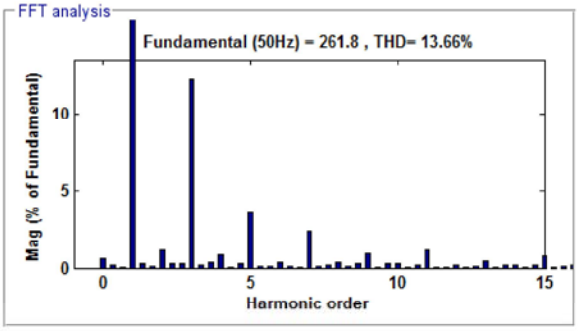


Fig. 8: Harmonic spectrum of three phase asymmetric MLI

generating the driving pulse to the switches for phase B and Phase C, as same process and operation with a phase shift of 120 and 240 respectively and three phase output waveform is shown in Fig 7.

Experimental Results: To test the overall performance of the system, experimental prototype is assembled as shown in Fig. 10. The power supply circuit comprises of a step down transformer and a voltage regulator IC 7805 and 7812, which provides the DC voltage to the controller and the driver circuit. ARM microcontroller is used to provide the driving pulses because of its superior features like

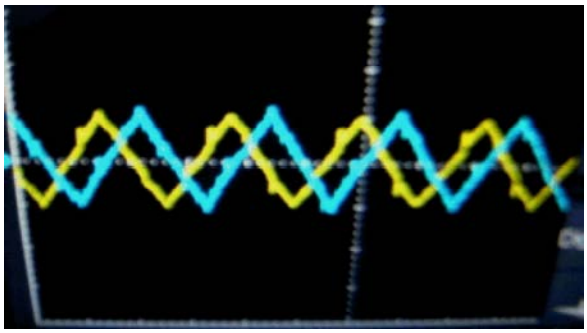
Table III: Mode of operation of the three-phase ternary multilevel inverter during positive cycle

Level	Output voltage	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
1	Vdc	ON	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	ON
2	2Vdc	OFF	OFF	ON	ON	ON	ON	OFF	OFF	OFF	ON	OFF	ON
3	3Vdc	OFF	ON	OFF	ON	ON	ON	OFF	OFF	OFF	ON	OFF	ON
4	4Vdc	ON	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	ON
5	5Vdc	OFF	OFF	ON	ON	OFF	0FF	ON	ON	ON	ON	OFF	OFF
6	6Vdc	OFF	ON	OFF	ON	OFF	OFF	ON	ON	ON	ON	OFF	OFF
7	7Vdc	ON	ON	OFF	OFF	OFF	OFF	ON	ON	ON	ON	OFF	OFF
8	8Vdc	OFF	OFF	ON	ON	OFF	ON	OFF	ON	ON	ON	OFF	OFF
9	9Vdc	OFF	ON	OFF	ON	OFF	ON	OFF	ON	ON	ON	OFF	OFF
10	10Vdc	ON	ON	OFF	OFF	OFF	ON	OFF	ON	ON	ON	OFF	OFF
11	11Vdc	OFF	OFF	ON	ON	ON	ON	OFF	OFF	ON	ON	OFF	OFF
12	12Vdc	OFF	ON	OFF	ON	ON	ON	OFF	OFF	ON	ON	OFF	OFF
13	13Vdc	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF

- Meeting the computing needs of the task on hand efficiently and cost effectively.
- The NuMicro™ NUC100 Series is 32-bit microcontrollers with embedded core the cost is equivalent to traditional 8-bit microcontroller
- Wide availability and reliable sources

The control circuit decides the sequence of pulses to be given to the switches in the power circuit. The driver circuit amplifies the pulses to the required level. The drivercircuitisusedfor an isolationof the negativecurrentto themicro-controller,amplificationof voltageandtocreate a constantvoltage source.Thesquare pulseshould have aconstantvoltageof5V. Isolationrefersto the separationofthepowercircuitfrom the control circuit. Outputvoltage from the microcontroller isgivento thedriverIC; and theoutputvoltage will have an increased magnitudethat willbesufficientfordrivingthe MOSFET. Vss and the common ground should be grounded separately else isolation will not work. A power circuit is fabricated using 12 IRF540 (MOSFETs) anditrequires three individual DC sources of an asymmetric geometric ratio. As per the switching sequence presented in Table 3, the pulse signals applied to the MOSFET switches are generated, using themicro-controller.

MOSFET with anti-parallel diodes are employed as switching devices. Each inverter leg takes different voltages**.** During the implementation, the inverter input sources are taken as V_{dc1} = 4 V, V_{dc2} = 12V and V_{dc3} = 36V with switching frequency f = 50 Hz. The prototype of the proposed inverter that includes the following; three DC supplies, three H-Bridge power circuits and embedded controller as shown in Fig 10. To reach 27 level, 3 unequal DC sources along with 12 switches are used for single phase. Figure 11 and Figure 12 depicts the experimental waveform for the inverter to generate driving pulses for



Scale:X-axis 1CM=5mSec, Y-axis 1CM=20 Volts

Fig. 9: Phase voltages of three phase asymmetric MLI

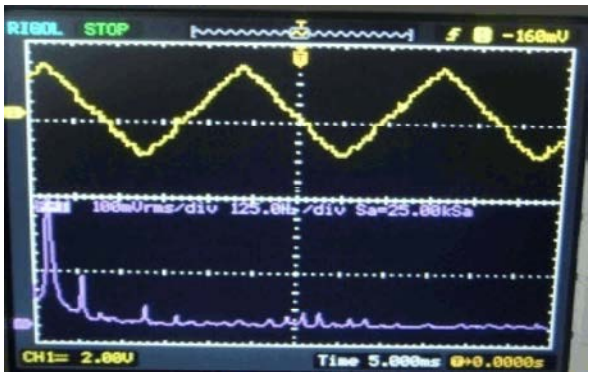


Fig. 10: Harmonic spectrum of ACMLI

Fig. 10: Experimental set up of three phase ACMLI

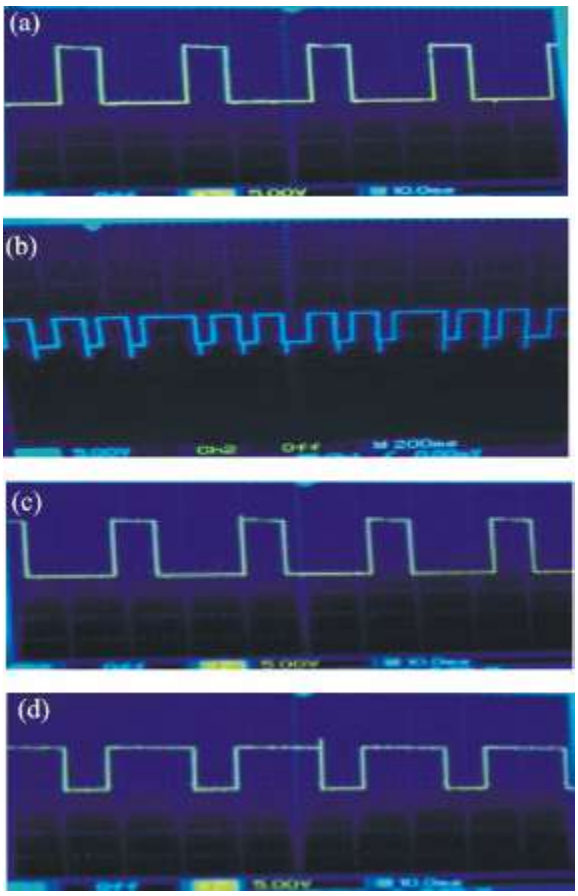


Fig. 11: Experimental waveforms - Driving pulse (a)For switch S_1(b)For switch S2(c)For switch S_3(d)For switch S_4

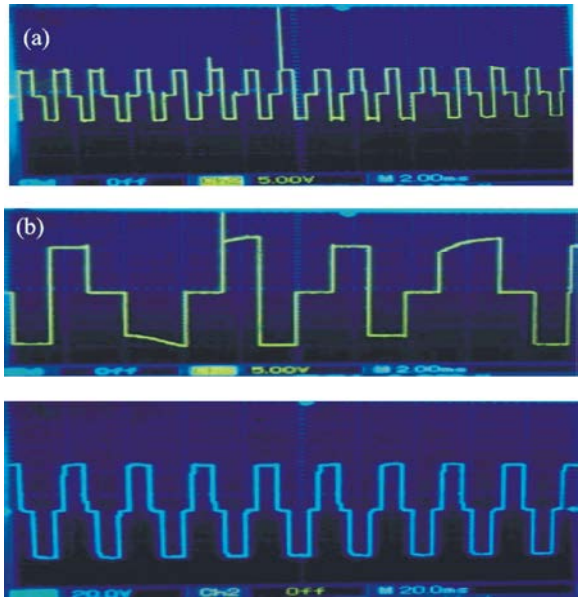


Fig. 12: Experimental output voltage waveforms (a) first H-bridge (b) second H-bridge (c) third H-bridge

the switches and the output voltage waveform of three bridges respectively.The output voltages with twenty seven-level stepped waveform can be clearly appreciated; with low distortion. THD of the output voltage can be calculated from

$$THD = \frac{\sqrt{\sum_{n=3,5,7}^{\infty} V_n^2}}{V_1}$$

where V_1 and n are the fundamental component and harmonic order, respectively. Switching losses are minimized and hence the efficiency is increased up to 88%.Figs. 10. Clearly show the substantial increment in theinverter output voltage levels with a reduction in power electronics components and DC supplies. Fig. 9illustrates the voltage waveforms of phase A and Phase B respectively.

Variation of the three phase voltage with phase difference is shown provides a phase shift of voltages. In this regard, the inverter has been adjusted to produce a 50 Hz, 27-level staircase waveform. In this case 36 switches are used. The hardware result obtained using arm processor is found to be in agreement with the simulation results.

CONCLUSION

Photovoltaic fed asymmetric cascaded Multilevel Inverter topology with ternary voltage progression with an unequal source has been implemented. The suggested configuration is formed by cascading three H-bridges with unequal DC sources in the ratio of 1:3. A three phase 27-level asymmetric cascaded multilevel inverter is implemented to demonstrate some of its advantages: excellent voltage waveforms reduced THD and improved efficiency. By proper selection of driver IC's, the design complexity occurs in multilevel inverter is eliminated. It uses lesser number of switches and DC sources, thus by decreasing the complexity, installation area and the cost of the circuit. Moreover, this approach enables to obtain a twenty seven-level conversion with only three DC bus. It increases the efficiency of the inverter by 89%. In order to verify the performance of the proposed multilevel inverter, Geometric progression (ternary voltage ratio) configuration is simulated and the same is tested experimentally by using ARM controller. Thus it is concluded three phase 27 level is optimum. Further increase in levels will cause the increase in losses and the circuit design has complexity.

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