A Modified Topology for Three Phase Asymmetric Multilevel Inverter

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Abstract: Motive behind this work is to accomplish the stable operation of asymmetric cascaded multilevel inverter (ACMLI) and development of distributed energy resources by photovoltaic’s cell. Photovoltaic energy is one of the extensively used renewable energy. To obtain maximum efficient output voltage, ACMLI for voltage progression has been proposed. Three phase 27 level ACMLI with PV sources is considered in this paper. Peak level inverter is used by which resolution is improved and the harmonic content is reduced to a great extent. Prime objective behind this proposal is to decrease the number of switching devices used and a low complex design when compared with a conventional multi-level inverter. This structure considerably reduces utilization of switches, driver circuit, reduced design size and cost. Validity and the efficiency of MLI are confirmed by simulation. A prototype of the ACMLI is developed to validate the theoretical and simulation results.

Key words: Asymmetric cascaded multilevel inverter • ARM Core controller • Photovoltaic Source • Ternary voltage progression

INTRODUCTION

Multilevel inverter requires numerous DC sources. It attracts for immense number of renewable energy as a source requirement. Since last decades, renewable energy harvesting is increasing to meet an energy demand. With the increase in demand, RES are gaining more attention, particularly solar energy produced through photovoltaic (PV) is acquiring more attention[1-5]. Compare to other renewable sources, solar is the most considerable sources because it’s widely available, modular, cost free, clean and more reliable. For high voltage- great efficiency operation, MLI has attained widespread acceptance. With increasing the output level of inverter, more or less a DC waveform is produced more conventionally with step by step order which reduces the disturbances or harmonics produced in the output. They are broadly used in workplaces where they use electrical motors like BLDC motor, alternating power supply, high operation converters and drive systems, etc. Number of voltage levels compiled together gives MLI output waveform. The cascaded has disadvantage, it requires distinct DC input sources still circuit design is not complex and sharing of voltage doesn’t arise any disturbance. Application for the given CMLI using RES is reviewed in [5] and [6]. Due to extensive advantages, the CML inverter bridge has been extensively applied to the applications as High Voltage DC, SVC, stabilizer, high power motor drive [6-7].

Owing to this advantage, the ternary MLI is built with PV cell to alleviate the problem of increasing the demand of separate DC sources. Input to the proposed prototype is obtained from PV modules. Prominence of proposed design is attributed by its characteristics than other two types of PLI’s, clamped diode’s and alignment of capacitors clamped. The CMLI’s arrangement of multiple H-Bridge units. It is a low cost solution in non-high voltage applications. When proper control techniques are implemented, level of output voltage increases which yields nearly sinusoidal waveform. It gets
more advantages as the level increases to maximum. Furthermore, ACMLI use uneven number of DC sources as it improves the modularity of the system [8-12]. Many researchers have worked hard to pave way for a conventional topology for ML converters by reducing number of active elements compared to traditional ML converters. This topology consists of series linked additional ML converter blocks. The major disadvantage associated with the circuit is due to the use bulky capacitor. Unfortunately, when the number of bridges is increased modulation techniques fail to serve the purpose, apart from this, a large number of auxiliary bridges have to be employed and large capacitor banks need to be included [13].

An effort has been made to locate the performance of the ACMLI in the works [14]. From earlier mentions switches operate at the peak output voltage since a complex interface transformer needs to be used for high-voltage applications. The uses of transformer increase the cost and make the structure complicated. Also, these designs are not flexible. In this proposed method, solar source is used as sources that produce increased levels of output and serving the applications with the less use of power electronic components. Compare to the traditional topology it provides increased number of output levels with reduced number of elements, improved efficiency and reduction of output harmonics due to multi step sinusoidal output voltages. The majority of electric power transmissions were three-phase and MLI is the common topology used extensively.

In this paper, a three phase geometric voltage progression with photovoltaic cell is proposed. The terrible problem of CMLI design can be outplayed using this proposed method. In addition, the power components are minimized with improved number of output levels. However, the projected method uses less number of bridges compare to the traditional hybrid CMLI. The complexity and the harmonics of the output waveform are reduced. Section II, illustrate the photovoltaic cell system modeling. In section III, projected topology is well explained in terms of working principles, voltage steps and DC supply selection. Section IV and V, brings out with a brief simulation and experimental results.

**PV System Modelling**

**Principle of Operation of Solar Cell:** Demand for renewable energy is gaining consistent attention about 27-30% per annum. Energy to the photo voltaic panel is radiant energy from the sun. It is vital as maximum amount of energy produced can be obtained and utilized. In has a capability to provide the energy that can sustain the requirement of the whole world. PV will have a front role in electricity generation and this RES is continually renewed. Photovoltaic arrays are compiled by many PV modules designed as a pre-wired, field-installable unit. A photo voltaic array is a comprehensive power-generating unit, consisting of many modules and panels. Arrangement of many arrays in solar cells converts solar energy into consumable quantity of direct electricity (DC). The arrangement of cells is such that series connection will improve output voltage and parallel connection will improve current. The solar cells are connected in series to form a PV module, which are then interlinked in series and parallel to form an array. The solar cells consist of semiconductor material that operates similar to PN diode. A typical PV cell produces 0.6 volts of electricity. When the solar cells are exposed to light, electron-hole pairs are generated. These are separated due to the influence of electric fields of the PN junction. Therefore current produced will be proportional to the light intensity. Fig.1(a) shows the equivalent circuit of a PV cell and Fig.1(b) shows the electrical characteristic of PV cell.

**Characteristics of Solar Cell:** The I-V and P-V features of the solar cells are nonlinear. The physiognomies of the solar cell vary crucially with both cell temperature and irradiance. The physiognomies of solar cell are shown in...
Fig. 1(b). The basic parameters of the solar cell are open circuit voltage ($V_{oc}$), short circuit current ($I_{sc}$), fill factor employed. The short circuit current can be expressed as

$$(V_{oc} = 0) = ??????$$

The open circuit voltage can be expressed as

$$(I_{sc} = 0) = ??????$$

$V_{oc} = \frac{nqITc}{k} \ln\left(\frac{I}{I_{a}} + 1\right)$$

where,

$I_a$ - Photo current
$I_r$ - Overload current of the diode
$q$ - charge of electron [1.609 x 10-19 C]
$k$ - Boltzmann constant [1.38x10-23 J/K]
$Tc$ - Operating temperature of the cell (K)

Ternary Topology
Generalised H-bridge Cascaded Topology: A CMLI compiles a series of H bridges in every phase. To obtain a three level output an H-Bridge topology needs a mono DC source with four MOSFET switches. Output voltage can have different three values $V_{dc}$ and zero liable on combinations of the 12 switches, S1-S12, each inverter can generate three different voltage outputs, $+V$, $-V$, and zero. Let the output of H bridge-1 be denoted as $V_1(t)$, that of the H bridge-2 as $V_2(t)$, and that of the H bridge-3 as $V_3(t)$. Hence the output voltage is given by

$$V(t) = V_1(t) + V_2(t) + V_3(t)$$

Proposed Topology: The PV array is linked to the Cascaded H-Bridge as input sources. The arrangement familiarized in this work is an ACMLI that uses different DC Sources. The general function of this MLI is the same as that of the other two inverters. ACMLI provides improved output voltage levels without changing the number of full bridge units. As depicted in Fig. 2. Asymmetric cascaded H-bridge inverter circuit is proposed in the work.

In the suggested model, ternary DC voltage progressions of unequal DC sources of ACMLI are used. This is the maximum unequal voltage progression with an amplitude of DC voltage having a ratio of 1:3:9:27:81...3N and the maximum output voltage reaches $(3^n-1)/2$ $V_{dc}$. The Asymmetric Cascaded H-Bridge consists of 3-bridges, to generate 27 level output for the DC Sources of 9:3:1 ratio. The output waveform has 27 levels as ±13Vdc and ±1Vdc and zero. By different combinations of the 12 switches, S1-S12, each inverter level can generate three different voltage outputs, $+V_{dc}$, $-V_{dc}$ and zero. Let the output of H bridge-1 be denoted as $V_{1}(t)$, that of the H bridge-2 as $V(t)$, and that of the H bridge-3 as $V_{3}(t)$. Hence the output voltage is given by

$$V(t) = V_{1}(t) + V_{2}(t) + V_{3}(t)$$

As per the patterns given in the switching Table 2, driving pulses for the H-bridges are developed. The produced gate pulses are set to every switch in accord with the established pattern as shown in Table I. Similarly the negative half will be generated to obtained 27 level output voltage. For $N$ such cascade inverters, one can achieve the following distinct voltage levels

$$n = 3^n, \text{if } V_{dc} = 3^{(n-1)}V_{dc}, j = 1, 2, . . . , N$$

The maximum output voltage of this $N$ cascaded multilevel inverter is

$$V_{0,MAX} = \sum_{j=1}^{N} V_{dc,j}$$

$$V_{0,MAX} = \left(\frac{3^n - 1}{2}\right)V_{dc}$$
if $V_{dc,j} = 3^j V_{dc}, j = 1, 2, \ldots, N$.

Table I: Performance parameters of ternary topology

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Asymmetric Inverter (Ternary)</th>
<th>Required components</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of level</td>
<td>$3^N$</td>
<td>27</td>
</tr>
<tr>
<td>Number of Switches</td>
<td>$4N$</td>
<td>12</td>
</tr>
<tr>
<td>Number of DC source</td>
<td>$N$</td>
<td>3</td>
</tr>
<tr>
<td>$V_{(Max)}$</td>
<td>$(3^N - 1)/2$</td>
<td>13</td>
</tr>
</tbody>
</table>

Table II: Switching state for one h-bridge cell

<table>
<thead>
<tr>
<th>State</th>
<th>Switches States</th>
<th>$V_o$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>On On Off Off</td>
<td>$+V_o$</td>
</tr>
<tr>
<td>2</td>
<td>Off Off On On</td>
<td>$-V_o$</td>
</tr>
<tr>
<td>3</td>
<td>Off On Off On</td>
<td>0</td>
</tr>
</tbody>
</table>

Table I summarizes the number of levels, switches, DC sources and maximum output voltage for asymmetrical cascaded multilevel inverter.

Objective of this proposed work is to apply three phase MLI with the renewable energy resources for a high power application.

Simulation Results: The following result shows the quality of waveform obtained by the ternary MLI. To see the performance of the proposed system; simulations are performed by MATLAB SIMULINK. SIMULINK is used to simulate the driving pulse to the model. The driving pulses are generated as shown in Table III with separate subsystem. The inputs sources are given by means of PV cell, which are connected in series to get the required voltage to the three H-bridges. Fig. 4. Illustrates the driving signal for four switches in first leg. An output voltage for H bridge is shown in Fig 5. The structure of the three phase model as shown in Fig 6 is obtained by
Fig. 4: Simulated waveforms – Driving pulse (a) for switch S, (b) for switch S, (c) for switch S, (d) for switch S

Fig. 5: Simulated output waveforms (a) for first H-bridge, (b) for second H-bridge, (c) for third H-bridge

Fig. 6: Simulink structure of Three phase asymmetric MLI

Fig. 7: Three phase output waveform of asymmetric MLI

Fig. 8: Harmonic spectrum of three phase asymmetric MLI

generating the driving pulse to the switches for phase B and Phase C, as same process and operation with a phase shift of 120 and 240 respectively and three phase output waveform is shown in Fig 7.

**Experimental Results:** To test the overall performance of the system, experimental prototype is assembled as shown in Fig. 10. The power supply circuit comprises of a step down transformer and a voltage regulator IC 7805 and 7812, which provides the DC voltage to the controller and the driver circuit. ARM microcontroller is used to provide the driving pulses because of its superior features like
Table III: Mode of operation of the three-phase ternary multilevel inverter during positive cycle

<table>
<thead>
<tr>
<th>Level</th>
<th>Output voltage</th>
<th>S1</th>
<th>S2</th>
<th>S3</th>
<th>S4</th>
<th>S5</th>
<th>S6</th>
<th>S7</th>
<th>S8</th>
<th>S9</th>
<th>S10</th>
<th>S11</th>
<th>S12</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1 Vdc</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>2</td>
<td>2 Vdc</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>3</td>
<td>3 Vdc</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>4</td>
<td>4 Vdc</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
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<tr>
<td>5</td>
<td>5 Vdc</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
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</tr>
<tr>
<td>6</td>
<td>6 Vdc</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
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<td>ON</td>
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<tr>
<td>7</td>
<td>7 Vdc</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
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<td>ON</td>
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<td>ON</td>
</tr>
<tr>
<td>8</td>
<td>8 Vdc</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
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<tr>
<td>9</td>
<td>9 Vdc</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
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<td>ON</td>
<td>ON</td>
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<td>ON</td>
</tr>
<tr>
<td>10</td>
<td>10 Vdc</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
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</tr>
<tr>
<td>11</td>
<td>11 Vdc</td>
<td>OFF</td>
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<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
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<tr>
<td>12</td>
<td>12 Vdc</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
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<tr>
<td>13</td>
<td>13 Vdc</td>
<td>ON</td>
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- Meeting the computing needs of the task on hand efficiently and cost effectively.
- The NuMicro™ NUC100 Series is 32-bit microcontrollers with embedded core the cost is equivalent to traditional 8-bit microcontroller
- Wide availability and reliable sources

The control circuit decides the sequence of pulses to be given to the switches in the power circuit. The driver circuit amplifies the pulses to the required level. The driver circuit is used for an isolation of the negative current from the microcontroller, amplification of voltage and to create a constant voltage source. The square pulses should have a constant voltage of 5V. Isolation refers to the separation of the power circuit from the control circuit. Output voltage from the microcontroller is given to the driver IC; and the output voltage will have an increased magnitude that will be sufficient for driving the MOSFET. Vss and the common ground should be grounded separately else isolation will not work. A power circuit is fabricated using 12 IRF540 (MOSFETs) and it requires three individual DC sources of an asymmetric geometric ratio. As per the switching sequence presented in Table 3, the pulse signals applied to the MOSFET switches are generated, using the microcontroller.

MOSFET with anti-parallel diodes are employed as switching devices. Each inverter leg takes different voltages. During the implementation, the inverter input sources are taken as \( V_{dc1} = 4 \text{ V} \), \( V_{dc2} = 12 \text{ V} \) and \( V_{dc3} = 36 \text{ V} \) with switching frequency \( f = 50 \text{ Hz} \). The prototype of the proposed inverter that includes the following; three DC supplies, three H-Bridge power circuits and embedded controller as shown in Fig 10. To reach 27 level, 3 unequal DC sources along with 12 switches are used for single phase. Figure 11 and Figure 12 depicts the experimental waveform for the inverter to generate driving pulses for
the switches and the output voltage waveform of three bridges respectively. The output voltages with twenty seven-level stepped waveform can be clearly appreciated; with low distortion. THD of the output voltage can be calculated from

$$\text{THD} = \frac{\sqrt{\sum_{n=1}^{n \infty} V_n^2}}{V_1}$$

where $V_1$ and $n$ are the fundamental component and harmonic order, respectively. Switching losses are minimized and hence the efficiency is increased up to 88%. Figs. 10. Clearly show the substantial increment in the inverter output voltage levels with a reduction in power electronics components and DC supplies. Fig. 9 illustrates the voltage waveforms of phase A and Phase B respectively.

Variation of the three phase voltage with phase difference is shown provides a phase shift of voltages. In this regard, the inverter has been adjusted to produce a 50 Hz, 27-level staircase waveform. In this case 36 switches are used. The hardware result obtained using arm processor is found to be in agreement with the simulation results.

**CONCLUSION**

Photovoltaic fed asymmetric cascaded Multilevel Inverter topology with ternary voltage progression with an unequal source has been implemented. The suggested configuration is formed by cascading three H-bridges with unequal DC sources in the ratio of 1:3. A three phase 27-level asymmetric cascaded multilevel inverter is implemented to demonstrate some of its advantages: excellent voltage waveforms reduced THD and improved efficiency. By proper selection of driver IC’s, the design complexity occurs in multilevel inverter is eliminated. It uses lesser number of switches and DC sources, thus by decreasing the complexity, installation area and the cost of the circuit. Moreover, this approach enables to obtain a twenty seven-level conversion with only three DC bus. It increases the efficiency of the inverter by 89%. In order to verify the performance of the proposed multilevel inverter, Geometric progression (ternary voltage ratio) configuration is simulated and the same is tested experimentally by using ARM controller. Thus it is concluded three phase 27 level is optimum. Further increase in levels will cause the increase in losses and the circuit design has complexity.
REFERENCES