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A New High Speed Full Adder Cell

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Abstract: This paper presents a low power 1-bit Full Adder with an improved performance. The proposed design overcomes the drawbacks of the Hybrid-CMOS Logic style and uses CMOS transmission gate and pass transistor based XOR-XNOR circuits to generate SUM and CARRY. The proposed full adder is compared with existing Hybrid CMOS 1-bit full adders. Based on the simulation results overall improvements of 60.77%, 0.25% and 60.84% are observed in delay, power consumption and power delay product respectively.

Key words: Power Delay Product · Full Adder · Power Consumption · Propagation Delay · CMOS Logic · Transmission Gate · Pass Transistor

INTRODUCTION

Most of the digital systems such as digital signal processors, image and video processors and microprocessors, extensively use arithmetic operations. These operations *i.e.* addition, subtraction, multiplication and multiply and accumulate use the 1-bit full adder cell as their basic building block. Enhancing the performance of 1-bit full adder cell is therefore critical for enhancing the overall module performance.

The LEAP adder [13] (Lean Integration with Pass transistors) that uses the top down pass transistor logic design uses the NMOS pass transistor. It has the power and delay statistics better that the CMOS based adder. In this integration scheme pass transistor based cell library and synthesis tools are created. This cell has the flexibility of transistor level circuit design and compatibility with conventional cell based design. The cell library has seven cells. At $V_{cc} > 2.7V_{th}$ NMOS pass transistor based cell library has better statistics than CMOS based cell library and hence the LEAP adder performs better.

The complementary CMOS full adder [12] (C-CMOS) comprises of 28 transistors. It is based on the regular CMOS structure with PMOS pull-up and NMOS pull-down transistors. The series transistors in the output stage form a weak driver. Additional buffers are required for necessary drive capability of the cascaded cells. This design offers the advantages of complementary CMOS style. Complementary CMOS circuits are robust against voltage scaling and transistor sizing. Robustness is essential to provide reliable operation at low voltage and for designing with arbitrary transistor sizes. The layout of the full adder circuit is straightforward and area efficient due to complementary transistor pairs and lesser interconnections. The circuit is slower than its predecessor but its power consumption is lower due to the pull-up and pull-down transistors. The primary reason for speed degradation is the larger input capacitance of C-CMOS full adder. The input capacitance is more as each input is connected to a PMOS as well as NMOS. The presence of PMOS block also increases delay due to the lesser mobility of the charge carriers.

The transmission gate adder (TGA) [14] is a special pass transistor logic circuit comprising of 20 MOS transistors. It is formed by connecting a PMOS transistor and an NMOS transistor in parallel that are controlled by complementary signals. The PMOS and the NMOS transistors provide the path to the input logic '1' and '0' respectively when they are turned ON simultaneously by the control signal. The primary disadvantage of transmission gate logic is that it requires double the number of transistors than the pass transistor logic. Another shortcoming of this design is the spurious transitions in the output signal.

The disadvantage of transmission gate logic is removed by the complementary pass transistor logic (CPL) full adder with swing restoration [13]. It provides high speed and good driving capability due to output inverters and the cross coupled PMOS transistors.

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Another advantage of this circuit is that one pass transistor network comprising of either NMOS transistors or PMOS transistors is sufficient to implement the logic function. This results in lesser number of transistors and lesser input load. However this circuit suffers from the inherent threshold voltage drop problem. The layout of a CPL cell is complicated due to its irregular transistor arrangement.

The 16 transistor adder [12] is based on the new four transistor XOR and XNOR circuits. This adder has several advantages *i.e.* it removes the inverter from the critical path of the cell that decreases the cell delay. It also balances the delays of generating H = A XOR B and H' = A XNOR B that leads to fewer glitches at the output. It decreases the capacitance at H since it is no longer loading an inverter. It is noticed that this circuit does not use any inverter or any standard CMOS style and this eliminates the short circuit component within the cell. The incomplete voltage swing at H and H' for some input combinations *i.e.* A = B = 0 and A = B = 1 reduces the power consumed in during transitions.

The transmission function full adder (TFA) [10-11] comprises of 16 MOS transistors and is based on the transmission function theory. The circuits based on this theory use pass transistors and transmission gates. The power consumption in these circuits is generally low. The main problem with these circuits is the threshold voltage drop problem due to which higher V_{cc} has to be used. The output is a weak logic '1' when an input of logic '1' is passed through an NMOS. Likewise, the output is a weak logic '0' when an input of logic '0' is passed through a PMOS. Output inverters are used to ensure drivability. Cells are used to generate XOR and XNOR function H and H' that control transmission gates to produce sum and C_{out} outputs. The inverter introduces unwanted delay between H and H' leading to 0-0 and 1-1 overlap. This causes glitches in the output signal and these spurious transitions increase power consumption.

The 10T full adder [9] use newly proposed XOR and XNOR gates. In this XOR gate there is no power supply *i.e.* it is powerless XOR, likewise the XNOR gate is groundless because there is no direct connection to ground. These features help this adder reduce power consumption. Low drive capability is its main disadvantage.

14T full adder [8] uses the non full swing pass transistors with swing restored transmission gate technique to reduce its transistor count. The low drive capability of this circuit is its main disadvantage and a buffer is required while making adder chains.

In the hybrid adder circuit [8] the switching speed is increased by eliminating the inverter from the critical path. The two complementary feedback transistors restore the weak logic caused by pass transistors. The circuit has inherited the advantages of complementary logic style. Its robustness against transistor sizing, due to high noise margin enables it to operate reliably at low power consumption.

Hybrid-CMOS logic style [6] design uses the features of different logic styles to improve upon the performance of the earlier logic styles. The pass transistor logic with cross coupled PMOS transistors produces XOR and XNOR gates. Transmission function implementation of XNOR function is used to generate sum and a hybrid CMOS output stage to generate a carry.

MVT 18 Transistor full adder [3] uses the concept of Mixed Threshold Voltage to improve performance. This is done by using high V_{th} transistors to reduce the leakage power consumption and using low V_{th} transistors to yield lesser delay in critical circuit branches.

PTL-TGL full adder [2] uses pass transistor logic and transmission gate logic to develop low power full adder by reducing the number of transistors. In Pass Transistor Logic the output voltage swing is degraded, which is due to the threshold loss problem. This full adder thus requires a higher voltage to compensate for the threshold loss, which is a disadvantage in low voltage circuit designs.

The Low Power High Speed Hybrid Full Adder[1] uses an XOR gate that is not directly powered by the supply voltage. It therefore has low power consumption that reduces its PDP. Its delay is higher due to the lower drive capability of its XOR gate.

The rest of the paper is organised as follows. Section 2. presents the proposed 1-bit full adder with its functionality. Section 3. describes the simulation set-up. Section 4. compares the proposed 1-bit full adder with architectures proposed earlier [12-14]. Finally, conclusions are drawn in section 5.

Proposed 1-bit Full Adder: The power consumption in a digital CMOS VLSI circuit has three main components [11]. The primary component is the switching power consumption that is due to charging and discharging of the circuit capacitances during transistor switching. Short circuit power consumption is due to short circuit current flowing from the power supply

to ground during transistor switching. Lastly, static power consumption is due to static and leakage currents flowing while the circuit is in stable condition. Reduction in Short circuit power consumption and static power consumption lead to reduction in power consumption without degrading drive capability. The total power is given by;

$$P_{Total} = V_{dd} \cdot f_{clk} \cdot \Sigma_i V_{swing} \cdot C_{load} \cdot P_i + V_{dd} \cdot f_{clk} \cdot \Sigma_i I_{isc} + V_{dd} I_i \quad (1)$$

where,

V_{dd} is power supply voltage, V_{swing} is the voltage swing of the output which is equal to V_{dd}, C_{load} is the load capacitance at the node 'i', f_{clk} is the system clock frequency, p_i is the switching activity at node 'i', $I_{i\,sc}$ is the short circuit current at node 'i', I_i is the leakage current. The summation is over all the node capacitances of the circuit.

Reducing the number and magnitude of the circuit capacitances, transition activity, reducing the voltage swing at the internal nodes to reduce short circuit current and reducing spurious transitions at the output signal, are the techniques used at circuit level to reduce power consumption. The proposed design reduces the number and magnitude of the circuit capacitances by reducing the number of transistors used.

The 1-bit Full Adder cell is a three-input, two-output combinational circuit with the following Boolean equation.

$$SUM = (A \odot B) C_{in} + (A \oplus B) \overline{C_{in}}$$

$$C_{out} = A(A \odot B) + C_{in} (A \oplus B)$$

The three inputs are A, B and C_{in} and the two outputs are C_{out} and SUM. The proposed 1-bit full adder comprises of three modules. The first module is a circuit that uses four NMOS pass transistors to produce XOR and XNOR Boolean functions as shown in Fig. 1. The two PMOS are cross connected to raise the output voltage to V_{dd}. This is done to avoid the "Threshold Voltage Drop" problem that arises due to the use of pass transistors. There is also an increase in the drive capability of the cell. The first module has A and B as inputs and generates (A XOR B) and (A XNOR B) output. It uses four NMOS and two PMOS transistors. It also requires complementary inputs. Two other modules are used to generate SUM and CARRY outputs.

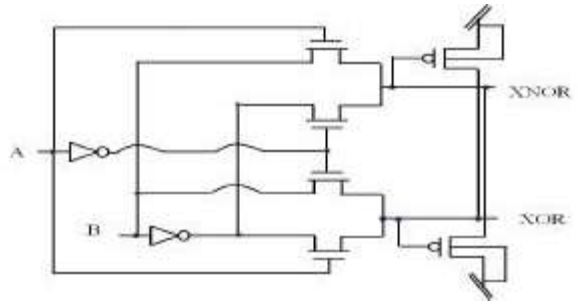


Fig. 1: Circuit that produces (i) A XOR B and (ii) A XNOR B

The module shown in Fig. 2 provides SUM output and is basically an XOR circuit. The inputs to this circuit are C_{in}, (A XOR B) and (A XNOR B). It consists of two NMOS and two PMOS transistors. In this circuit the SUM output is generated by the following Boolean equation.

$$SUM = (A \odot B) C_{in} + (A \oplus B) \overline{C_{in}}$$

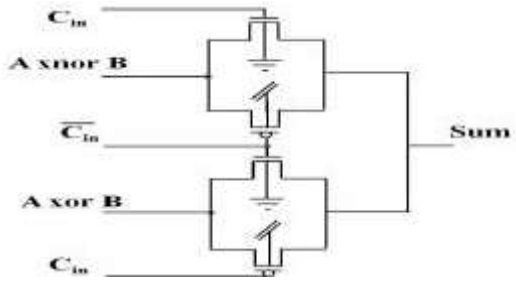


Fig. 2: Module that generates "SUM" output.

The module that provides CARRY output is shown in Fig. 3. The inputs to this circuit are (A XOR B) and (A XNOR B), C_{in} and A. It consists of two NMOS and two PMOS transistors. The NMOS and PMOS are connected together to form a transmission gate. In this circuit the carry output is generated by the following Boolean equation using two transmission gates.

$$C_{out} = A(A \odot B) + C_{in} (A \oplus B)$$

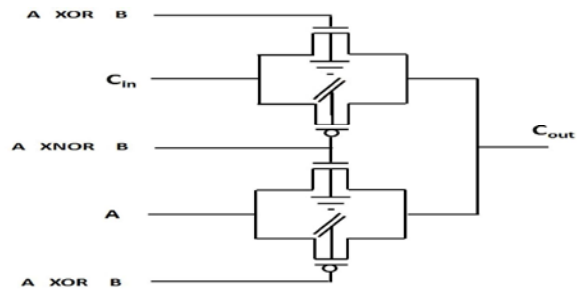


Fig. 3: Module that generates "CARRY" output.

Simulation Setup: The proposed full adder is simulated in a set up that resembles real environment as shown in Fig. 4. Real environment means that realistic waveforms are fed to inputs A, B and C_{in} by inserting two symmetrical inverters before the inputs. The sum output and the carry output are connected to an output load of 5.6 fF that is equivalent to a fan-out of four inverters (FO4). Each inverter has a capacitance of 1.4fF in 0.18-nm technology). Power dissipation is evaluated by averaging the power flowing into the full adder.

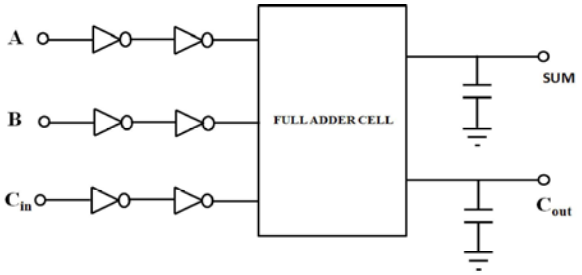


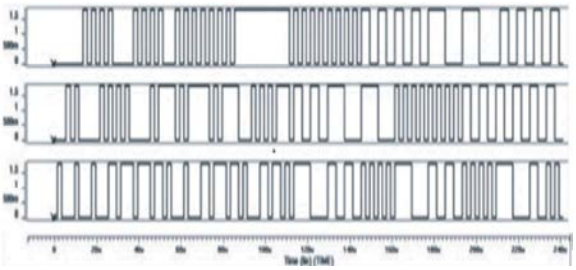
Fig. 4: Set-Up used for simulation

RESULTS AND DISCUSSIONS

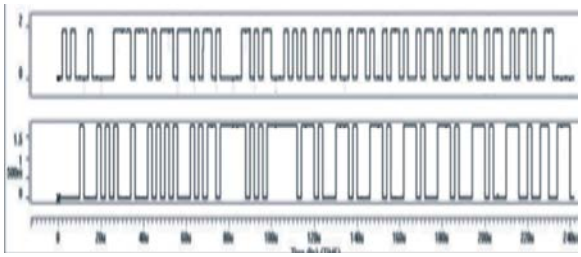
The proposed circuit is implemented on Tanner S-Edit using TSMC 0.18 µm technology. The circuit performance is evaluated in terms of worst case delay, power consumption and power delay product for a supply voltage of 1.8V and a signal of 50 MHz frequency. Fig. 5 shows the inputs A, B and C_{in} with a frequency of 50 MHz.

Based on the simulation results overall improvements of 60.77%, 0.25% and 60.84% are observed in delay, power consumption and power delay product respectively. This circuit works up to 5 Ghz for an output load of 5.6 fF.

The circuit used for simultaneous generation of XOR and XNOR shown in Fig. 1 is based on complementary pass-transistor logic with cross connected PMOS. This circuit has higher power consumption and but higher drive capability. SUM and CARRY are generated from the circuit that has very low power consumption. The resulting Full Adder made from, CPL logic based XOR-XNOR and the circuit for SUM and CARRY generation gives lesser delay and lower power consumption. It is seen that an XOR/XNOR gate with good drive capability reduces delay considerably. The proposed one bit full adder requires lesser number of transistors *i.e.* twenty. It does not have



(a) Inputs A, B and C_{in}



(b) Outputs SUM and C_{out}

Fig. 5: (a) The three signals are inputs A, B and C_{in} (b) The two outputs are SUM and C_{out}. Frequency of the inputs is 50 MHz with a supply voltage of 1.8 V.

Table 1: Simulation results for the proposed full adder in 0.18-µm technology at 50-MHz frequency and 1.8V V_{DD}.

Design	No. of Transistors	Power(nW)	Delay(ps)	PDP(e^{-17})
C-CMOS	28	60.27	456.8	2.7531
CPL	32	82.56	554.2	4.5754
TGA	20	48.83	326.1	1.5923
TFA	16	44.99	353.7	1.5912
HPSC	22	42.06	548.9	2.7198
New HPSC	26	36.20	455.7	1.605
Hybrid-CMOS	24	35.82	352.3	1.2619
*LP-HS-Hybrid	16	34.91	224.6	0.784
Proposed	20	34.82	88.1	0.307

Fig 6 Output of proposed Flip Flop V_{out}

*LP-HS-Hybrid [2]

dissipation due to short circuit current and static current. Therefore all the power is used to improve drive capability.

CONCLUSION

A new high speed full adder cell is proposed and compared with existing designs. The performance parameters of this full adder cell are better than the full adder cells reported till date. Based on the simulation results overall improvements of 60.77%, 0.25% and 60.84%

are observed in power, delay and power delay product respectively. The proposed Full Adder works at higher clock frequency and is useful up to 5GHz. It is hence useful in high performance and low power environments.

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