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Generator of Graph Models of Computationally-Converter Circuits as a Stream Processors of Virtual Instrument Framework

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Abstract: General formulation of structural synthesis of streaming processors in the class of computationally-converter circuits based on operational elements with control parameter is presented. Its' decomposition on several private graph tasks: 1) research the problem of the solvability of the general task; 2) research the conditions of construction of a class of minimal computationally-converter circuits with peer s-model; 3) reduction of the derived set of competitive nonreducible structures (N-structures) with the specified rank value; 4) determination of whether the N-structures are isomorphic structures; 5) research the problem of the algorithmic verification of the condition of cyclic connectivity of N-structures (with engagement of apparatus of algebra of structural numbers) - is given. The limitations for creation a class of the minimal (according to the number of using operational elements) computationally-converter circuits with peer model for virtual instruments frameworks (VI-frameworks) are established.

Key words: Virtual instruments frameworks (VI-framework) · IP-blocks · Stream processes · *S*tructural synthesis of computationally-converter circuits · CAD emerging knowledge base

INTRODUCTION

The Research Community which is working at formal methods of synthesis of computationally-converter circuits [1-4], succeeded in exploration of its mathematical aspects. But things are in a bad way with feed movement of the methods in practice of computer-aided design engineering of real IP-blocks (IP) [5] and the following replication of useful practice for its realization in virtual instrument (VI-framework) [6]. Although, we can see the sustainable growth of projects with formal methods. Yet, this practice of computer-aided design engineering is rather exception than norm.

In the article we look upon usage of structural number means for combinatorally-topologic synthesis of minimal computationally-converter circuits by compilation (in a number of operative with linear operated elements variable) with equivalent approximating ability in class of rational functions.

General Formulation: General problem of synthesis comes to generation of complete set of nonisomorphic unreduced structures (*N*-structures) $II(r, r_{kk})$ *s*-models of computationally-converter circuits, each of which makes sure fixed value of rangs (polynomial degree in numerator and nominator of rational coversine) r and r_{kk} at minimum number of operational elements (OE) from the basic set, in other words:

$$F\{H_T, rang(S), rang'(S_{kn})\} \to \min_{H_T \in \tilde{H}_T} \qquad (1, A)$$

where:

$$rang(S) = r \qquad (1, b)$$

$$rang'(S_{kn}) = r_{kk} \qquad (1, c)$$

$$T = \{T_1, T_2\} \qquad (1, d)$$

$$H_T \not\cong H'_T \qquad (1, e)$$

$$\underset{\alpha \in A}{\exists} \quad \underset{\beta \in A}{\forall} \quad \left(\frac{\partial A}{\partial \alpha} \cap \frac{\partial A}{\partial \beta} \neq 0 \right) \qquad (1, f)$$

Here $F\{g\}$ - is a composed functional which is given in ground set H_T labeled *N*-structures $H_T, rang(g)$? $rang'(g)$ - are functionals of calculations of rangs r and r_{kk} of structural models of computationally-converter circuits; S and S_{kn} - respectively peer *s*- models of computationally-

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converter circuits with open cycle and short-circuited outermost co-ordinate poles; T- two- conventional set of OE; ratio sign « $\neq$ » reflects nonisomorphy of N-structures H_T и H'_T, which are the elements of the ground set $\tilde{H}_T$; A - is a structural number, which has N-structure H_T as a reversal geometrical of image; $\frac{\partial A}{\partial \alpha}$ and $\frac{\partial A}{\partial \beta}$ - are algebraic derivations of a structural number A up to α and β, respectively.

Approaches to a Solution of the Problem: There are two essentially different approaches to the solution of the problem.

The first approach provides for combinatory mode of its solution as extremum problem in graphs.

Within the limits of the second approach it comes to solution of the systems of the component equation. And in case of other equal constraints better solution is one which contains maximum possible number of zero parameters of OE which builds full typological structure of circuit [7, 8]. For the purpose of concerned class of circuits with non-linear operated module, realization of this approach presents severe difficulties so algorithmic as computation mode. It can be explained by discreteness and multiextrimeness, also the complexity of constraint satisfaction for structural circuit constants when usage of steady setting of the problem involves difficulties for its solution.

I consider more reasonable decomposition of general synthesis problem (which includes problems of parametric and structural synthesis) into two problems:

- Search for Ration Structure
- Calculation of options of OE circuit with found structure complying with posed factors of quality.

For sure we shouldn't set and solve these problems in absolute independence from each other. The stages of parametric and structural synthesis are connected in consequence of interactive character of the search of the best engineering solution. And it determinates necessity of multiple solution of the problems. But spent additional timing recourses in comparison to solution of general problem of synthesis by method of solution of component equation within the framework of full topological structure (for sure in case of successful outcome, which warrants globality of the optimum) of circuit are compensated by simplification of the process of structure synthesis and process of ES calculation of parameters in case of posed structure of circuit. Practical experience which was gained during solution of wide range of problems of computationally-converter circuits' synthesis confirms productivity of this point of view. That is why in the following presentation of questions of structural synthesis I will follow above-named the first (combinatory) approach.

Problems Decomposition: From the formulated general problem of synthesis we can point out partial problems which have individual value. Solution is affected in case of restrictions of running N-structure. Each of them is a subgraph of a graph of a full topological structure with fixed number of state points. In this case the question that has to be answered is a question about existence of the solution for this problem.

The content of the first partial problem contains investigation of questions about solubility of partial problem. If in the set of constraints (1, A-f) we leave only one restriction for rang of circuit, i. e. do not take into consideration identification of outermost poles and consider it without of account of relation with outside framework, we will come to the problem of synthesis of peer circuit. This is the second partial problem. It contains investigation of conditions of creation of minimal computationally-converter circuits with peer s-model. It is important to note that desirable birank minimal circuit is an element of class of peer circuits with fixed value of rank.

Constraint satisfaction (1, c) composes the content of the third partial problem - is restriction of given range of competitive structure in a result of the solution of the second problem. They have fixed value of rang $r(r_{kk})$ set of structure which are complies with the meaning of the second rang r_{kk}. Here account of link of computationally-converter circuits with outside framework on the basis of identification of outermost pair of poles is appears.

Combinatory character of the solution of above-named partial problems doesn't except creation of two and more birank structures which are models of the same computationally-converter circuits. By identity we shall mean isomorphism of its N-structure in case of fixed pair of outer vertex.

The problem of evaluation whether N-structures are isomorphic or not is making up a content of the forth partial problem which reflects realization of the restriction of the forth partial problem which reflects realization of the restriction (1, e). The problem of network isomorphism belongs to a number of the most difficult in a graph theory [9-11]. In work [12] we see that the problem belongs to a class of problems which have NP-fullness. Some methods exist for it. These are methods of network isomorphism establishment of standard form with polynomial dependency of time of solution from of the problem dimension. All known pure algorithms are characterized by exponential relationship of time of solution from the problem dimension. The account of characteristics of the analyzed class of problems in graphs provides an opportunity to work out useful for majority of practical problems of isomorphism setting process using some heuristic rules. While using as an invariant of circuit graph of its presented structure (*P*-structures), it is possible to make a process of graph isomorphism establishment using some heuristic rules.

The account of cyclic connectivity in a process of synthesis of N -structures of computationally-converter circuits is helpful to the restriction of a number of competitive structures which are minimal by its complexity $(1, f)$. Investigation of the question about algorithmization of condition examination of cyclic connectivity composes a contest of the fifth partial problem. Algebra's means of structural numbers [1] is invoked for its solution, which serves to automation of this not simple procedure in a process of the analysis of computationally-converter circuits structures.

There is a clearly big affinity in statement of the partial problem of synthesis of two- and double-pole of computationally-converter circuits. The main difference consists in characteristic parameter of *N*-structures and in those topologic operands which are connected with evaluation and calculation of circuits' ranks because of condition of constraint with outside framework.

Synthesis of Minimal by Rang S-Model of Computationally-Converter Circuits: According to the work [3] the next synthesis of the theorem of *N*-structure of *s*-model of computationally-converter circuits is correct:

Theorem: Minimal by rang r *N*-structure of computationally-converter circuits is a grouping

$$H_{T_{r_{\min}}} = DR_\nu \dot{\cup} DR_\eta \qquad (2)$$

of two adjoint graphs DR_ν и $DR_\eta, DR_\nu \in \tilde{DR}_\nu, DR_\eta \in \tilde{DR}_\eta$, .

Here $\dot{\cup}$ - is the index of the graph's composition which means application of two graphs whereby their final vertices with common names are in line.

Deduction: As far as the *N*-structure is minimal by rang r, then, as it was shown in work [3], it has only one pair of adjoint graphs, $\langle DR_\nu, DR_\eta \rangle$ where DR_ν - is a graph from twigs of type g but DR_η - is a graph from twigs of type

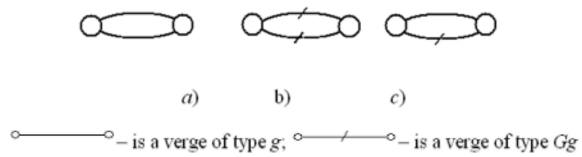

Fig. 1: Variants of minimal by rang r = 1 N-structures are possible.

$G\theta$, where $card\left(DR_\nu \dot{\cup} DR_\eta\right) = 2r$. As long as $DR_\nu \dot{\cup} DR_\eta \subseteq H_{T_{r_{\min}}}$ and $cardH_{T_{r_{\min}}} = 2r$, then $H_{T_{r_{\min}}} = DR_\nu \dot{\cup} DR_\eta$, which was to be proved.

We will show that there is a *N*-structure $H_{T_{r_{\min}}}$, which is minimal according to rang r. We will pursue the deduction by method of mathematical induction. Suppose $r = 0$. Then $n = 1$, $m = 0$. But resulting graph is not going to correspond to the determination of *N*-structure [2], which speculates occurence, as a minimum, of two points. Suppose $r = 1$. Then $n = 2$, $m = 2$ and the next three variants of *N*-structures (Figure 1) are possible. Rang of *N*-structure, which is illustrated in Figure 1, *c*, is equal to 1, 1i. e. *N*-structure, which is minimal by rang $r = 1$, exists. Assuming that there is *N*-structure $H_{T_{r_{\min}}}$, minimal by rang $r = p$. Then, $n = p + 1$, $m = 2p$ and $H_{T_{p_{\min}}} = DR_\nu^p \dot{\cup} DR_\eta^p$, where $\left\langle DR_\nu^p \dot{\cup} DR_\eta^p \right\rangle$ - is the only one pair of adjoint graphs of *N*-structure, where DR_ν^p - is a graph from twigs of type g and DR_η^p - is a graph from twigs of the type $G\theta$.

We will show that there is the *N*-structure $H_{T_{(p+1)_{\min}}}$, which is minimal be rang $r = p + 1$. Suppose X^p - is a vertex set of *N*-structure $H_{T_{(p+1)_{\min}}}$. This structure can be built in such a manner:

$$H_{T_{(p+1)_{\min}}} = H_{T_{(p)_{\min}}} \dot{\cup} \begin{pmatrix} \langle x^*, x_{p+1} \rangle & \langle x^{**}, x_{p+1} \rangle \\ G\theta & g \end{pmatrix} \qquad (3)$$

where, x^*, $x^{**} \in X_p$ (as possible $x^* = x^{**}$), $x_{p=1} \notin X_p$. The number of points of *N*-structure is equal to $p + 1$, the number of verges is - $-2p + 2$. We will show that rang is equal to $p + 1$. In fact,

$$H_{T_{(p+1)}} = DR_\nu^p \dot{\cup} DR_\eta^p \dot{\cup} \begin{Bmatrix} \langle x^*, x_{p+1} \rangle & \langle x^{**}, x_{p+1} \rangle \\ G\theta & g \end{Bmatrix} \qquad (4)$$

$$= DR_\nu^{p+1} \cup DR_\eta^{p+1}$$

where DR_ν^{p+1}, DR_η^{p+1} - are graphs of *N*-structure $H_{T_{(p+1)}}$,

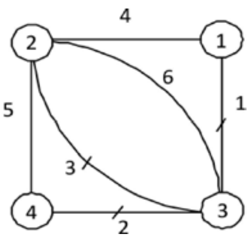

Fig. 2: Variant of minimal by rang r = 3 N-structure

respectively, from the twigs of type g and $G\theta$ (it can be easily checked on determination of the rang). It is obvious that the pair $\left\langle DR_{\nu}^{p+1}, DR_{\eta}^{p+1} \right\rangle$ is the pair of adjoint graphs of *N*-structure ${}^{H}T_{(p+1)}$. Then, allowing for the fact that

$$r = \eta - \nu \qquad (5)$$

where $\eta = G_\eta$, $\nu = G_\nu$, but G_η and G_ν - is a number of twigs of type G_θ in graphs DR_η and DR_ν , we will get $r = p + 1$. Besides, as far as the pair $\left\langle DR_{\nu}^{p}, DR_{\eta}^{p} \right\rangle$ is unique, then pair $\left\langle DR_{\nu}^{p+1}, DR_{\eta}^{p+1} \right\rangle$ is also unique. Then *N*-structure ${}^{H}T(p+1)$ is minimal by rang $r = p + 1$, i. e. ${}^{H}T(p+1) = {}^{H}T(p+1)_{\min}$.

Example: It takes to construct a minimal by rang $r = 3$ *N*-structure of circuit in a basic set of OE.

In consideration of above-mentioned, the number of points of *N*-structure is $n = 4$ and the number of verges is $m = 6$. We will find one of possible variants of *N*-structure is shown in Figure 2. Δ- coversine of circuit *s*-model, which corresponds to *N*-structure, in structural numbers algebra:

$$\Delta(\theta) = \det_{\{G\theta,\, g\}} A \qquad (6)$$

where A = [1 4] [3 4 5 6][1 2 3 6] - structural number, the geometrical illustration of which is the graph of circuit *N*-structure (Figure 2). As follows from the multiplication of single-line structural numbers, we get

Therefore

$$\Delta(\theta) = \theta^3 G_1 G_2 G_3 + \theta^2 \begin{bmatrix} G_1 G_2 (G_4 + G_5 + G_6) \\ +G_1 G_3 G_5 + G_2 G_3 G_4 \end{bmatrix} + \qquad (7)$$
$$+\theta\left[G_4 G_5 (G_1 + G_2 + G_3) + G_1 G_5 G_6 + G_2 G_4 G_6\right] + G_4 G_5 G_6$$

Here G_i - are conductances of OE of depicted, in *N*-structure of circuit, correspond, according to the number, verges $i = 1 \div 6$.

CONCLUSIONS

- The catolicity of the recommended combinatorially-algebraic approach of graph model generating of computationally-converter circuits provides an opportunity to penetrate a universally recognized process complicity of stream processes' investigation for a virtual instrument framework.
- General problem of structural synthesis is illustrated in the form of convolution for partial problems, which have individual valuation. The decomposition speculates taking into account constraints, which limit running *N*-structures. Each of them is a linked subgraph of topological structure with fixed number of points.
- Decline of competitive structures, which are minimal by compilation, speculates account in process of synthesis of *N*-structure of computationally-converter circuits of its cyclic connectivity. Investigation of questions about cyclic connectivity makes a contest of a separate partial problem. For its solution it is reasonable to invoke algebra means of structural numbers and it provides a possibility to automatize this difficult procedure while analyzing of computationally-converter circuits.

REFERENCES

1. Bellert, S. and G. Vozniacki, Analysis and synthesis of electric circuit by method of structural numbers / Transl. from pol. edited by P.A. Ionkina. - M.: Mir, 1972. pp: 332.
2. Gerasimov, I.V. and S.V. Rodionov, 1980. About a possibility of usage of the method of structural numbers for synthe-sis of the functional generator in terms of the elements with linearly-driven argument // Methods of organization and engineering of computer equipment. - L.: Leningrad Electronic Technical Institute Press, No. 278. - S. 17-21.
3. Gerasimov, I.V., 1986. The theory of designing and usage of computationally-transforming circuits (synthesis and realization): Dissertation of Doctor of Engineering. - L.: LETI, pp: 420.
4. Gerasimov, I.V. and N.M. Safyannikov, 2003. Evolution of the problem of structural analog calculations: quantum computing // Mercury of young academics. Line «technology»,- ^{1} 6. - S. 3-16.

5. Gerasimov, I.V., N.M. Safyannikov and D.O. Yakimovskii, 2012. Composite function blocks of mixed system semi-conductor element: automatization of functional designing: Monograph / edited by I.V.Gerasimov. - SBR.: Publishing office «ELMOR», pp: 236.
6. Gerasimov, I.V., S.A. Kuzmin, L.N. Lozovoi and A.V. Nikitin, 2010. The main teology of complementary engeneering of scientific product: Monografy. - SBR.: Publishing office SBRSETU «LETI», pp: 196.
7. Lanne, A.A., 1978. Optimal synthesis of linear electric scheme. - M.: Sviaz, pp: 336.
8. Lanne, A.A., E.D. Mihailiva, B.S. Sarkisian and Y.N. Matvijchuk, 1982. Optimal realization of linear electronic RLC-circuits. - Kiev: Scientific Thought, pp: 208.
9. Kristofides, N., 1978. The theory of graphs: Algorithmic approach. - M.:Mir, pp: 432.
10. Ilnickij, L.Y., 1971. The usage of bilinear approximations in the theory of functional generator. - Kiev: Scientific thought, pp: 224.
11. Wilson, R., 1977. Introduction to the graph theory. - M.: Mir, pp: 207.
12. Svami, M. and K.Thulasiraman, 1984. Graphs, networks and algorithms. - M.: Mir, pp: 455.