New Noise Tolerant Domino Logic Circuits

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Abstract: In this paper, we propose four wide domino circuits to improve the robustness and reduce the power consumption. All proposed circuits use small potential at the source of the pull down network in the standby mode. Simulation is done using 90nm HSPICE for 32 input OR gate. Our proposed circuits reduce power consumption by 11.75% to 41.85%, improvement of unity noise gain by 41.03% to 90.87% and have better figure of merit as compared to conditional keeper domino.

Key words: Domino logic • Keeper ratio • Standby power • Power consumption • Unity noise gain

INTRODUCTION

Domino logic is very fast and requires less area as compared to static CMOS logic. It is used in high performance critical system such as microprocessor, multiplexor etc. As the technology is scaled down, supply voltage is reducing. This reduces the power consumption. Threshold voltage is also scaled to maintain the required performance. Low threshold voltage of the transistor, increase the subthreshold and gate oxide leakage current [1, 2]. However, low threshold voltage makes the domino circuit more prone to input noises. The main source of noise signal in deep-submicron circuits are crosstalk, leakage current, charge sharing and supply noise. These noise signals reduce the robustness of the domino circuit. High leakage current discharges the dynamic node and make the logic failure of the domino circuit. A remedy of the problem by using weak pMOS keeper at the dynamic node. Keeper provides immunity against noise and leakage current. Conventional method for improving the robustness of the domino circuit is the upsizing the keeper ratio. The keeper ratio is K is defined as the ratio of the current driving capability of the keeper transistor to the evaluation transistor.

\[ K = \frac{\mu_n(W/L)}{\mu_p(W/L)} \]

where \( W \) and \( L \) denote the size of transistor, \( \mu_p \) and \( \mu_n \) are the motilities of hole and electron, respectively. Size of the pull down network is fixed and the size of the keeper is variable. Increasing the value of \( K \) improves the robustness but has two negative effects on power consumption. First, it increases the contention current between the keeper and the pull down network which increases the short circuit power consumption. Second, dynamic and output node capacitance increases which increase switching power consumption. Upsizing of keeper also increase the delay of the domino circuit. There is tradeoff between the robustness and speed [3-7]. This method is not reliable solution because it increases the speed and power consumption of the domino circuit. Other conventional method to improve robustness is using high threshold voltage transistor at the expense of speed [8-13]. Different techniques are proposed in the literature to deal this issue. High speed domino logic and conditional keeper domino are the effective technique as compared to conventional footless domino logic circuit.

In this paper, we propose three robustness footed domino logic circuits and one footless domino logic circuit. These circuits use small voltage at the source of pull down network in the standby mode. The remainder of the paper is organized as follows. Previous proposed circuit techniques are described in section 2. The noise immunity metric for our study are described in section 3.
Fig. 1: Standard footless domino high fan-in OR gate without keeper.

Fig. 2: Standard footless domino high fan-in OR gate with keeper.

Fig. 3: Standard footed domino high fan-in OR gate.

Fig. 4: Wide domino OR gate using HS domino keeper technique [14].

The proposed circuits is explained in section 4. Simulation results is presented in section 5 and conclusion is presented in section 6.

**Previous Work:** Dynamic node of footless domino circuit (FLDL) is very sensitive to noise is shown in Fig 1. Once the dynamic node is discharged due to noise signal, its data cannot be recovered. During evaluation phase dynamic node must be stable. Fig. 2 shows the standard footless domino logic with keeper. By adding nMOS footer transistor at the source of the pull down network it becomes footed domino logic circuit (FDL) is shown in Fig 3. FDL minimize the leakage current due to stacking effect at the cost of speed. Several circuit techniques have been proposed in the literature such as HS Domino [14, 15], conditional keeper domino circuit [16] etc. Main idea regarding these circuit designs to improve circuit performance and noise robustness.

**High Speed Domino Logic (HS Domino):** The n-input HS-Domino OR gate [14] is shown in Fig 4. This is similar to standard domino footless keeper except keeper gate is connected to output through nMOS transistor M4 and pMOS transistor M3. The operation of HS-Domino are as follows. During precharge phase, clock is low, dynamic node is charged to VDD through pull-up transistor M1. After delay of two inverter, transistor M4 is OFF, M3 is ON, charged the gate of transistor M2 to high voltage. Thus keeper transistor M2 turns OFF.
Fig. 5: Wide domino OR gate using conditional keeper technique [16].

At the start of the evaluation phase, delayed clock output is low thus keeper transistor M2 is OFF. When any one input of the circuit is high, dynamic node is discharged to ground, output is charges to high and keeper transistor is remaining OFF. After delay of two inverter, transistor M4 is ON, M3 is OFF and again M2 is OFF. Thus this circuit solves the problem of contention current during evaluation phase. Similarly, all inputs are low, dynamic node is high, output node is low, after delay of two inverters, transistor M2 turns ON to maintain the dynamic node VDD against charge sharing and charge leakage.

Conditional-keeper Domino Logic (CKD): The n-input conditional keeper domino (CKD) OR gate [16] is shown in Fig 5. Here, we use two keepers, week keeper M2 (fixed keeper) and strong keeper M3 (conditional keeper). When clock is low, dynamic node is charged to VDD, week keeper M2 turns ON and strong keeper M3 turns OFF. At the start of evaluation phase (clock low to high) week keeper turns ON. After a delay of \( T_{\text{keeper}} = T_{\text{delay element}} + T_{\text{NAND}} \), keeper M3 gets activated. Transistor M3 is conditional keeper, it turns ON only if the dynamic node is high. Thus conditional keeper improves noise immunity of the circuit. Week keeper provides small contention current to the pull down network, this improves the speed of the circuit and it is also sufficient to maintain the noise immunity during \( T_{\text{keeper}} \). Keeper sizes are chosen such that \( W(M0) = W(M2) + W(M3) \). Where \( W(M0) \) is the standard keeper size, \( W(M2) \) is the week keeper size and \( W(M3) \) is the strong keeper size. For high performance and better noise immunity, \( W(M0) \) is 10% of the size of pull down network.

Other Previous Techniques: Hamid Mahmoodi et al. [17] proposed a technique that diode is connected in series with the pull down network. Due to stacking effect, leakage current is reduced and enhanced the robustness of the circuit. For improving the speed, current mirror is also employed in the pull down network to increase the evaluation current. Simulation is done in 70nm technology for 32 bit input, it improves robustness 5.8\( \times \) as compared to standard footless domino and 4.1\( \times \) as compared to conditional keeper domino under the same delay.

A. Peiravi et al. [18] proposed a technique that diode circuit. For improving the speed, current mirror is also employed in the pull down network to increase the evaluation current. Simulation is done in 70nm technology for 64 bit input, it improves robustness by 17.7\( \times \) as compared to standard footless domino and 10.6\( \times \) as compared to conditional keeper domino under the same delay.

F. Moradi et al. [19] proposed a circuit employs footer transistor that is initially OFF in the evaluation phase to enhance immunity and turn ON to complete evaluation. Proposed circuit improves noise immunity by 26\( \times \) and provides 20% improvement in speed as compared to standard footless domino circuit.

Noise Immunity Metric and Figure of Merit: Noise immunity of the domino circuit is measured by applying noise pulse at the inputs. Noise amplitude is varied such that static gate output has same noise amplitude. In this measurement, duration of input noise pulse is kept 50ps (for 90nm technology). Metric used for leakage and noise robustness comparison is unity noise gain. Unity noise gain is the amplitude of noise at the inputs that produce same amplitude at the output [17]. The UNG metric is given by

\[
\text{UNG} = \{ V_{\text{noise}}; V_{\text{noise}} = V_{\text{out}} \} \tag{2}
\]

UNG is the important parameter for measuring noise immunity. We use a pulse noise here at the input. For measurement of the UNG, either pulse duration or pulse amplitude is varied. In our simulation we varied the pulse amplitude. We proposed figure of merit (FOM) for the design of wide OR domino gate. Figure of merit in terms of noise, total power consumption, standby power and propagation delay.

\[ FOM = \frac{UNG_{\text{norm}}}{I_d \times P_{\text{tot-norm}} \times P_{\text{s-norm}}} \]  

(3)

Where \( UNG_{\text{norm}} \), \( P_{\text{tot-norm}} \) and \( P_{\text{s-norm}} \) are unity noise gain, propagation delay, total power consumption and standby power consumption, respectively. Each of the parameter is normalized to the value of HS domino circuit. For better circuit the value of FOM must be high.

**Proposed Circuits:** Proposed circuit adopts negative gate-source voltage at the source of the pull down network to improve robustness of the circuit. In the evaluation phase, when all inputs are low, subthreshold leakage current flows from dynamic node o the source of the pull down network. Subthreshold leakage current can be expressed

\[ I_{\text{sub}} = I_0 e^{\frac{V_{ds}}{kT/q}} (1 - e^{\frac{V_{ds}}{kT/q}}) \]  

(4)

where \( I_0 = \mu_0 C_{ox} \left( \frac{W}{L} \right)^2 \) e\(^{1.8} \), \( W \) and \( L \) are the transistor channel width and length, \( \mu_0 \) is the low field mobility, \( C_{ox} \) is the gate oxide capacitance, \( k \) is the Boltzmann constant, \( q \) is the electronic charge, \( V_{ds} \) and \( V_{gd} \) are the gate to source and the drain to source voltages, \( n \) is the subthreshold swing factor.

\[ I_{\text{sub1}} = I_{\text{sub2}} = I_{\text{sub}} = I_0 e^{\frac{V_{ds}}{kT/q}} (1 - e^{\frac{V_{ds}}{kT/q}}) \]  

(5)

\( V_X \) represents dc voltage to the source of pull down network as shown in Fig 6.

\[ I_{\text{Leakage}} = \sum_{i=1}^{n} I_{\text{sub}} \]  

(6)

where \( i \) is the number of transistor in the pull down network. For wide fan-in inputs, leakage currents increase and dc voltage value also increase.

\[ V_X = I_{\text{Leakage}} \times R_X \]  

(7)

where \( R_X \) is the parasitic resistance at the node X. Threshold voltage of the transistor is given by

\[ V_{th} = V_{tho} + \gamma (\sqrt{2F_P} + V_{sb}) - \sqrt{2F_P} \]  

(8)

where \( V_{tho} \) is the threshold voltage when \( V_{sb}=0 \), \( \gamma \) is the body effect coefficient, \( 2F_P \) is the silicon surface potential at the onset of strong inversion, \( V_{sb} \) is the source to body voltage. As the dc voltage at node X increase, it increases the threshold voltage of the pull down transistor due to body bias effect. However, robustness of the circuit increases. In the following section, we proposed four circuits to reduce power consumption and improve robustness of the domino circuit.

**Proposed Circuit 1:** Circuit diagram of proposed circuit 1 is shown in Fig. 7 this is similar to FDL except footer transistor is controlled by control circuit. The control circuit consist of even number of inverter and NOR gate. Clock is connected to the footer transistor through control circuit. The operation of the circuit is explained in two different phase.

During precharge phase, clock is low and pull up transistor M1 turns ON. Dynamic node is charged to VDD and output discharges to low. Keeper transistor M2 turns ON, it helps in charging the dynamic node.
During evaluation phase, clock is high, pull up transistor M1 is OFF. There are two different cases in evaluation phase.

**Any One Input Is High:** At the start of evaluation phase, dynamic node is high and output is low. For short interval of time, delayed of two inverter is low and NOR gate turns ON. After delay of \( T_{\text{foot}} = T_{\text{Delay Element}} + T_{\text{NOR}} \), footer transistor M5 get conditional turn ON when both inputs of NOR gate are low. Dynamic node is discharged to low before the footer delay voltage changes from high to low. After delay of two inverter, its voltage changes from low to high. NOR gate turns OFF and it turns OFF the M5. At this stage footer node F_Node is floating and bump small potential \( V_x \) at the node N_Foot. Upsizing the pull down network elevate the footer node voltage, width of pull down network is varied from 2.5\( \mu \)m to 5\( \mu \)m is shown in Fig 8. Upsizing the footer transistor lowers the footer node voltage. \( V_x \) provides negative gate-to-source potential and increase the threshold voltage of the pull down network. This increase the robustness of the circuit. The characteristic of the circuit is shown in Fig 9.

**All Inputs Are Zero:** In standby mode, dynamic node is maintained high and output is low. Footer delay is low and it turns OFF the M5. Footer node N_Foot is again floating which improves the robustness of the domino circuit.

**Proposed Circuit 2:** Then input proposed circuit 2 is shown in Fig 10 and its characteristics in Fig 11. The footer transistor M5 is controlled by control circuit. The control circuit consists of even number of inverter and EXOR gate. The EXOR gate is controlled by output of non inverting delay and dynamic node. Clock is connected to the M5 through control circuit. Operation of the circuit is divided into two phase.

When clock is low, precharge phase, dynamic node is charge to VDD by pull up transistor M1 and output is discharge to low voltage. Keeper transistor M1 is turns ON to precharge the dynamic node. Output of control circuit is high which turn ON the footer transistor. No input is applied to the pull down network during precharge to avoid short circuit current. When clock is high, evaluation phase, M1 is OFF. M5 is conditional transistor and it will turn ON depends on the input combination of the EXOR gate. There are two different cases in the evaluation phase.

![Fig. 8: N_Foot voltage versus pull transistor width and footer transistor width.](image1)

![Fig. 9: Proposed circuit1 waveforms in standby mode.](image2)
Any One Input Is High: At the beginning of the evaluation phase, dynamic node is high and output is low. For short duration of time, output of non-inverting delay element is low. Due to the combination of input of the EXOR gate is (1, 0), it turn ON the EXOR gate and activate the M5. Dynamic node is discharge to zero before the output of non-inverting delay changes to high. After the delay of non-inverting element, its output changes from low to high. Therefore, input combination of EXOR gate is (0, 1) and gain the M5 remains ON.

All Input Is Zero: In this case, dynamic node is maintained high against the noise. Input combination of EXOR gate is (1, 1) which turns OFF the gate and deactivate the M5. At this stage footer node N_foot is floating and small potential $V_x$ is produced which provide negative gate-source voltage to the pull down network. This increase the robustness of the circuit.

Proposed Circuit 3: Another proposed circuit is shown in Fig 12 and their characteristic is shown in Fig 13. Footer transistor is controlled by control circuit. Its control
Fig. 12: Proposed circuit 3.

Fig. 13: Proposed circuit 3 waveforms in standby mode.

circuit consists of odd number of inverter. The operation is described as follows. During precharge phase, operation of the proposed circuit is similar to previous proposed circuits. When clock is high, evaluation phase there are two different cases in evaluation phase.

**Any One Input Is High:** At the beginning of the evaluation phase, dynamic node is high and output is low. For short interval of time, delay of three inverters is high. It turns ON the M5 which discharges the dynamic node to zero voltage before the output of delayed element changes to low. After the delay of three inverters its output changes from high to low which turns OFF the M5.Node. N_Foot becomes floating and small voltage V_s is generated. This improves the robustness of the domino circuit during rest of the evaluation phase.

**When All Input Is Zero:** In this case, dynamic node must be high. Output of controlled circuit is low which turns OFF the M5. Node N_Foot is floating which improves the robustness of the circuit.

**Proposed Circuit 4:** Another new proposed circuit is shown in Fig 14.This circuit is similar to FLDL circuit except the source of the pull down network is connected to the output of the control circuit. Control circuit consists of odd number of inverter and NOR gate. Inputs of the NOR gate is the output of inverting delay and output of the domino circuit.

The operation of the circuit is explained into two phases. During precharge phase, when clock is low, dynamic node is charged to VDD and output to low. Node X becomes zero voltage. When clock is high, there are two different cases in the evaluation phase.
Any One Input Is High: At the start of the evaluation phase, dynamic node is high and output is low. For short interval of time, delay of three inverters output is high. Input combination of NOR gate is (0, 1) makes the node X low. This helps in discharging the dynamic node to low voltage. After the delay of three inverters its voltage changes from high to low. Input combination of NOR gate becomes (1, 0). This again retains the node X low voltage.

When All Input Is Low: In this case, output maintains low voltage. Input combination of NOR gate is (0, 0). This turns the node X high. High voltage at node X avoids subthreshold leakage in the pull down network and increase the robustness of the circuit.

Simulation Results: The proposed circuits are simulated using HSPICE in the high performance 90-nm predictive technology [20] and the operating temperature for technology is 110°C. The supply voltage in the simulations is 1V and clock rate is 2.4GHz with 50% duty cycle (clock period is 420ps) for wide fan-in (4,8,16,32) OR gate circuit. Rise and fall time of the clock rate is set equal to 1ps. Simulations are done using load capacitance of 8fF. Transistor size is set by $W_{\text{PMOS}} = 13L_{\text{min}}$, $W_{\text{PMOS}}/W_{\text{NMOS}} = 2$ for whole circuit except keeper transistor and inverters are minimum size. For better performance and noise tolerant, keeper ratio $K$ of the proposed circuits is set to 0.1.

Worst case delay is determine from input IN1 to the output node $V_{\text{out}}$ in the evaluation phase while other inputs are applied to zero voltage. Power consumption is
Table 1: Comparison of Number of transistor, Delay, Power Consumption, PDP and UNG of the various existing circuits based on 32-input OR gate.

<table>
<thead>
<tr>
<th>Domino circuits</th>
<th>No of Transistor</th>
<th>Delay(ps)</th>
<th>Power(µW)</th>
<th>PDP(fJ)</th>
<th>UNG (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard footless</td>
<td>36</td>
<td>27.807</td>
<td>286.41</td>
<td>7.96</td>
<td>0.2625</td>
</tr>
<tr>
<td>HS domino</td>
<td>42</td>
<td>27.595</td>
<td>518.89</td>
<td>14.318</td>
<td>0.2619</td>
</tr>
<tr>
<td>Conditional keeper</td>
<td>47</td>
<td>31.727</td>
<td>540.67</td>
<td>17.153</td>
<td>0.2773</td>
</tr>
</tbody>
</table>

Table 2: Comparison of Number of transistor, Delay, Power Consumption, PDP, UNG, standby power and short circuit power of the existing HS domino circuit and three proposed circuit based on 32-input OR gate.

<table>
<thead>
<tr>
<th>Domino circuits</th>
<th>No of Transistor</th>
<th>Delay (ps)</th>
<th>Power (µW)</th>
<th>PDP (fJ)</th>
<th>UNG (V)</th>
<th>Standby Power (µW)</th>
<th>FOM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conditional keeper</td>
<td>47</td>
<td>31.727</td>
<td>540.67</td>
<td>17.153</td>
<td>0.2773</td>
<td>186.73</td>
<td>1.00</td>
</tr>
<tr>
<td>Proposed1</td>
<td>46</td>
<td>31.136</td>
<td>395.46</td>
<td>12.31</td>
<td>0.4259</td>
<td>116.73</td>
<td>3.44</td>
</tr>
<tr>
<td>Proposed2</td>
<td>48</td>
<td>45.025</td>
<td>477.09</td>
<td>21.48</td>
<td>0.5293</td>
<td>165.31</td>
<td>1.39</td>
</tr>
<tr>
<td>Proposed3</td>
<td>42</td>
<td>26.176</td>
<td>314.38</td>
<td>8.22</td>
<td>0.3911</td>
<td>54.534</td>
<td>10.22</td>
</tr>
<tr>
<td>Proposed4</td>
<td>46</td>
<td>37.981</td>
<td>403.95</td>
<td>15.34</td>
<td>0.4625</td>
<td>253.69</td>
<td>1.74</td>
</tr>
</tbody>
</table>

Fig. 16: Delay vs. number of fan-in.

Fig. 17: Power consumption vs. number of fan-in.

Fig. 18: PDP vs. number of fan-in.

We simulated the existing circuit standard footless domino, high speed domino logic and conditional keeper domino to compare the number of transistor, delay, UNG, power consumption and PDP is shown in Table 1. From table it is clear that conditional keeper domino has maximum UNG at the cost of speed. Conditional keeper domino is high noise tolerant circuit among existing circuit. So we compare the simulation parameter of proposed circuits with the conditional keeper domino is shown in Table 2. From table it is clear that proposed circuits has significant improvement in UNG by 41.03% to 90.87% and power consumption by 11.75% to 41.85% as compared to HS domino circuit at the cost of speed. Proposed circuit 3 has better delay, PDP, standby power and FOM as compared to other topologies.

Comparison of delay, power consumption, PDP, UNG and standby power for 4,8,16 and 32 input OR gate of four proposed circuits with conditional keeper domino is shown in Fig 16 to Fig 21. From the figure it is clear that if we increase fan-in, delay, power consumption, PDP and standby power increases. In conditional keeper domino UNG drops as fan-in increase but in our proposed circuits
for wide fan-in UNG increase because voltage drop at footer node increases causing higher threshold voltage of the pull down network.

UNG is plotted against noise duration pulse in Fig 22. From figure it is clear that small noise duration pulse provides higher noise immunity, noise immunity decrease as noise pulse duration increase. Our proposed circuits have better noise immunity as compared to conditional keeper domino. UNG is plotted against temperature is shown in Fig 23. UNG of conditional keeper proposed 3 and proposed 4 circuit decreases as temperature increase. Similarly, UNG of proposed1 and proposed2 circuit increase as temperature increase. The layout of the standard domino and proposed circuit are implemented in Tanner L-EDIT tool using 0.18um standard CMOS technology as shown in Fig.24. Further, the proposed circuit1 required 3.23×, proposed circuit 2 required 4.98×, proposed circuit 3 required 2.45× and proposed circuit 4 required 3.43× larger area as compared to standard domino circuit.
CONCLUSION

In this paper, four new circuit techniques are proposed. Three circuits are footed and one circuit is footless. The main idea by using these techniques to produce small potential at the source of pull down network, this provide negative gate to source voltage and increase the robustness of the circuits. Existing and proposed circuits are simulated in 90nm using HSPICE for wide fan-in 4 to 32-bit OR gate circuit.

Results of the proposed circuits show improvement in robustness by 41.03% to 90.87% and power consumption reduction by 11.75% to 41.85%. Proposed circuit 3 has better delay, PDP and standby power as compared to other topologies. Moreover, figure of merit (FOM) that includes UNG, power consumption, propagation delay and standby power. Therefore, proposed circuits are superior design, especially for wide fan-in gates. The proposed circuit 1 required 3.23×, proposed circuit 2 required...
4.98×, proposed circuit 3 required 2.45× and proposed circuit 4 required 3.43× larger area as compared to standard domino circuit.

REFERENCES


