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A 12Ghz Fractional-n Extended TSPC Frequency Dividers Using 0.18µm CMOS Technology

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Abstract: In this paper, the design of fractional-n (n: 2, 3, …, 8) extended True-Single-Phase-Clock (E-TSPC) frequency dividers with 0.18µ CMOS technology and TSMC process is presented. The proposed structure operates up to 12GHz and therefore a 12GHz sinusoidal input voltage applies to produce simulation results. The E-TSPC circuits have a small area occupation, extremely low power consumption (less than 220µW from 1.8V supply voltage) and 50% duty-cycle sinusoidal output voltage. The linear noise (with 10Hz,100Hz and 1kHz bandwidths) at the output nodes of E-TSPC frequency dividers are calculated and the maximum linear noise of circuits is about 325nV. The new MOSFETs aspect ratio for FF (fast-fast) and SS (slow-slow) corner process are presented and analyzed. The high-swing sinusoidal input voltage and 1pF load capacitance impact on the E-TSPC structure have been investigated and Advanced Design System (ADS) used to produce simulation results.

Key words: Frequency Divider · Extended TSPC · Fractional-n · 0.18 µm CMOS Technology

INTRODUCTION

With the development of the wireless communication system, studies depend on communication circuits and structures has attracted a lot of attention. The main challenges are a low-price, low-voltage, small-area and low-power components that merged performance with the capability to be constructed economically in Large quantities. Recently, there has been an extra emphasis on integration of heterogeneous parts that organized a communication transceiver. The new transceivers perform over a wide range of frequencies [1]. A phase-locked-loop (PLL) is one of the major parts for transceivers. PLLs are often utilized for frequency synthesis to produce an input local oscillator signal to up-conversion in the transmitter and down-conversion in the receiver. It is also used to generate HF (High Frequency) oscillations in a new communication system component [2]. A PLL synthesizer consists of four parts: phase detector (PD), a loop filter (LF), a voltage controlled oscillator (VCO) and a frequency divider (FD) [3]. In PLL synthesizer, frequency divider is the most significant parts that consumes a large power as compared to other parts. True-Single-Phase-Clock (TSPC) dividers are recognized for low power consumption as compared to the current-mode-logic (CML) frequency dividers, but their operation is confined to the low frequency range. With the explosive growth of CMOS Technologies, the improvement of the speed of a component causes the TSPC logic gates superseded CML even in high-frequency operations. The prescaler is a synchronous structure that consists of D flip-flops and added logic gates. Because of the concatenate of more logic gates among the flip-flops to attain the two distinct division ratios, the speed of the prescaler is influenced and the switching power incremented. Conventional high speed FF based divide-by counter designs utilize current-mode-logic (CML) latches and having a problem with large load capacitance. This is not only confines the operating frequency and current-drive ability, but also increments the whole power consumption. FF based divide-by counter designs adjust dynamic logic FFs (flip-flop) such as True-Single-Phase-Clock (TSPC). The designs can be further increased by utilizing extended True-Single-Phase-Clock (E-TSPC) FFs for high-speed and low power consumption components. E-TSPC designs canceled the transistor stacked structure so that

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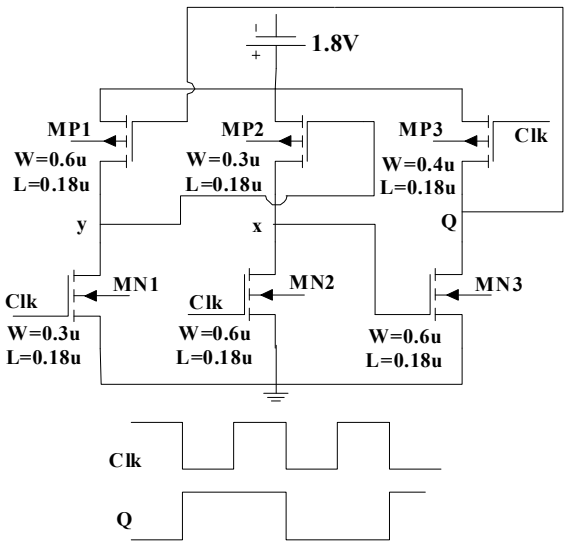

Fig. 1: Divide-by-2 E-TSPC frequency divider

all the transistors are free from the body effect. They are thus more suitable for high operating frequency applications with low voltage power supply [4]. In this paper the high-speed, small area occupation and low power consumption fractional-n (n: 2, 3,…, 8) E-TSPC frequency dividers with 0.18µm and TSMC process is presented. The proposed structure operates up to 12GHz and consumes less than 220µW from 1.8V supply voltage. The linear noise (with 10Hz, 100Hz and 1kHz bandwidths) at the E-TSPC output nodes are calculated and the MOSFETs new aspect ratio for FF and SS corner process presented. High-swing sinusoidal input voltage and 1pF load capacitance impact on E-TSPC circuits are investigated. This structure is suitable for high-resolution, fast-speed, small area occupation, low-noise and low power consumption frequency synthesizers in wireless communication.

Analysis of Extended-TSPC (E-TSPC): Fig. 1 displays the divide-by-2 E-TSPC frequency divider. It consists of six transistors, three PMOS labeled as MP1, MP2 and MP3 and three NMOS labeled as MN1, MN2 and MN3. The aspect ratio of MOSFETs in this type of DFF (D flip-flop) are very significant. The PMOS drains connected to NMOS drains. Input Clock (Clk) and the output (Q) are shown in Fig. 1. The circuit operates in pre-charge and evaluation mode.

In the pre-charge mode, before arriving at the falling edge of the Clock, Clock is high and Q has a low value. The x node is discharged to low and when the aspect ratio of MP1 is greater than MN1, y has a high value. At the falling edge of the Clock, MN1 and MN2 operate in cutoff region. MP1 is still connected, so the output (Q) is charged up faster than the x node and MN1 remains in cutoff region. Therefore in pre-charge mode, the node x has a low value while y and Q have high values.

In the evaluation mode, MN1 and MN2 are connected on the rising edge of the clock, both MP2 and MN2 are connected and operated in triode region and the y node is discharged quickly, which turns MP2 on. For the suitable performance, the voltage on x node required to has a low value and the aspect ratio of MN2 necessary to be greater than MP2. Therefore, the aspect ratio of MP2 should be less than 3.3. Based on this, MN3 remains in cutoff region and the output (Q) keeps it's high value. Similarly, the aspect ratio of MN3 should be greater than MP3 and the aspect ratio of MP1 should be larger than MN1 [5].

E-TSPC frequency divider is needed only a single clock to resolve clock skew problems. The E-TSPC load capacitance is obtained from Eq. (1). E-TSPC switching power depends on the load capacitance as Eq. (2), described. In Eq. (2), C_L is load capacitance, f_{Clk} is operating frequency and V_{dd} is a 1.8V power supply.

$$C_L = C_{dbMN3} + C_{gdMN3} + C_{dbMP3} + C_{gdMP3} + C_{gMP1} \quad (1)$$

$$P_{sw} = f_{Clk}.C_L.V_{dd}^2 \quad (2)$$

The period of time during which a straight path creates between the power supply and ground is known as short-circuit power. The short-circuit power depends on the MOSFETs aspect ratio and the duty-cycle of the input voltage. The E-TSPC flip-flop utilizes smaller switching power, but higher short-circuit power as compared to the TSPC frequency divider. The short-circuit power creates every fourth of a duty-cycle clock when the Extended-TSPC flip-flops are working as a divide-by-2 circuit [6]. It is also expressed that the short-circuit power in Extended-TSPC structures is larger and depends on the MOSFETS aspect ratio.

In E-TSPC frequency divider the power consumption is affected by the variation in the DC level and the amplitude of the clock signal obtained from the VCO which, is sinusoidal and its DC level and amplitude can be included in the design of the VCO in a phase locked loop (PLL). In E-TSPC circuit, the DC level should be high for negative edged clock circuits to obtain low power

Table 1: E-TSPC Circuit specifications

	Divide-By-2	Divide-By-3	Divide-By-4	Divide-By-5	Divide-By-6	Divide-By-7	Divide-By-8
(W/L)MN1	0.3/0.18	0.4/0.18	0.4/0.18	0.225/0.18	0.22/0.18	0.3/0.18	0.3/0.18
(W/L)MN2	0.6/0.18	0.65/0.18	0.65/0.18	0.77/0.18	0.77/0.18	0.8/0.18	0.9/0.18
(W/L)MN3	0.6/0.18	0.65/0.18	0.65/0.18	0.77/0.18	0.77/0.18	0.9/0.18	1.2/0.18
(W/L)MP1	0.6/0.18	0.65/0.18	0.65/0.18	0.77/0.18	0.77/0.18	0.9/0.18	1.2/0.18
(W/L)MP2	0.3/0.18	0.4/0.18	0.4/0.18	0.77/0.18	0.77/0.18	0.8/0.18	1/0.18
(W/L)MP3	0.4/0.18	0.5/0.18	0.5/0.18	0.67/0.18	0.67/0.18	0.7/0.18	0.8/0.18
DC_L(mV)	730	560	510	480	450	450	450
AMP range(mV)	1-500	1-500	1-500	1-500	1-500	1-500	1-500

Table 2: E-TSPC Power Consumption.

	Divide-By-2	Divide-By-3	Divide-By-4	Divide-By-5	Divide-By-6	Divide-By-7	Divide-By-8
P_C (µW)	212	180	162	184	180	183	186

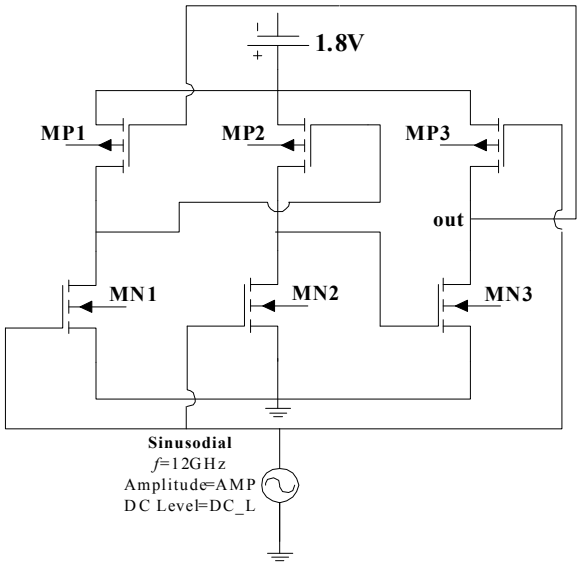

Fig. 2: Fractional-n (n: 2, 3, …, 8) E-TSPC frequency divider structure

consumption and power consumption is significantly varied with respect to the DC level and amplitude of the clock signal. E-TSPC circuits also need larger amplitude for the clock signal compared to that of TSPC circuits [7].

Proposed Fractional-n E-TSPC: A fractional-n (n: 2, 3,…, 8) E-TSPC frequency dividers structure with improved speed, low power and less area occupation are proposed. The circuits consist of two D type flip-flops, six MOSFET and 12GHz sinusoidal input voltage as Fig. 2 Shown. Transistors dimensions and the amplitude and DC level of sinusoidal input voltage are displayed in Table 1. E-TSPC output and input signals have a duty-cycle of 50%. The peak to peak amplitude of the input signal can be varied from 1mV to 500mV. Fractional-n E-TSPC simulation results displayed in Fig. 3 (Note that for simplicity the DC level of sinusoidal input voltage, as mention in Table 1, is not shown).

The power consumption of E-TSPC frequency dividers are presented in Table 2. The maximum power consumption of proposed E-TSPC is 212µW from 1.8V supply voltage and it belongs to divide-by-2 circuit.

Transistors have an uncertainly in parameters such as *Leff*, *Vt* and *tax*. Process corners describe the worst case variations. If a design works in all it will probably work for any variation. Table 3 displays fractional-n E-TSPC frequency dividers transistor's dimensions with FF (Fast-Fast) and SS (Slow-Slow) corner process. The SS corner process has a smaller transistor's size than the FF corner process as Table 3 mentioned. However, the SS corner process needs sinusoidal input voltage with higher DC level as compared to the FF corner process. Transistor's size in fractional-n E-TSPC frequency dividers with SS and FF corner process increment by increasing n (n: 2, 3, …, 8). To achieve sinusoidal output voltage with 50% duty-cycle, the amplitude of sinusoidal input voltage must be in the range from 1mV to 500mV. Fig. 4 shows the structure of E-TSPC circuits with high sinusoidal input and output swing. In these circuits the

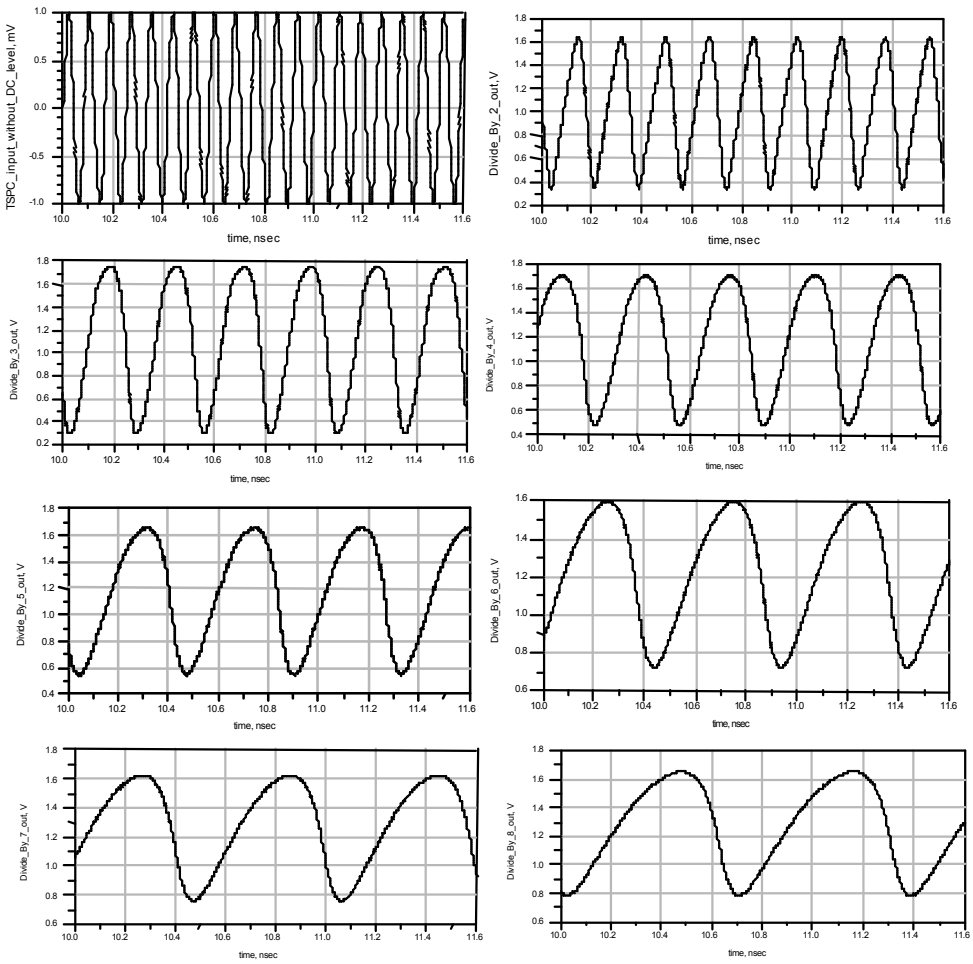

Fig. 3: Fractional-n E-TSPC frequency dividers input and output signals

Table 3: E-TSPC Transistors Dimensions with FF and SS Corner Process

	Divide-By-2		Divide-By-3		Divide-By-4		Divide-By-5		Divide-By-6		Divide-By-7		Divide-By-8	
	FF	SS	FF	SS	FF	SS	FF	SS	FF	SS	FF	SS	FF	SS
(W/L)MN1	0.3/0.18,	0.22/0.18	0.4/0.18,	0.22/0.18	0.3/0.18,	0.3/0.18	0.3/0.18,	0.3/0.18	0.5/0.18,	0.4/0.18	0.6/0.18,	0.4/0.18	0.5/0.18,	0.5/0.18
(W/L)MN2	0.6/0.18,	0.3/0.18	0.6/0.18,	0.3/0.18	0.4/0.18,	0.3/0.18	1.1/0.18,	0.4/0.18	1.1/0.18,	0.5/0.18	1.2/0.18,	0.5/0.18	1.2/0.18,	0.6/0.18
(W/L)MN3	0.6/0.18,	0.3/0.18	0.65/0.18,	0.4/0.18	0.8/0.18,	0.6/0.18	1.2/0.18,	0.8/0.18	1.5/0.18,	1/0.18	0.2/0.18,	1.3/0.18	2.3/0.18,	1.7/0.18
(W/L)MP1	0.6/0.18,	0.3/0.18	0.65/0.18,	0.4/0.18	0.85/0.18,	0.6/0.18	1.2/0.18,	0.8/0.18	1.5/0.18,	1/0.18	2/0.18,	1.3/0.18	2.3/0.18,	1.7/0.18
(W/L)MP2	0.3/0.18,	0.22/0.18	0.6/0.18,	0.3/0.18	0.8/0.18,	0.5/0.18	1.2/0.18,	0.8/0.18	1.5/0.18,	1/0.18	2/0.18,	1.3/0.18	2.3/0.18,	1.6/0.18
(W/L)MP3	0.4/0.18,	0.22/0.18	0.55/0.18,	0.3/0.18	0.4/0.18,	0.3/0.18	0.4/0.18,	0.3/0.18	0.5/0.18,	0.4/0.18	0.6/0.18,	0.5/0.18	0.6/0.18,	0.6/0.18
DC_L(mV)	500,	900	430,	750	400,	700	400,	680	400,	630	400,	620	400,	600
AMP range(mV)	1-500		1-500		1-500		1-500		1-500		1-500		1-500	

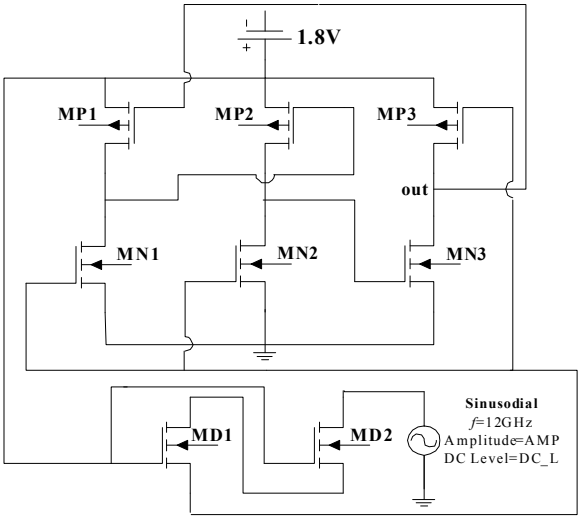

Fig. 4: E-TSPC structure with high sinusoidal input and output swing

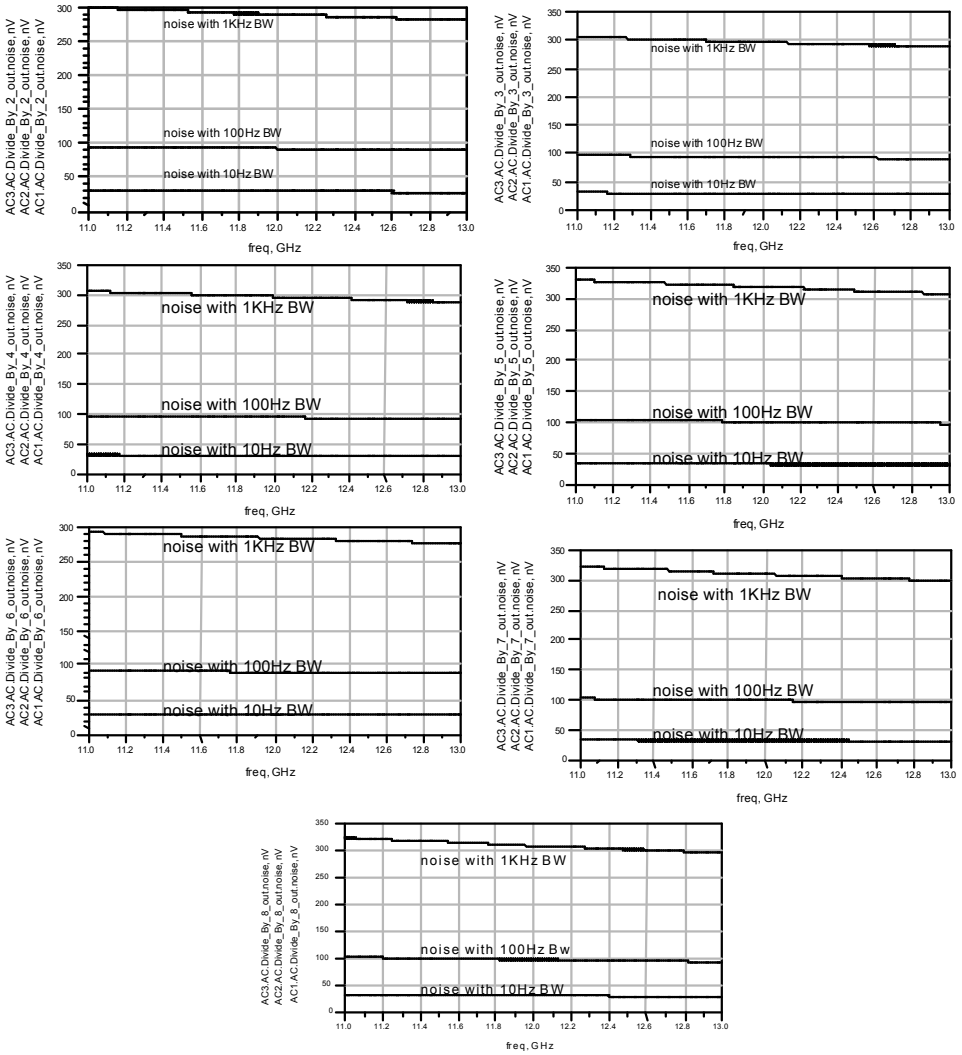

Fig. 5: Fractional-n (n: 2, 3,…, 8) E-TSPC linear noise at output node

amplitude of 12GHz sinusoidal input voltage can be in the range from 1mV to 2V and the circuits provide sinusoidal output voltages proportional to input amplitude swing. MD1 and MD2 gates are connected to Vdd and worked in triode region. These transistors decrease the input sinusoidal amplitude before the signal applies to E-TSPC frequency divider circuit. In triode region MD1 and MD2 operate as variable resistance as Eq. (3) and (4) described. The amplitude divides between R_{MD1} and R_{MD2} proportional of the parameter's value and then applies to E-TSPC frequency divider circuits.

Fig. 5 shows the amplitude of linear noise with 10Hz, 100Hz and 1kHz bandwidths in considering frequency at the output nodes of E-TSPC frequency dividers.

$$R_{MD1} \approx \frac{1}{\mu_n.C_{ox}.\left(\frac{W}{l}\right)_{MD1}.(Vdd - V_{SMD1} - V_t)} \quad (3)$$

$$R_{MD2} \approx \frac{1}{\mu_n.C_{ox}.\left(\frac{W}{l}\right)_{MD2}.(Vdd - V_{SMD2} - V_t)} \quad (4)$$

Linear noise in the ADS consists of four parts (as ADS help mention):

- Temperature-dependent thermal noise from lossy passive elements, including those specified by data files.
- Temperature and bias-dependent noise from nonlinear devices.
- Noise from linear active devices specified by 2-port data files that include noise parameters.
- Noise from noise source elements.

The Linear noise with 10Hz and 100Hz bandwidths have an equal values for all fractional-n (n: 2, 3, …, 8) E-TSPC frequency dividers. Whereas fractional-n (n: 5, 7 and 8) E-TSPC frequency dividers have a greater linear noise with 1kHz bandwidth value than the others.

E-TSPS with High-Swing Sinusoidal Input and 1pF Load Capacitance: At high frequency, the next-stage MOSFETs parasitic capacitors influenced on E-TSPC output speed and swing. According to MOSFET's structure these parasitic capacitors are distributed and their exact calculation is quite complex. However, the values of MOSFET parasitic capacitors can be obtained by using simple approximation [8]. High-swing sinusoidal input fractional-n E-TSPC frequency dividers with 1pF load capacitance are considered. To achieve a high output swing, E-TSPC MOSFET's aspect ratio should be increased to provide the necessary current for load capacitor. Fig. 6 displays the structure of E-TSPC frequency divider circuits with 1pF load capacitance. For fractional-n (n: 6, 7, 8) E-TSPC, the output buffer should be used to provide high-swing sinusoidal output as Fig. 6 shown. Fractional-n E-TSPC transistor's dimensions with 1pF load capacitance are presented in Table 4. Fig. 7 displays proposed E-TSPC simulation results (Note that for simplicity the DC level

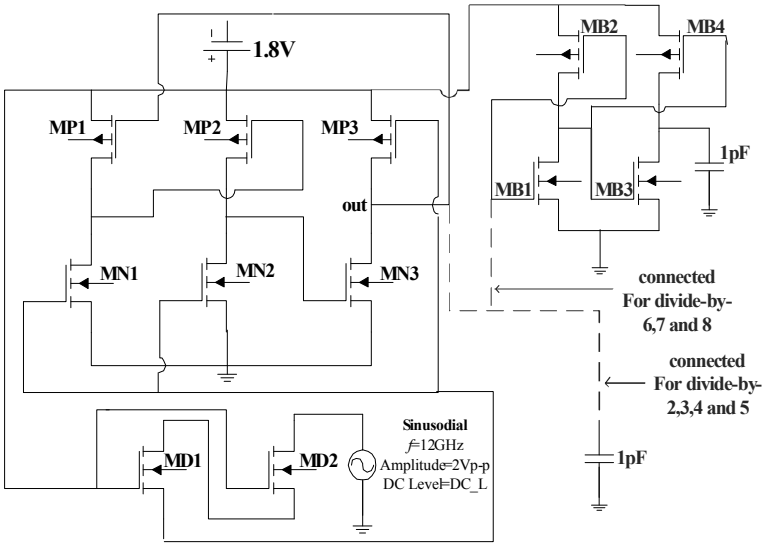

Fig. 6: The structure of high-swing sinusoidal input E-TSPC with 1pF load capacitance

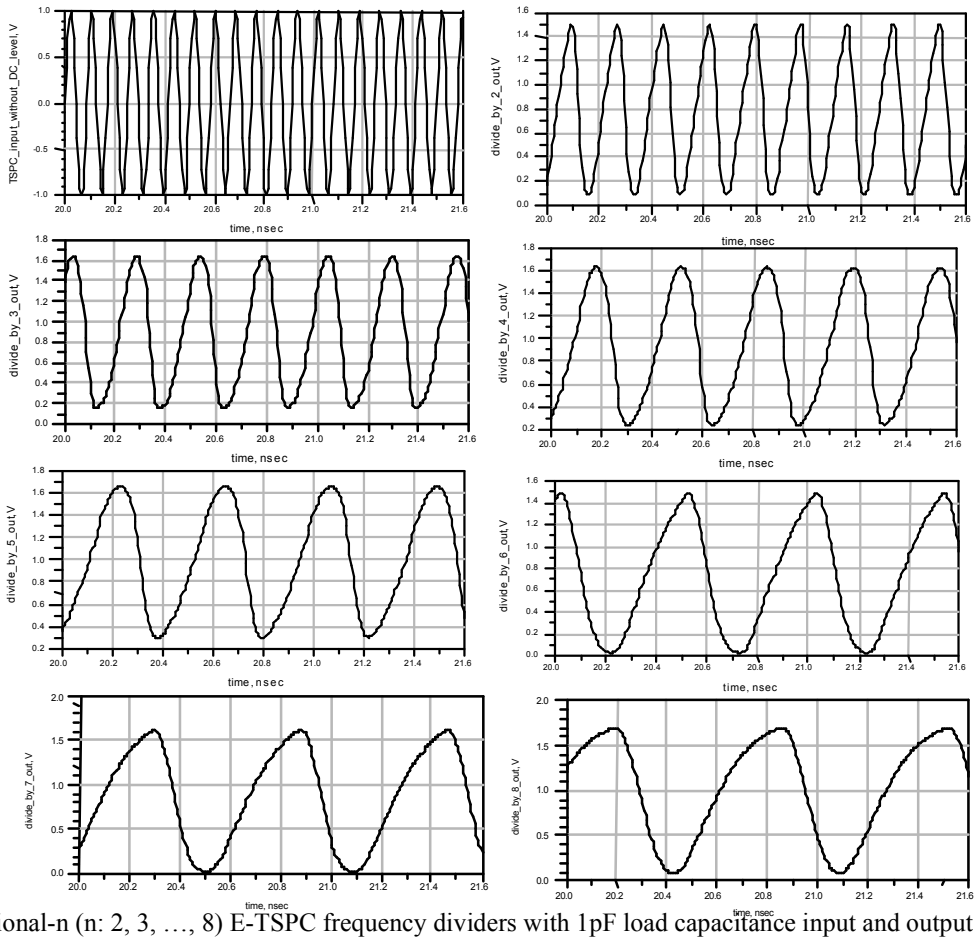

Fig. 7: Fractional-n (n: 2, 3, …, 8) E-TSPC frequency dividers with 1pF load capacitance input and output signals

Table 4: High-Swing Sinusoidal Input E-TSPC Transistors Dimensions with 1pF Load Capacitance.

	Divide-By-2	Divide-By-3	Divide-By-4	Divide-By-5	Divide-By-6	Divide-By-7	Divide-By-8
(W/L)MN1	480/0.18	480/0.18	460/0.18	380/0.18	400/0.18	400/0.18	400/0.18
(W/L)MN2	500/0.18	500/0.18	500/0.18	500/0.18	500/0.18	500/0.18	500/0.18
(W/L)MN3	500/0.18	500/0.18	500/0.18	500/0.18	500/0.18	600/0.18	600/0.18
(W/L)MP1	490/0.18	490/0.18	500/0.18	600/0.18	600/0.18	600/0.18	600/0.18
(W/L)MP2	480/0.18	480/0.18	480/0.18	480/0.18	480/0.18	500/0.18	500/0.18
(W/L)MP3	490/0.18	490/0.18	490/0.18	490/0.18	490/0.18	500/0.18	500/0.18
(W/L)MB1	-	-	-	-	10/0.18	10/0.18	7.5/0.18
(W/L)MB2	-	-	-	-	40/0.18	40/0.18	40/0.18
(W/L)MB3	-	-	-	-	25/0.18	25/0.18	25/0.18
(W/L)MB4	-	-	-	-	25/0.18	30/0.18	25/0.18
DC_L(mV)	700	820	750	750	690	670	650
AMP range(mV)	1-2000	1-2000	1-2000	1-2000	1-2000	1-2000	1-2000

Table 5: Power Consumption of High-swing Sinusodial Input E-TSPC Frequency Dividers with 1pF Load Capacitance.

	Divide-By-2	Divide-By-3	Divide-By-4	Divide-By-5	Divide-By-6	Divide-By-7	Divide-By-8
P_C (mW)	270	266	230	214	202	196	187

of sinusoidal input voltage, as mention in Table 4, is not shown). The power consumption of the E-TSPC circuits are increased By incremented in an aspect ratio of MOSFETs (to provide the necessary current for load capacitance and achieving a high sinusoidal output swing). The fractional-n E-TSPC circuits with 1pF load capacitance consume about 225mW power from a 1.8V supply voltage.

Table 5 describes the power consumption of the E-TSPC circuits with 1pF load capacitance. The E-TSPC divide-by-2 has the maximum value of the power consumption and the divide-by-8 has the least power dissipation.

CONCLUSION

Fractional-n (n: 2, 3,…, 8) extended True-Single-Phase-Clock (E-TSPC) frequency dividers with 0.18µm CMOS technology and TSMC process have been successfully designed and simulated. Proposed structure operates up to 12GHz and therefore a 12GHz sinusoidal input voltage applies to produce simulation results. Considered E-TSPC frequency dividers have a 50% duty-cycle sinusoidal output voltage and consumes less than 220µW power from a 1.8V supply voltage. The fractional-n E-TSPC linear noise with 10Hz, 100Hz and 1kHz bandwidths are presented and the circuits linear noise had the maximum value about a 325nV. The high-swing sinusoidal input voltage and 1pF load capacitance impact on the E-TSPC structure have been investigated. Simulation results show improvement in speed, area occupation, resolution and power consumption as compared to conventional E-TSPC. This structure can use in Fast-speed, low-noise, low power and small area occupation frequency synthesizer.

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