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A Novel Approach to Reduce Sub Threshold Leakage in Deep Sub-Micron SRAM

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Abstract: This paper deals with design opportunities of Static Random Access Memory (SRAM) for low power consumption. Initially three major leakage current components are reviewed and then for a 6T SRAM cell, some of the leakage current reduction techniques are discussed. Finally double finger latch is analyzed and compared with single finger latch which shows reduction in sub threshold leakage current.

Key words: SRAM % SOC % DIBL % DRV % SNM

INTRODUCTION

In SOC devices, the area and power consumption of SRAM increases largely with technology scaling. Thus they are critical components in both high performance processors and other portable devices. So in modern VLSI designs, SRAM energy power becomes a major issue and low power SRAM design without compromising speed performance is crucial. The low leakage SRAM is of prime concern as 30% of total chip consumption is due to memory circuits. SRAM cell design considerations are important because design of SRAM cell is key to ensure stable and robust SRAM operation. To enhance on-chip storage capacity, packing density is increased, so SRAM cell must be as small as possible while meeting stability, speed, power and yield constraints. In scaled technologies, cell stability is of paramount significance and SNM (Static Noise Margin) is measure of cell stability. The SRAM cell consumes energy in both dynamic and static ways. Historically, the primary source of power dissipation has been dynamic energy due to word line decoding, bit line charging / discharging, sense amplification, output driving and so on. As we move into sub-micron technology, scaling of the transistor threshold voltage sharply increases the sub threshold leakage current, whereas, the ultra-thin gate oxide results in an exponential increase in gate leakage current. Fig. 1 shows the SRAM leakage current with technology scaling and it indicates that the leakage current has dramatically increased when technology scales down to 90 nm and below.

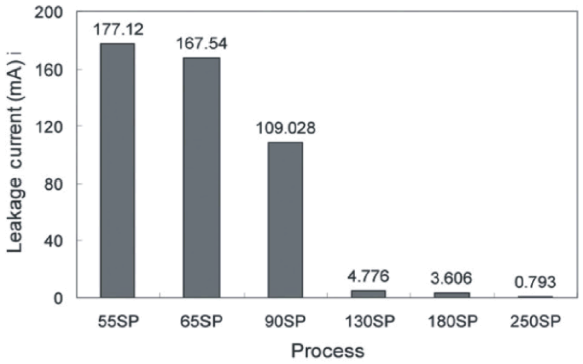

Fig. 1: SRAM leakage current with technology scaling

Leakage Current Components in 6t Sram Cell: Fig. 2 shows the structure of the conventional 6T SRAM cell. One bit memory cell is constructed by PMOS and NMOS transistors. There are four main sources of major leakage current in CMOS Transistor. First, is Gate Leakage due to very thin gate oxide, I_G becomes the dominant leakage source for CMOS technologies beyond 45nm. Second is the junction Leakage current (I_j) which occurs due to the heavily doped halo doping profile [1]. The junction leakage occurs from the source or drain to the substrate

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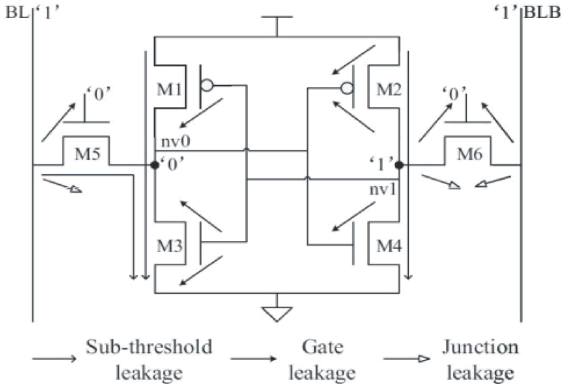

Fig. 2: Leakage current in 6T SRAM cell

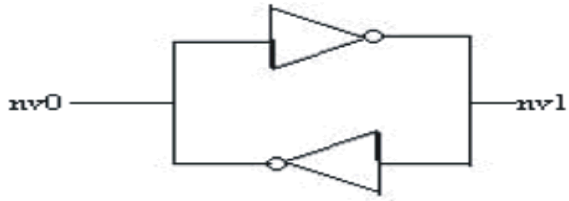

Fig. 3: Alternative SRAM

through the reverse biased diodes when a transistor is OFF. It is an exponential function of doping concentration and reverse biasing voltage across the junction. Third, Gate induce drain leakage current (I_{GIDL}) which is due to high field effect in the Drain junction of a MOS transistor Both I_{GIDL} and I_j also decrease dramatically with $+V_{DD}$ and fourth is the sub threshold leakage current (I_{SUB}), the Sub threshold leakage current (I_{SUB}) is produced when to the gate sources voltage (V_{GS}) is lower than Threshold voltage(V_T). V_{DD} scaling can effectively reduce the total cell leakage current and the Sub threshold Leakage Current (I_{SUB}) due to Low Threshold voltage (Vt). All leakage currents are indicated in Fig 2.

A Sub Threshold Leakage Current: Sub threshold leakage current is the drain-source current of a transistor when the gate-source voltage is lower than the threshold voltage i.e. weak inversion mode and it is mainly composed of diffusion current [2]. It is observed that for sub threshold leakage power reduction, optimal transistor sizing is essential. Another important consideration is transistor threshold voltage. With successive technologies, Vdd is being uniformly scaled down. The transistor delay is inversely proportional to the difference of supply and threshold voltage [3], Vt must be scaled down proportionally with each technology node to maintain circuit performance. This leads to exponential increase in sub threshold leakage current. This component of leakage current is dominant factor among the three leakage components. For SRAM cell shown in Figure 2, the two dominant sub threshold leakage paths are:

- V_{DD} to the ground.
- Bit lines to the ground, through access transistors M5 and M6

When the node nv0 stores '0', there is significant sub threshold leakage current through the off-transistors M1, M4 and access transistor M5, whereas, that of M6 is negligible, because its source-drain voltage difference is zero. When both pass transistor are OFF, then the 6T-SRAM cell is reduced then the same circuit acts as a flip-flop. The flip-flop representation of 6T SRAM cell is shown in Fig 3.

Leakage Reduction Techniques: Extensive work on techniques to reduce leakage power of SRAM cells and the memory peripheral circuits has been done at different levels. The leakage of the peripheral circuits can be effectively suppressed by turning off the leakage paths with switched source impedance (SSI) during idle period. Our work focuses on the leakage control of 6T-structure SRAM core cell of Fig. 2 during the standby mode. Following are the existing SRAM cell leakage reduction techniques.

- Novel SRAM cell design.
- Dynamic-biasing
- The V_{DD}-gating techniques

Novel SRAM cell design: When the supply voltage (V_{DD}) scales down in each new technology generation, in recent years several new SRAM cell designs were proposed with a reduced leakage power. A 10-T SRAM cell in CMOS technology improves the read margin by buffering the stored data during a read access and enhances the write margin with a floating VDD during write operation [16]. The improved operation margins allow this cell to operate at a V_{DD} lower than 400mV. Memory operations at such a low voltage effectively reduce both the active and standby power. In another work, a 4-T FinFET-based SRAM cell used back-gated feedback design to boost the static noise margin (SNM) and reduce cell leakage [17].

In contrast to these approaches, this work focuses on improving the conventional 6-Tstructure CMOS SRAM cell for ultra-low power standby operation.

In dynamic biasing scheme, dynamic control is used on transistor gate-source and substrate- source bias so that during stand by period, the driving strength of active operations is enhanced low leakage path is created.

For 130nm and 90nm technologies, this technique can be used to achieve reduction in leakage power by 5-7X but as the technology scales down, short channel effects become more prominent and cause reverse body bias effect on leakage suppression to diminish [9]. This technique when integrated with other low power design techniques can be used to achieve sustainable and higher (30X) leakage power reduction.

The V_{DD}-gating techniques either gate-off the supply voltage of idle memory sections, or put less frequently used sections into a low-voltage standby mode. There are three types of leakage mechanisms in an SRAM cell: sub-threshold

Leakage, gate leakage and junction leakage. A lower V_{DD} reduces all of these leakages effectively. The reduction ratio in leakage power is even higher because both the supply voltage and leakage current are reduced. In recent years as the need of leakage reduction in high-utilization memory structures increases, there have been many research activities on low voltage SRAM standby techniques.

Although the available techniques can be very effective in enhancing the efficiency of low-voltage memory standby operation, an important parameter needed by all of these schemes is the value of SRAM standby V_{DD}. This is because a high standby V_{DD} preserves memory data but produces high leakage current and a very low standby V_{DD} effectively reduces leakage power but does not guarantee a reliable data retention. An optimal standby V_{DD} is needed to maximize the leakage power saving and satisfy the data preservation requirement at the same time. This will be the main focus of our work.

In a typical 6T - SRAM design, the bit line voltages are connected to V_{DD} during standby mode. This cell can be represented by a flip-flop comprised of two inverters. These inverters include access transistors M5 and M6. When V_{DD} is reduced to DRV during standby operation, all six transistors in the SRAM cell are in the sub-threshold region. Thus, the capability of SRAM data retention strongly depends on the sub-threshold current conduction behavior.

As the minimum V_{DD} required for data prevention, DRV of an SRAM cell is measure of its state-retention capability under very low voltage. In order to reliably preserve data in an SRAM cell, the cross coupled inverters must have a loop gain greater than one. When V_{DD} scales down to DRV, the VTC of the cross coupled inverters degrade to such a level that the loop gain reduces to one. If V_{DD} is reduced below the DRV, the inverter loop switches to the other biased state determined by the deteriorated inverter VTC curves and loses the capability to hold the stored data.

The circuit structure of a 6T SRAM cell is shown in Figure 2. In a typical SRAM design, the bit line voltages are connected to V_{DD} during standby mode. This cell can be represented by a flip-flop comprised of two inverters. These inverters include access transistors Q5 and Q6. When V_{DD} is reduced to DRV during standby operation, all six transistors in the SRAM cell are in the sub-threshold region. Thus, the capability of SRAM data retention strongly depends on the sub-threshold current conduction behavior.

RESULTS AND DISCUSSION

In this paper we have presented two finger technique to reduce leakage current in 6T SRAM cell. This is a layout technique in which a single transistor is split into a number of parallel transistors with the same width, but smaller channel lengths. This reduces gate resistance, improves noise and delay, however the drawback is that it increases source and drain side-wall capacitance. Fig. 4 shows layout of MultiFinger transistor.

A length of 0.2um is similar to having four transistors connected in parallel, each with a width of 10um and a length of 0.2um. The MOS is said to have 2 fingers. The fingering technique allows the designer to reduce the drain and source area and in turn to reduce the parasitic capacitance

DRV is a measure of state retention capability at very low voltage and data retention strongly depends on sub threshold current conduction behavior.

Table 1 shows the leakage currents in various terminals of MOS transistors used in 6T SRAM cell for single finger and double finger layout. It also shows the difference in leakage currents.

In this paper. We have compared the leakage currents in single and double finger latch for 28nm technology at V_{dd}= 1.5V. DRV for single finger latch is 1.5V under the calculated values of leakage currents while by the use of

Table 1: leakage currents in MOS transistors of 6t sram cell

MOS	Status	Current_ type_ device	Single finger latch	Double finger latch	Difference in leakage currents
M3	ON	i_drain_n1	5.24E-07	7.12E-07	-1.88E-07
		i_source_n1	5.22E-07	7.11E-07	-1.88E-07
		i_bulk_n1	-1.96E-09	-1.29E-09	-6.66E-10
M1	OFF	i_drain_n2	1.43E-09	5.37E-09	8.89E-10
		i_source_n2	2.58E-09	1.28E-09	1.31E-09
		i_bulk_n2	-3.43E-13	-1.09E-13	-2.34E-13
M2	ON	i_drain_p2	1.04E-06	7.46E-06	2.90E-07
		i_source_p2	1.03E-06	7.45E-06	2.89E-07
		i_bulk_p2	-1.64E-09	-8.53E-09	-7.83E-10
M4	OFF	i_drain_p1	2.80E-09	1.84E-09	9.60E-10
		i_source_p1	-1.03E-09	-2.93E-09	-7.36E-10
		i_bulk_p1	-3.81E-09	-2.12E-09	-1.69E-09
M5	OFF	i_drain_pg1	5.09E-07	5.13E-07	-4.17E-09
		i_source_pg1	5.07E-07	5.12E-07	-4.95E-09
		i_bulk_pg1	-1.95E-09	-1.18E-09	-7.65E-10
M6	OFF	i_drain_pg2	1.74E-09	9.29E-09	8.07E-10
		i_source_pg2	-1.74E-09	-9.29E-09	-8.07E-10
		i_bulk_pg2	-3.42E-09	-1.84E-09	-1.58E-09
			4.12E-06	3.93E-06	1.90E-07

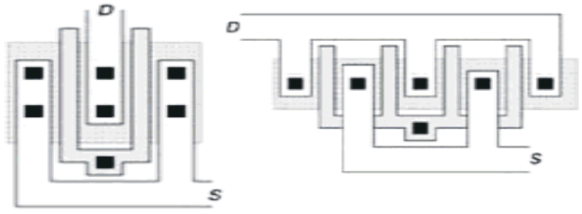

Fig. 4: Layout of multi finger transistor

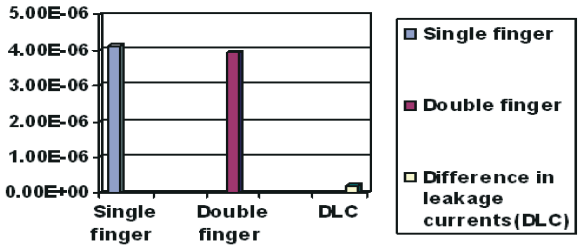

Fig. 5: Single finger vs. Double finger vs. Difference in leakage current (28 nm)

two finger layout, the total leakage of 6T SRAM cell is saved by 1.90E-07 and DRV is reduced to 1.43V therefore V_{dd} is reduced from 1.5v to 1.43v hence total 0.3V is saved when we are going to design one bit 6T SRAM by the use of two finger layout, while total resistance remains unchanged.

CONCLUSION

This paper presents leakage reduction technique of 6T- based SRAM, which are the critical issues in designing low power SRAM in deep sub-micron (DSM) technologies. Leakage currents in one bit 6T SRAM for single fingering method are 4.12E-06 and in double fingering method leakage current are 3.93E-06 therefore total leakage current saved in one 6T bit cell SRAM are 1.90E-07A by designing 6T one bit SRAM with help of double fingering method. When total sub threshold leakage current are saved 1.90E-07A by double fingering method for one bit 6T SRAM cell therefore , total saving of V_{dd} are 0.07V for one bit SRAM.

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