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Design of an Efficient Reversible 8x8 Wallace Tree Multiplier

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Abstract: Reversible logic gates provide power optimization which can be used in low power CMOS design, optical computing, quantum computing and nanotechnology. This paper proposes a Novel reversible 4:2 compressor, 6:2 compressor and 9:2 compressor designed from the DKGP gate that can work singly as a reversible full adder/full subtractor. These are later used to design a novel 8x8 reversible Wallace tree multiplier. This is the first attempt to design a reversible 6:2 and 9:2 compressors and a reversible Wallace tree multiplier using the above said circuits as far as our knowledge is concerned. Thus, this paper provides a threshold to build more complex systems using reversible logic.

Key words: Multipliers · Low power CMOS · Reversible logic · Reversible gates

INTRODUCTION

The synthesis of reversible logic circuits has been the main area of research in recent years. Reversible circuits are of high interest in the field of low power CMOS design, optical computing, quantum computing and nanotechnology. With increasing complexity of CMOS VLSI circuits, Power dissipation has become the main area of concern in VLSI design. It has been demonstrated by Landauer [1961] that circuits and systems constructed using irreversible logic will result in power consumption and energy dissipation due to information loss [1]. It is proved that the loss of one bit of information dissipates kT*log2 joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which computation is performed [1]. Bennett [1973] showed that zero power dissipation in logic circuits is possible only if a circuit is composed of reversible logic gates since the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation [2]. The state of the output prior to and during present output transition must be known to perform a non-dissipative transition of the output. That is the copy of the state of the output must be present at all times which can be obtained by using reversible logic. The circuit constructed using Reversible logic does not erase or lose information. Reversible computation in a system can be performed only when the system comprises of reversible gates. The field of quantum computing also uses reversible logic. All quantum gates are reversible [3]. The number of output bits is relatively small compared to that of input bits in many computing tasks. All of the information encoded in the input must be preserved at the output in computational tasks such as digital signal processing, communication, computer graphics and cryptography. Hence there are compelling reasons to consider circuits composed of reversible gates and the synthesis of such networks.

Reversible Logic: An n-input, n-output, totally specified Boolean function is reversible if it is a bijection, that is; each input pattern is mapped to a unique output pattern. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered back from the outputs. A balanced reversible function has half of minterms with value 1 and other half with value 0. In an n-output reversible gate the output vectors are

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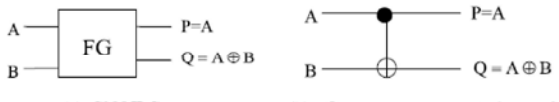
permutation of the numbers 0 to 2n-1. The input that is added to an nxk function to make it reversible is called constant input (CI). Garbage outputs (GO) are the outputs of the reversible circuit that are not used in the circuit except to preserve its reversibility. Number of garbage outputs for a particular reversible gate is not fixed, but any output that is not used in a circuit in which the gate is used is labeled garbage outputs. Quantum cost (QC) refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit [4]. These parameters have to be reduced while designing a reversible circuit. Some of the major problems with reversible logic synthesis are that fanouts cannot be used and also feedback from gate outputs to inputs is not permitted. However fanout in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates.

Reversible circuits have been proposed for different purposes like half adder, full adder, multipliers and dividers. Multiplier circuits are most important of all because they are the integral components of every processing system. It is important for every processor to have a high speed multiplier. Several 4x4 reversible gates (e.g. HNG [5], MKG [6], TSG [7] and PFAG [8]) have been used in reversible multipliers which are designed to work as full adder.

In this paper, a novel reversible 4:2 compressor, 6:2 compressor and 9:2 compressor are designed from the DKGP gate which can work singly as a reversible full adder and a full subtractor. Furthermore, the adder, 4:2 compressor and 6:2 compressor are used to design the novel 8x8 reversible Wallace tree multiplier. It is proved that multiplier architecture proposed is better than its counterpart existing in literature, in terms of number of reversible gates and garbage outputs. This is the first attempt to design a reversible Wallace tree multiplier using a reversible 6:2 compressor as far as existing literature and our knowledge is concerned. The proposed 9:2 compressor can be used to design higher order multipliers.

Literature Survey

Reversible Gates: Some major reversible gates required for this study are Feynman gate (FG) [9], Toffoli gate (TG) [10], Fredkin gate (FRG) [11], Peres gate (PG) [12] and BVF gate [13]. Quantum cost of FG, TG, FRG, PG and BVF gates are 1, 5, 5, 4 and, 2 respectively. The reversible gates and their quantum circuits are shown in Fig. 1.

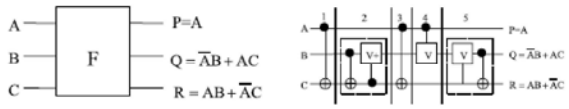


(a) CNOT Gate (b) Quantum representation of CNOT Gate

Fig. 1a: Feynman (FG) gate [9]

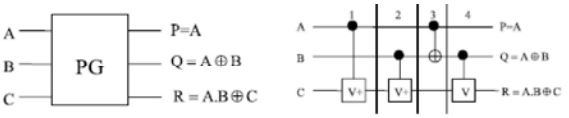
(a) Toffoli Gate (b) Quantum implementation of Toffoli Gate

Fig. 1b: Toffoli (TG) gate [10]



(a) Fredkin Gate (b) Delay of Fredkin Gate

Fig. 1c: Fredkin (FRG) gate [11]



(a) Peres Gate (b) Quantum implementation of Peres Gate

Fig. 1d: Peres (PG) gate [12]

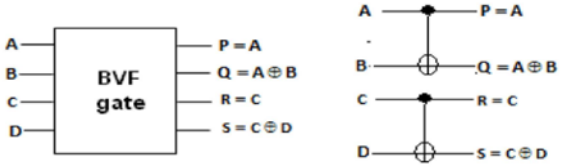


Fig. 1e: BVF gate [13]

Existing Reversible Wallace Tree Multiplier: The existing design for 8X8 Wallace tree multiplier [7] uses TSG gate as full adder and 4:2 compressor designed from TSG gates. The total number of reversible gates used is 61 (number of TSG gates=14, 4:2 compressors=17, parallel adder=1 containing 13 TSG gates) and the number of garbage outputs produced from this design is 122. A total of 75 constant inputs are given. As the partial product generation is done using Fredkin gates, 64 Fredkin gates are required. Fanout circuit is not given in the existing design. First stage of the multiplier contains 6 TSG gates and 12 4:2 compressors, thus a total of 30 gates are used. Second stage consists of 8 TSG gates and 5 4:2 compressors, contributing to 18 gates. Last stage is a parallel adder.

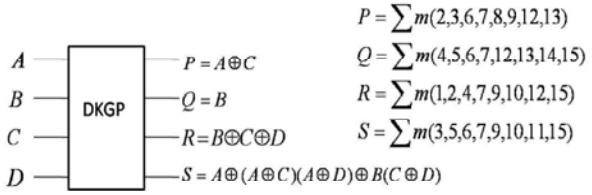


Fig. 2a: Reversible DKGP gate

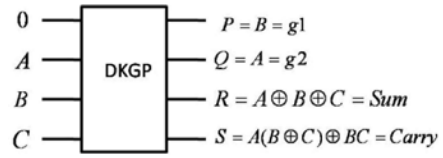


Fig. 2b: Reversible DKGP gate as Full adder

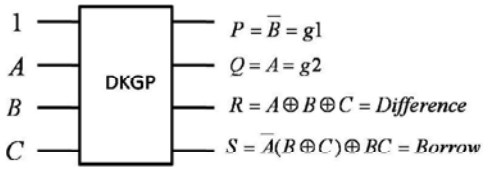


Fig. 2c: Reversible DKGP gate as Full subtractor

Proposed 4*4 Reversible Gate: A 4* 4 reversible DKGP gate can work singly as a reversible Full adder and a reversible Full subtractor and is shown in Fig. 2a. It can be verified that input pattern corresponding to a particular output pattern can be uniquely determined. Its implementation as a full adder and as a full subtractor is shown in Fig. 2b and 2c respectively. If input A=0, the proposed gate works as a reversible Full adder and if input A=1, then it works as a reversible Full subtractor.

The proposed reversible full adder/subtractor circuit produces two garbage outputs, so it is optimal in terms of number of garbage outputs.

Reversible 4:2 Compressor, 6:2 Compressor and 9:2 Compressor: In this paper, reversible 4:2 compressor, 6:2 compressor and 9:2 compressor using DKGP gates are proposed. The advantage of using higher order compressors is primarily speed improvement over conventional Full adder Wallace Tree realization. So 4:2, 6:2 or 9:2 compressors can be used for optimal design of a multiplier. The rows of partial product bits are reduced more rapidly as higher order compressors are used. Depending on the size of multiplier, an appropriate compressor is chosen. The compression ratio for a 3:2, 4:2, 6:2 and 9:2 compressor is 1.5, 2, 3 and 4.5 respectively.

The basic structure of 4:2 compressor, 6:2 compressor and 9:2 compressor is shown in Figure 3. The delay of basic 4:2, 6:2 and 9:2 compressor is 3 XOR gates, 5 XOR gates and 6 XOR gates in series, respectively.

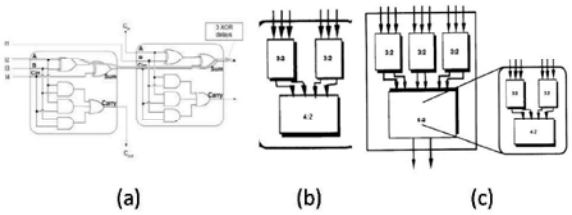


Fig. 3: Basic structure of (a) 4:2 Compressor (b) 6:2 Compressor (c) 9:2 Compressor

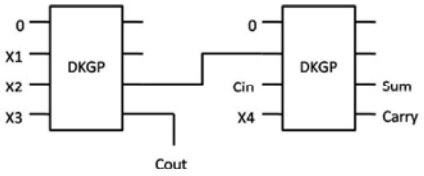


Fig. 4: Proposed Reversible 4:2 Compressor designed from DKGP gates

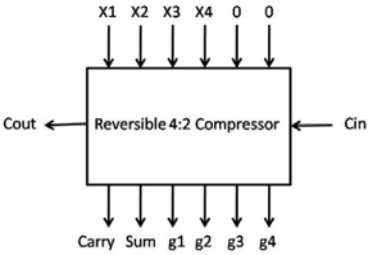


Fig. 5: Block diagram of Reversible 4:2 Compressor

The 4:2 compressor is designed by connecting the sum output of one full adder as an input to second full adder. Five inputs including carry in can be given to the 4:2 compressor and carry out, carry and sum are obtained as outputs. Carry out is given as carry input to next bit position while carry is passed on to the next level. Sum output is passed to the next level of addition in the same bit position. Thus, the four input bits which are given as input to the 4:2 compressor are compressed to two bits. The delay of 4:2 compressor is 3 XOR gates in series.

The reversible 4:2 compressor designed from two DKGP gates and its block diagram are shown in Figure 4 and 5 respectively.

The reversible 6:2 compressor designed from four DKGP gates and its block diagram are shown in Figure 6 and 7 respectively. The proposed 6:2 compressor compresses 7 partial product bits into three bits in which one of the inputs (carry in) is fed from neighbouring position j-1. The outputs of 6:2 compressor consists of one bit in position j, second bit in position j+1 and the third bit in position j+2. The proposed 6:2 compressor has a delay of 4 XOR gates as compared to 5 XOR gates for the basic structure.

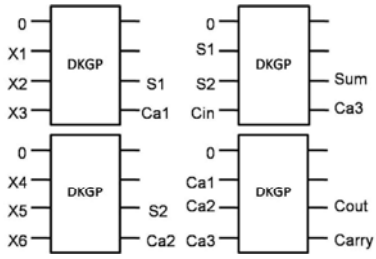


Fig. 6: Proposed Reversible 6:2 Compressor designed from DKGP gates

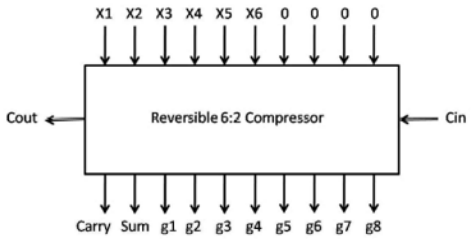


Fig. 7: Block diagram of Reversible 6:2 Compressor

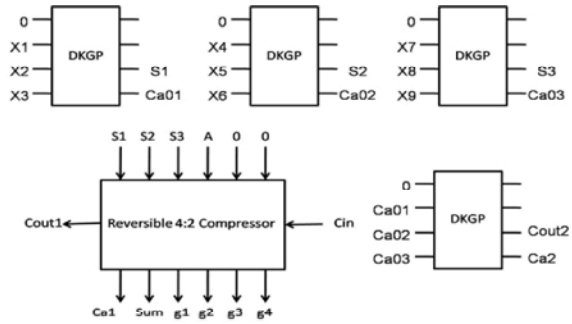


Fig. 8: Proposed Reversible 9:2 Compressor designed using DKGP gate

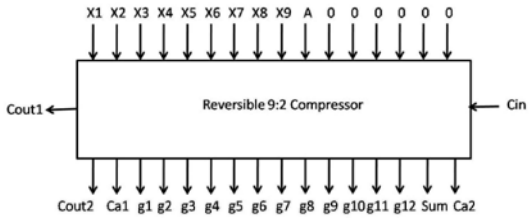


Fig. 9: Block diagram of Reversible 9:2 Compressor

The reversible 9:2 compressor designed from four DKGP gates and 4:2 compressor along with its block diagram, are shown in Figure 8 and 9 respectively. The proposed 9:2 compressor compresses 10 partial product bits into four bits in which one of the inputs (carry in) is fed from neighbouring position j-1. The output of 9:2 compressor consists of one bit in position j, two bits in position j+1 and one bit in position j+2. The proposed 9:2 compressor has a delay of 5 XOR gates as compared to 6 XOR gates for the basic structure. This is first attempt to design reversible 6:2 and 9:2 compressors.

The proposed 4:2 compressor, 6:2 compressor and 9:2 compressor can also be designed using the existing gates HNG [5], MKG [6], TSG [7], PFAG [8] and DPG [13].

Reversible 8x8 Wallace Tree Multiplier Using DKGP Gate: The three stages required to be performed for multiplication of two numbers are partial products generation stage, partial products addition stage and the final addition stage [14]. The second stage determines the overall speed of the multiplier. The Wallace tree multiplier makes use of carry save adders in a tree like fashion. As the critical path delay in a Wallace tree multiplier is proportional to the logarithm of the number of bits in the multiplier, it is faster than other multipliers.

Much less design effort would be needed if we use the same size compressors for every product bit position. This may use more hardware than is necessary, but it gives a much more regular layout and does not cost any extra time delay. We can use higher compressors at every bit position without increasing the worst case delay (the unneeded inputs would be set to 0) since all of the compressors are in parallel. This approach does take more area (probably about 30-50% at most).

Proposed Reversible Wallace Tree: The reversible full adder, 4:2 compressor and 6:2 compressor designed from reversible DKGP gate and half adders using PG gate [12] are used as the basic building blocks for the design of reversible 8x8 Wallace tree multiplier. The proposed architecture can be generalized for NXN bits. PG Gate is used as a half adder in the design as it has minimum quantum cost. Using PG gates, all partial products of the multiplication can be generated in parallel (the bits of the multiplier and multiplicand are ANDed) as shown in Figure 10a. Then the addition of partial products is performed using reversible Wallace tree.

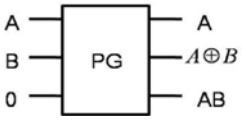


Fig. 10a: Use of PG gates to generate partial products in parallel

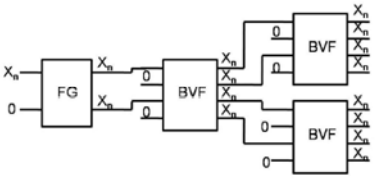


Fig. 10b: Fanout circuit to duplicate the operand bits using BVF gate

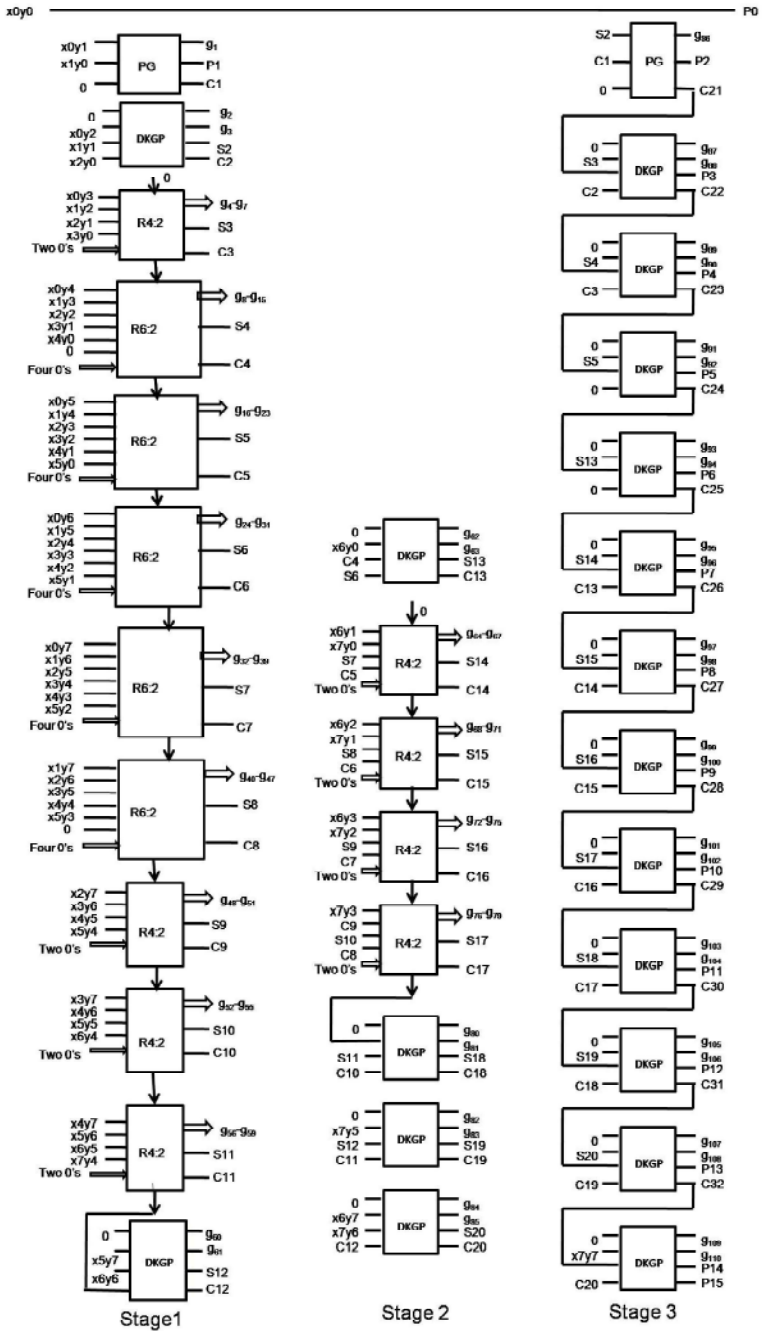


Fig. 11: Proposed Reversible 8X8 Wallace tree multiplier using Reversible 6:2 Compressor (R6:2), Reversible 4:2 Compressor (R4:2) and DKGP gates

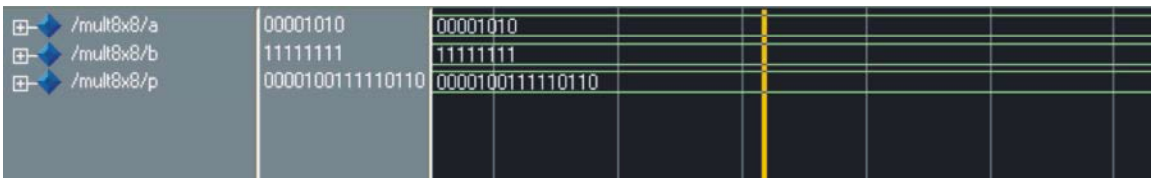


Fig. 12a: Simulation of Reversible Wallace tree 8 X 8 multiplier Design with inputs '11111111' and '00001010' and output '0000100111110110'

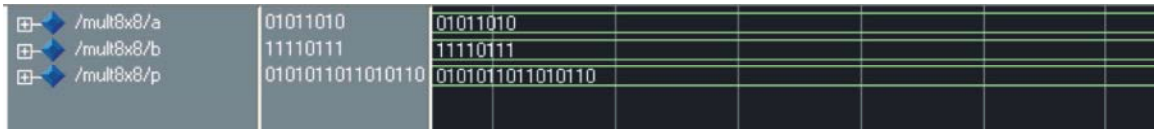


Fig. 12b: Simulation of Reversible Wallace tree 8 X 8 multiplier Design with inputs '11110111' and '01011010' and output '0101011011010110'

Table 1: Reversible Gates used in Level 1 of the 8 X 8 Wallace tree multiplier

	No. of half adders	No. of full adders	No. of 4:2 Compressors (=total gates)	No. of 6:2 Compressors (=total gates)	Total gates
Existing Design [7]	-	6 TSGs	12 (=24TSGs)	-	30
Proposed Design	1 PG	2 DKGPs	4 (=8 DKGPs)	5 (=20 DKGPs)	31

Table 2: Reversible Gates used in Level 2 of the 8 X 8 Wallace tree multiplier

	No. of half adders	No. of full adders	No. of 4:2 Compressors (=total gates)	No. of 6:2 Compressors (=total gates)	Total gates
Existing Design [7]	-	8 TSGs	5 (=10TSGs)	-	18
Proposed Design	-	4 DKGPs	4 (=8 DKGPs)	-	12

Table 3: Reversible Gates used in Level 3 (parallel adder) of the 8 X 8 Wallace tree multiplier

	No. of half adders	No. of full adders	No. of 4:2 Compressors (=total gates)	No. of 6:2 Compressors (=total gates)	Total gates
Existing Design [7]	-	13 TSGs	-	-	13
Proposed Design	1 PG	12 DKGPs	-	-	13

Table 4: A comparison of 8x8 Wallace tree multiplier with the existing circuit*

	No of Reversible Gates	No of Garbage Outputs (GO)	Number of Constant Inputs (CI)	Delay
Proposed Circuit	56	110	62	28 XOR+3 AND
Existing Circuit [7]	61	122	75	31 XOR+2 AND

* Numbers calculated excluding partial product generation

Table 5: Partial Product Generation

	No of Reversible Gates	No of Garbage Outputs (GO)	Number of Constant Inputs (CI)
Proposed Circuit	128 (PG & BVF gates)	128	176
Existing Circuit [7]	176 (FRG & FG gates)	128	176

Figure 11 shows the proposed reversible 8x8 Wallace tree multiplier in which (R4:2) represents reversible 4:2 compressor and (R6:2) represents reversible 6:2 compressor. In Stage 1, the partial products are added using 6:2 compressors, 4:2 compressors, full adders and half adders. In the Stage 2, the reduced partial products are again added using 4:2 compressors, full adders and half adders. The result obtained in Stage 2 is finally added using a parallel adder designed from DKGP gates to generate the product bits P0…P14, P15.

The proposed design of 8*8 multiplier circuit in reversible logic requires 8 copies of each operand bit. The fanout circuit is as shown in Fig. 10b. It uses 4*4 BVF gates with two constant inputs [13]. 48 BVF gates and 16 FG gates are used to obtain 8 copies of each operand bit (a total of 16 bits: x_7-x_0, y_7-y_0). Partial products can be generated in parallel using 64 PG gates and the fanout circuit requires a total of 64 gates. Thus partial product generation uses a total of 128 gates.

Evaluation of the Proposed Reversible 8X8 Wallace Tree Multiplier: This paper proposes a new reversible 4*4 DKGP gate that works singly as a full adder/ subtractor and is used along with 4:2 compressor, 6:2 compressor blocks to design the novel reversible 8X8 Wallace tree multiplier. The proposed 9:2 compressor can also be used in the design of larger multiplier circuits to reduce the delay. Similarly, higher order compressors can be implemented for designing larger reversible systems to increase the speed of the circuit.

Fig. 12 displays the results obtained during simulation of the Wallace tree multiplier using VHDL language and Xilinx and modelsim softwares. Fig. 12a and 12b shows the results for multiplication of inputs '11111111' and '00001010' and inputs '11110111' and '01011010' respectively.

The comparison of the proposed design with the existing design [7] at each level of the Wallace tree multiplier is given in the Tables 1, 2, 3, 4 and 5.

Important parameters to be reduced in the design of a reversible logic circuit are the number of constant inputs, reversible gates used, garbage outputs and critical path delay.

Table 4 gives the comparison of the proposed circuit with the existing circuit in terms of the number of constant inputs, reversible gates used, garbage outputs and critical path delay. It is seen that as the size of the multiplier increases, the critical path delay of the multiplier in terms of XOR and AND gates reduces if 4:2, 6:2 and 9:2 compressors are used in the design. Table 5 gives the comparative study of the partial product. It is seen that the proposed design is optimal in terms of the number of constant inputs, reversible gates used, critical path delay and garbage outputs.

CONCLUSION

This paper proposes a new reversible 4*4 DKGP gate using which 4:2 compressor and a 6:2 compressor are designed. Further, a 9:2 compressor and a Reversible 8x8 Wallace tree multiplier are also been designed. It also proposes multiplier architecture with the number of reversible gates, constant inputs the garbage outputs and critical path delay reduced to a significant amount. It reduces the size of the circuit and also gives significant power savings. The reversible multiplier and compressors discussed in this paper can be used to build higher order multipliers and complex designs of quantum computers.

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