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A Master-Slave Flip Flop for Low Voltage Systems with Improved Power-Delay Product

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Abstract: The paper presents a new static master-slave flip flop configuration based on a regenerative feedback loop strategy using a single clocked pass transistor. The proposed flip flop is realized using only eleven transistors (including an inverter to produce complementary clock signals locally). Simulations are performed using SPICE 180nm/1.8V CMOS technology BSIM 3v3 parameters and the results indicate at least 16% improvement in the power delay product with respect to the conventional designs at 250MHz. Scaled power supply voltages are used demonstrate the flip flop behavior at low voltages. The flip flop is particularly suitable for microcontrollers, microprocessors and standard cell library development.

Key words: Flip flops · Low voltage · Power-delay product · VLSI

INTRODUCTION

Due to increasing demand of battery operated portable handheld electronic devices like laptops, palmtops and wireless communication systems (personal digital assistants and personal communicators) the focus of the VLSI industry has been shifted towards low power and high performance circuits. The ultimate goal of VLSI designers these days is towards achieving the best possible trade-off between power and delay for a circuit while maintaining high density on the chip to reduce the overall cost of manufacturing.

Flip-flops and latches are the basic sequential components used for realizing digital systems. D-flip flop, is a fundamental circuit block in digital logic circuits. The flip-flops used in digital systems can be either dynamic or static based on their functionality when the clock is stopped/grounded, but the power is maintained. Dynamic flip-flops rely on charge storage at transistor node capacitances and can produce faulty logic levels when clock is grounded (due to charge leakage effects).On the other hand, static flip flops maintain the logic levels at the output when the clock is stopped and power is maintained [1].

From a low power perspective, flip-flops are clocked at the system operating frequency and consume a large amount of power, about 30%-70% of the total power dissipation in the system which also includes the power dissipated in the clocking network [2]. Thus reducing the power dissipation of latches and flip-flops is a prime concern for the total chip power conservation. The maximum speed at which synchronous systems can operate is determined by flip-flops since they are the starting and ending points of signal delay paths [3].

Several significant contributions have been made in the past for realizing low power and high performance master slave flip-flop designs. Transmission gate master slave flip flop (TGMSFF) embedded in Power PC-603 utilized two transmission gate latches and two feedback loops which made the design robust with respect to noise [4]. C^2MOS based flip flop employed clocked invertors as latches and reduced the overall delay by using feedback loops outside the D-Q path [5]. Pass transistor logic based flip flop used NMOS pass transistors as latches instead of transmission gates in an attempt to reduce transistor count and clock load [6].

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The previous designs consumed large area on the chip due to high transistor count thus trading off high chip density and hence manufacturing cost for either power or speed. A need ultimately arises for a static master slave flip-flop circuit configuration which is optimized with respect to power, performance as well as area overhead. In this paper, a new fully static master slave flip-flop circuit design is proposed. The flip flop is realized with only eleven transistors (including an inverter to produce complementary clock signals locally). The proposed flip-flop is compared in terms of power-delay product with the previously proposed [4-6] static flip-flop configurations which are highly utilized in the digital systems for low power and high performance applications.

The remaining paper is organized as follows. Section II states the standard power and performance metrics used for the analysis and comparison of designs. Section III outlines the previously proposed flip flops investigated in this paper along with a description of the proposed design. Section IV describes the simulation test bench, optimization techniques and the parameters used for simulation. Section V illustrates the simulation results. Finally, the discussion and conclusions are summarized in Section VI.

Standard Power and Performance Metrics

Power Characterization: The dynamic power consumption (P_D) in a circuit is estimated as

$$P_D = C * V^2_{DD} * f \text{ [3], [7]}$$

Where

C Load capacitance;
V_{DD} Power supply voltage;
f Operating frequency.

The switching activities at various nodes of the circuit determine its dynamic power dissipation which depends on the circuit configuration/structure and the statistics of the applied data. Thus, different data patterns at different clock frequencies comprising the best and the worst cases provide a fair idea about the power consumption of the circuit and can also determine the range of power consumption for a particular flip-flop design at different switching probabilities [8]. Most of the previously proposed flip-flops analyzed the designs with respect to only internal power dissipation, whereas Stojanovic&Oklobdzija proposed [9] that the total power dissipation is composed of the following three components:

Local data power dissipation represents the power dissipated in the inverter driving the data input of the flip flop.

Local Clock Power Dissipation: represents the power consumption of the inverter driving the clock input of the flip flop.

Internal Power Dissipation: Includes the intrinsic power dissipated on switching of the internal nodes of the flip-flop excluding the load capacitance.

The flip-flops were simulated and analyzed for total power consumption in our simulations (including all the three components) under different data activity rates. All the results were conducted for 16 clock cycle long data sequences.

Timing Characterization: The single edge triggered flip-flops can be either positive edge triggered or negative edge triggered depending on whether they operate on rising or falling edge of the clock. Moreover, for correct flip-flop operation the input logic level has to be maintained constant just before (T_{set-up}) and just after (T_{hold}) the triggering edge of the clock. T_{cq} is the propagation delay from the occurrence of the triggering clock edge to a change in the output logic level. Yet another parameter is D-Q delay or ($T_{set-up} + T_{cq}$) which determines the minimum clock time period for master–slave structures. Stojanovic&Oklobdzija [9] showed that D-Q delay is the real performance factor and not CLK-Q delay alone because D-Q delay also takes into account optimum set-up time which is positive for master–slave flip-flop structures. As $T_{d\text{-}clk}$delay (the time difference between the last transition of data and the triggering clock edge) decreases, at a certain point CLK-Q delay starts to increase monotonously and leads to failure. This results in metastability. For our analysis, we have chosen D-Q delay as the delay parameter of the flip-flops.

Power-Delay Product: In VLSI, there is always a trade-off between power and performance. A flip-flop can be optimized for either high performance or low power but

both the parameters are critical, so generally we want power–delay product to be minimum, which means that the flip-flop operates at optimum energy under a given frequency. Several metrics are available for comparative analysis of digital circuits. PDP (power-delay product) based metric is generally used for low power portable systems where battery life is the prime concern. In contrast EDP (energy delay product) or ED^2P are used for high performance systems [10], [11]. In this paper, we have taken total power (P_{Total}) as the power metric and D-Q delay as the performance metric. We have simulated the designs so as to achieve minimum P_{Total} and D-Q delay product PDP_{dq}.

Additionally, transistor count and total transistor widths are also included to increase the level of characterization for comparative study of all the flip flops in the paper.

Previous Designs: The TGMSFF flip-flop shown in Figure 1 was used in Power PC-603 microprocessor. The circuit basically is a Master-Slave flip–flop where CMOS transmission gates have been used as latches. When the clock signal is 'HIGH', the TG T1 in the master-section becomes functional and samples and transfers the input data at node D to an intermediate node X after one inversion. When the clock goes 'LOW', the TG T2 in the slave section becomes functional and transfers the data from node X to output node Q after one more inversion. Since there are exactly two inversions from input node D to the output node Q, the actual logic state at the input is preserved while it is transferred to the output at the triggering clock edge. The flip-flop is static in nature because loop L2 continuously restores the logic levels at the output when the clock is grounded.

The flip-flop shown in Figure 2 is composed mainly of C^2MOS latches in the Master and the Slave sections [5]. When the clock is 'HIGH' C^2MOS latch C1 transfers the data at input node D to an intermediate node M, while the C^2MOS latch C2 transfers the data from node M to the output node Q when the clock signal goes 'LOW'. There are two loops L3 and L4 which maintain the charge levels at nodes M and Q when clock goes HIGH and LOW respectively. The C^2MOS latches C3 and C4 in loops L3 & L4 are weak feedback latches with low driving capability. Again, the design is less sensitive to clock skew [12, 13] but suffers from area overhead (transistor count is twenty two including the inverter to produce complementary clock signals). The design does not show significant improvement with respect to power-delay product when compared to TGMSFF.

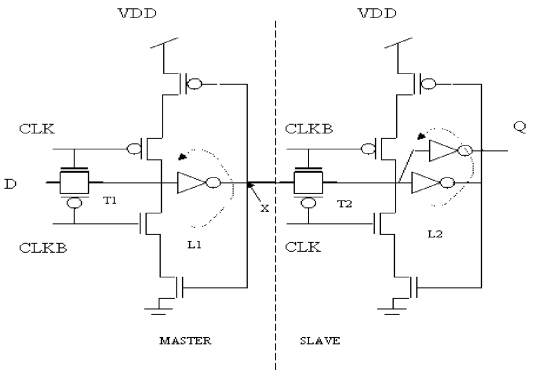

Fig. 1: TGMS based flip flop [4]

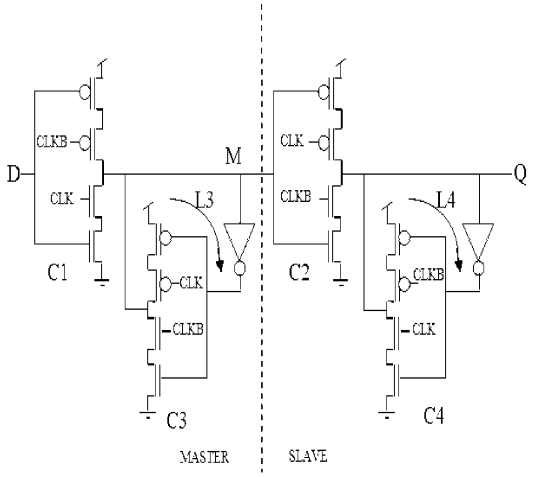

Fig. 2: C^2MOS based flip flop design [5]

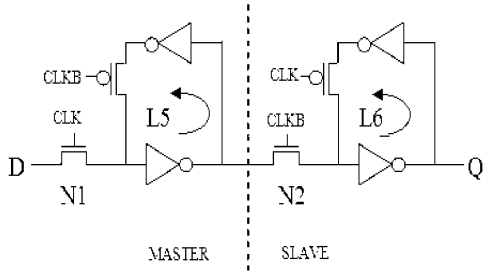

Fig. 3: Pass transistor logic based flip flop [6]

The flip-flop shown in Figure 3 utilizes NMOS switches (N1 and N2) as latches both in the Master and Slave sections which operate on complementary clock signals. There are two feedback loops L5 and L6 which become functional when the clock signal goes LOW & HIGH respectively and maintain the charge levels at internal flip-flop nodes thus maintaining the static nature of the flip-flop. This was an attempt to reduce the clock load and related power dissipation by using pass transistors instead of transmission gates.

The proposed design is shown in Figure 4. Its structure is based on master-slave configuration and the Master and the slave stages are clearly demarcated. The TGs T1 and T2 act as latches in the master and slave sections while inverted and non-inverted clock signals CLK and CLKB are generated locally by using an inverter INV3.

To make the flip-flop static in nature a feedback is provided from the output node to a specific internal node in the master-stage as shown in Figure. 4. This feedback is employed keeping in mind that there are exactly two inversions in the forward path. The feedback strategy used in our design is entirely different with respect to previous designs since the conventional static designs used two feedback loops one each in the master as well as the slave stage as demonstrated in previous implementations, which increased the total parasitic capacitance at the internal flip-flop nodes, leading to higher dynamic power dissipation and reduced performance. This also resulted in total chip area overhead due to increased transistor count.

The problem is eliminated in the proposed design by using a single switch (marked by a dot ·) for maintaining a regenerative feedback loop, which remains functional even when the clock is grounded to continuously restore the output of the flip-flop. The main advantage of using the proposed design is reduced device count and decreased parasitic capacitance at internal nodes of the flip flop which results in improved power-delay product and narrowing of the metastability window.

Originally , the feedback strategy was employed in static flip flops based on clocked invertors [8]. The whole idea was to reduce the transistor count and lower the power consumption, but some of the other important aspects like performance and low voltage operation of flip flops remained completely unexplored.

But using TGs in the critical path leads to highest performance and symmetrical delays unlike (3-T) clocked invertor based designs [8] which produce unsymmetrical H-L and L-H delays leading to glitches. This can further lead to unnecessary switching and enhanced power dissipation. Moreover, TG based flip flops display undeterred functionality even at much lower supply voltages due to higher driving capabilities when compared to pass transistors or clocked inverters. The operation at low voltages has been given due emphasis in this work.

Table 1: Cmos Simulation Parameters

0.18 um CMOS Technology		Clock	Data	
Min. Gate Width	2um	(1) Duty Cycle	50%	N/A
Max. Gate Width	22um	(2) Risetime	100ps	100ps
		(3) Falltime	100ps	100ps
MOSFET Model :				
BSIM 3v3 Level 53		(4) Frequency	250MHz	N/A
Nominal Conditions :				
Vdd =1.8V T=25°C		(5) Sequence Length	N/A	16 clock

Capacitive Load Cl (FO14) = 21fF cycles

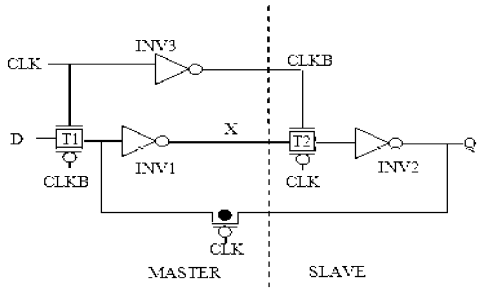

Fig. 4: Proposed Design

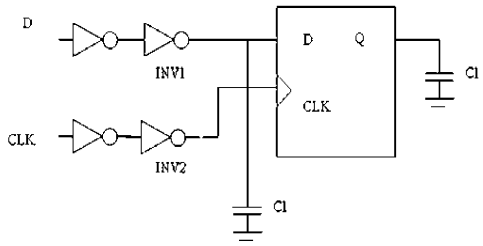

Fig. 5: The simulation test bench

Simulation

Testbench: Simulation parameters used for comparisons are depicted in Table 1. For this study, 180nm CMOS technology is used for obtaining the results. All simulations are performed at nominal conditions: V_{DD} =1.8V and at room temperature (25°C) except the supply voltage based analysis which demonstrates the power and performance of all the designs at lower supply voltages. The clock frequency is kept at 250 MHz.

The test bench for this study is illustrated in Figure 5. In order to obtain accurate results, buffering inverters are used to provide realistic clock and data signals. A fanout of fourteen minimum sized inverters (FO14) is used as the capacitance load at node Q. This capacitance load is estimated to be 21fF [14, 15]. A 16-cycle pseudorandom sequence with an activity factor of 18.75%is supplied at the input for average power measurements. As mentioned in the section on power characterization, the total power dissipation is composed of three components. They are estimated as follows:

- Local data power which represents the power dissipation in the inverter INV1 which drives the data input of the flip flop.
- Local clock power which represents the portion of power consumption in the inverter INV2 driving the clock input of the flip flop.
- Internal power consumption is the intrinsic power dissipated on switching the internal nodes of the circuit excluding the power dissipated on switching the output load capacitances Cl.

The flip flop under test is initially connected to the set up and the total power dissipation is measured. To compute the local data power and the local clock power the power dissipation in the inverters INV1 and INV2 is observed by disconnecting the flip flop from the initial set up. The flip flop is connected again and the power consumption of the inverters INV1 and INV2 is computed once again. Hence, the local data power dissipation is calculated as the difference of the two power consumption values of the inverter INV1. Similarly, the local clock power dissipation is estimated as the difference of the two power dissipations of the inverter INV2.

Optimization: The first step of the optimization is to identify the critical path. The widths of the transistors on the critical path are then optimized for the minimum T_{cq} and the total power using the Levenberg-Marquardt optimization algorithm embedded in SPICE to obtain PDP_{cq}. Moreover, the inverters and transistors in the feedback paths are kept at minimum widths to reduce area overhead. In the next step, minimum T_{dq} is replaced as the delay parameter which is the sum of T_{set-up} and T_{cq} and the flip flops are optimized for minimum PDP_{dq} using an iterative procedure. Once transistor widths are optimized for minimum PDP_{dq} , the optimum T_{set-up} is recorded at a point when T_{cq} delay increases by 5% of the constant value.

RESULTS

All the flip flops are optimized as explained earlier in Section IV. The optimal timing parameters are reported in Table 2. It is observed that the proposed design has 41.4% and 42.2 % increased performance than the conventional C^2MOS and PTL based flip flops respectively. The optimum set up time is 35.2% lower in case of the proposed flip flop when compared to the TGMSFF due to reduced parasitic capacitances at internal nodes. Since master slave structures have negative or zero hold time [12], set up time becomes the dominant parameter for minimizing the window of metastability. In comparison to the conventional designs the aperture of metastabilty is quite narrow in the proposed flip flop primarily because of the significantly reduced T_{set-up} requirements.

Table 2: Optimaltiming/performance Parameters

Cell	T_{cq}	T_{dq}	T_{set-up}
C^2MOS	225ps	413ps	175ps
PTL	222ps	419ps	198ps
TGMSFF	191ps	244ps	85ps
Proposed Design	200ps	242ps	55ps

Table 3 Optimal Power Parameters

Cell	Clock Power	Data Power	Internal Power	Total Power
C^2MOS	25uW	42uW	383uW	450uW
PTL	17uW	3uW	399uW	419uW
TGMSFF	20uW	37uW	367uW	424uW
Proposed Design	15uW	8uW	340uW	363uW

The optimal power results are summarized in Table 3 using a pseudorandom sequence at the data input for 16 clock cycles. The clock power depends on the clock load which is high in case of both the C^2MOS and the TGMSFF designs and hence increased clock power as indicated by the results. The clock power consumption is much lower in the proposed design since there are far less number of clocked transistors when compared to the previous designs. Moreover, PTL based flip flop has the highest internal power consumption although it has lesser clock and data power dissipation. The simulation results indicate that the proposed flip flop has the least total power dissipation among all the designs. Reduced transistor count and hence decreased parasitic capacitance at the internal nodes of the proposed design leads to at least 13.3% lesser power dissipation when compared to any of the conventional designs.

Table 4 illustrates the transistor count for the various flip flop designsdiscussed in this paper (excluding the inverter to generate the complementary clock signals locally). Our design is composed of only nine transistors and has the least transistor count among all the previously proposed static flip flops. This leads to lower manufacturing cost and high chip density due to lesser complexity overhead. It is further seen that C^2MOS and TGMSFF designs occupy larger silicon area when compared to PTL based flip flop and the proposed design in terms of total transistor width after all the designs have been optimized for minimum power delay products, PDP_{cq} and PDP_{dq}. Additionally normalized PDP_{dq} have been calculated to provide a fair idea about the relative

Table 4: Optimal Power Delay Products

Cell	Transistor count	Total Width	PDP_{eq}	PDP_{dq}	Normalized PDP_{dq}
C^2MOS	20	194.7um	101.25fJ	185.85fJ	1.79
PTL	14	146.3um	93.01fJ	175.56fJ	1.69
TGMSFF	18	178.1um	80.98fJ	103.45fJ	1.00
Proposed Design	09	147.3um	72.60fJ	87.84fJ	0.84

Table 5: Total Power vs Supply Voltage

Cell	1.8V	1.6V	1.4V	1.2V	1V	0.8V
C^2MOS	450uW	352uW	266uW	197uW	133uW	failed
PTL	419uW	297uW	220uW	failed	failed	failed
TGMSFF	424uW	334uW	254uW	187uW	129uW	failed
Proposed Design	363uW	287uW	219uW	161uW	110uW	71uW

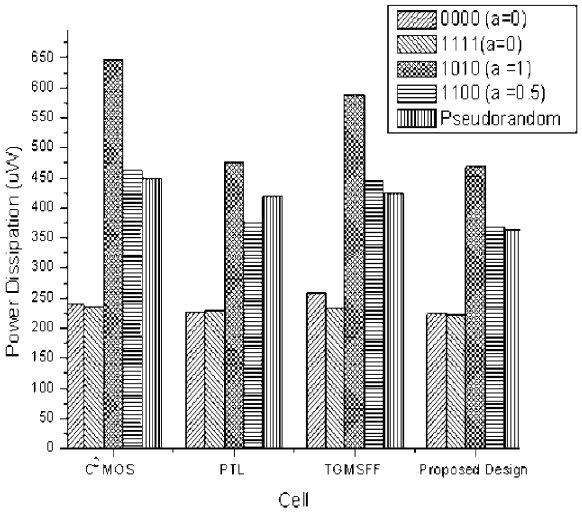

Fig. 6: Power consumption distribution as a function of data activity

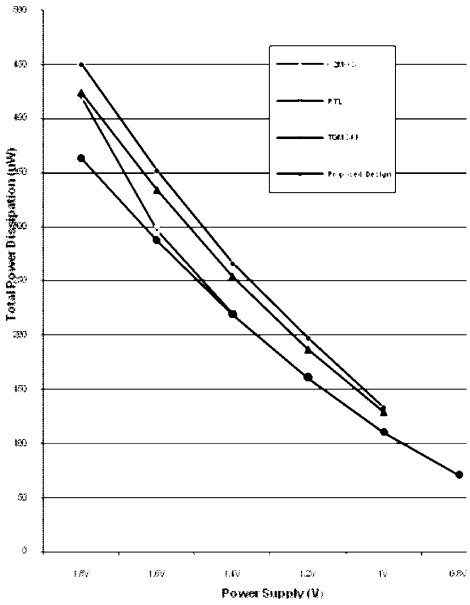

Fig. 7: Curves showing power dissipation valuesat scaled power supply voltages

improvement in the power delay product. The proposed design shows 16% improvement in the power delay product over TGMSFF which is one of the best conventional static master slave flip flops till date.

Figure 6 shows a comparison of the total power dissipation for the aforementioned flip flops with different switching probabilities of the input data. For each master slave configuration, the total power dissipation is directly proportional to the switching activity. This is supported by the simulation results. It can be observed that at higher switching probabilities (α =0.5 and α =1), the power consumption of the proposed flip flop is respectively 17.3% and 20.3% lesser than the TGMSFF which leads to further improvement in the overall PDP_{dq}. The power delay product PDP_{dq} for the proposed design improves to 17.98% at α =0.5 and 21% at α =1 compared to 16% at the pseudorandom data activity.

For low data activity (α =0), although the proposed design remains the finest alternative, the PTL based flip flop can also be considered as another low power consuming design option. At high switching probabilities, C^2MOS based flip flop has the highest power consumption.

The power supply voltage is considerably reduced for low power battery operated systems. Although the nominal power supply voltage used for simulations is 1.8V at 180nm technology, comparisons are carried out even at scaled power supply voltages (V_{DD} is scaled from 1.8V down to 0.8V). The simulation test bench is the same even for the lower voltages .Table 5 lists the various power consumption values and it is monotonously decreased at lower voltages for all the designs as illustrated in the curves in Figure 7. .It can be readily observed that PTL based design fails well before at 1.2V because of poor driving capability. Similarly C^2MOS and TGMSFF based designs fail to operate at or below 0.8V, since at lower power supply voltages the driving capability of the corresponding latches used in the master and slave

Table 6: Delay vs Supply Voltage

Cell	1.8V	1.6V	1.4V	1.2V	1V	0.8V
C^2MOS	413ps	477ps	577ps	637ps	1152ps	failed
PTL	419ps	632ps	1120ps	failed	failed	failed
TGMSFF	244ps	291ps	377ps	560ps	1082ps	failed
Proposed Design	242ps	285ps	345ps	468ps	755ps	1554ps

Table 7: PDP_{dq} Vs Power Supply Voltage

Cell	1.8V	1.6V	1.4V	1.2V	1V	0.8V
C^2MOS	185.85fJ	167.90fJ	153.48fJ	125.48fJ	153.32fJ	failed
PTL	175.56fJ	187.70fJ	246.40fJ	failed	failed	failed
TGFF	103.45fJ	97.19fJ	95.75fJ	104.72fJ	152.22fJ	failed
Proposed Design	87.84fJ	81.79fJ	77.52fJ	75.34fJ	82.72fJ	110.33fJ

portions of these flip flops is degraded and the parasitic capacitances at the internal nodes is relatively higher due to higher transistor count in low power feedbacks. However, the proposed design is able to function correctly even at 0.8V mainly due to the feedback technique which uses only one switch in the feedback path to maintain the static functionality and considerably reduces the capacitance at internal nodes of both the master and the slave sections when compared to all the conventional designs.

The overall delay T_{dq} delay variation is demonstrated in Table 6. The delay for all the designs monotonously increases when power supply is scaled from (1.8V down to 0.8V). The simulation results are in accordance with the expected behaviour in terms of delay as shown in the plot in Figure 8. It is to be noticed here that at 1V power supply the delay in the proposed design decreases significantly by 30.22 % when compared to TGMSFF. Thus the design becomes considerably more performance efficient at lower voltages.

The corresponding power delay products at scaled voltages are represented in Table 7.The simulation results indicate that the power delay products for the proposed flip flop shows a dramatic reduction of over 45.65% and 46.04% with respect to TGMSFF and C^2MOS based flip flop designs respectively when the power supply voltage is scaled to 1V. Furthermore, it can be noticed that PTL based designs show erroneous behaviour at or below 1.2V.

DISCUSSION AND CONCLUSION

In this paper a new design of static Master Slave flip flop configuration is proposed which is compared with various state of the art flip flops. The flip flops are investigated using the standard parameters, optimization techniques and extensive simulation procedures. The timing simulation results depict that PTL based design although has lesser device count than TGMSFF and C^2MOS configurations but it has the worst performance. In high performance systems $T_{set\text{-}up}$ contributes significantly in the determination of maximum frequency of operation. The proposed design has the lowest set up time requirements and hence suitable for systems with high performance and lower aperture of metastabilty. Moreover, the proposed design shows highest performance with least transistor count. From a power perspective, C^2MOS based flip flop has the highest total power consumption while PTL based flip flop consumes highest internal power. It is also observed that the sum of clock and data power is minimum for PTL based designs The proposed flip flop is the best design alternative for high performance low power systems since its power delay product PDP_{dq} is minimum. To maintain a fair level of comparisons, the flip flops are simulated for various switching activities apart from the pseudorandom sequence. The proposed design maintains lowest power dissipation at all switching activities. Despite the fact that the total power consumption of PTL based designs is considerably high at pseudorandom data sequences its power dissipation at lower switching probabilities is comparable to the proposed design and hence it is the second best option after the proposed design when data activity is low.

The designs are also simulated at scaled voltages. It is further noticed that although the power consumption reduces and delay increases monotonously for all the designs, the proposed design shows a relatively high improvement in performance and power delay products at lower supply voltages as shown by the results in Table 6 and Table 7respectively. Moreover the power delay products at 1V for both C^2MOS and TGMSFF based flip flops are almost twice that of the proposed design and hence the designs are not recommended for low voltage systems. Hence it is concluded that the proposed design is ideally suited for low power and high performance systems operating at low voltages.

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