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PCB Layout Design And Interfacing of 16-Bit 1-MSPS CMOS ADC to FPGA Based Signal Processing Card

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Abstract: The purpose of this paper is to describe the PCB layout design and interfacing of 16-bit 1-MSPS CMOS ADC to FPGA based signal processing card. An on board real time digital signal processing system is designed using FPGA, the architecture and the state-of-the art of the Field Programmable Gate Arrays (FPGAs) make it especially suitable to act as interface between an high speed ADC and a data processing unit [1]. PCB layout is the process of designing the template for manufacturing a PCB (Printed Circuit Board). The process consists of using a CAD program to connect tracks that represent connections between components on the final board. These connections have to be in accordance with the rules of the schematic capture files. When complete, the PCB files (Gerber) are used to manufacture the physical boards. When necessary, the process is repeated to ensure design requirements [2]. The schematic and routing is done using mentor graphics, the resultant PCB is a multi layered, having surface mount construction. For the optimum performance a 16 bit 1 MSPS ADC is interfaced with FPGA to make all the data processing onboard in real time [3]. The Virtex4-SX FPGAs offer designers a low cost and feature rich platform for interfacing with high speed Analog to Digital Converters (ADCs). The platform can decode process of various kinds of digital and analog signals simultaneously. Interfacing high speed ADCs can present several challenges to designers including: DDR to SDR Conversion, LVDS Buffers, Tight Timing Margins and High Data Rates.

Key words:

INTRODUCTION

As the need for data bandwidth increases for end systems, data transmission rates continue to increase for Analog to Digital Converters (ADC) and the associated FPGA solution to interface to the ADCs and other parts of the system. Manufacturers of ADCs and FPGAs have responded with faster, more capable devices at a lower cost [1]. In the context of signal processing, arbitrary binary data streams and on-off signals are not considered as signals, but only analog and digital signals that are representations of analog physical quantities. This card is tested for laser beam communication which requires very fastdata processing although it can also be used for a vast range of signal processing simultaneously. For that purpose a high speed system is being developed that not only delivers high performance, but also a high degree of flexibility that is not commercially available. To limit energy in a reasonable size battery, minimum power dissipation in the mixed-signal integrated circuits is necessary [3, 4, 5]. The analog-to-digital converter (ADC) is the key component because it bridges the gap between the analog physical world and digital logic world [6, 7]. The main concept is that by using A/D converter we can maintain the good energy and time resolution. We are using AD7671 ADC with 16-bit resolution, 1 MSPS, charge redistribution SAR, analog-to-digital converter that operates from a single 5 V power supply [4]. It contains a high speed 16-bit sampling ADC, a resistor input scalar that allows various input ranges, internal conversion clock, error correction circuits and both serial and parallel system interface ports [6]. The AD7671 has a maximum integral nonlinearity of 2.5 LSB with no missing 16-bit code. ADC output samples stored in 16 bit flash memory i.e. LHF00L28 IC. Flash memory used to store multiple samples which are coming from LASER beam

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through ADC. After the comparison of different samples the effective data pass through the DDS interface. FPGAs are replacing processors and their associated peripheral components in many new designs and applications for a variety of reasons but primarily because of their extreme-high performance and flexibility. This is particularly true now that FPGAs have integrated gigabit serial communications, memory interfaces, immersed processors and a wide range of available core firmware modules [6, 8].

Background of Adc

Fpga - Adc Connectivity: Digital Signal Processors Takes digital data from ADC (Analog-Digital Converter) and passes out data which is finally output by converting into analog by DAC (Digital-Analog Converter).

Analog input-->ADC-->DSP-->DAC-->analog output.

Digital signal processing is for signals that have been digitized. Here the processing is done by field programmable gate arrays. First the FPGA is initialized for all I/O peripherals, then analog data is applied to the ADC in the form of LASER beam, where it gets converted to digital form and stored in FLASH memory. This digital signal is then retrieved and processed by FPGA and synthesized by DDS interface, the o/p of this stage is processedanalog signal. This analog signal is then compared with the previous analog signal and is checked for noise removal. If the noise has been removed the signal is transferred to the display. If there is no change in the compared signal then it is again send for processing and synthesizing.

Architecture / Schematic Of ADC Created In Orcad Tools: Schematic capture is the process of drawing and electronic design on a computer. Generally the design exists on paper. Schematic capture is necessary as a preparation for PCB manufacture which requires PCB Layout. For successful PCB layout, the schematic capture has to be done as thorough as possible. Electronic knowledge is crucial, as well as knowledge of the final design requirements, component technology used, component sourcing, component footprints, target pricing and operation of the final product is necessary.

The basic specification of ADC7671 is describes as follows:

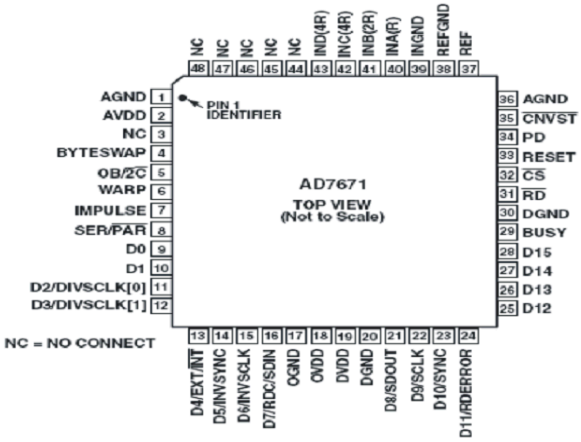


Fig. 1: Pin Configuration Of ADC

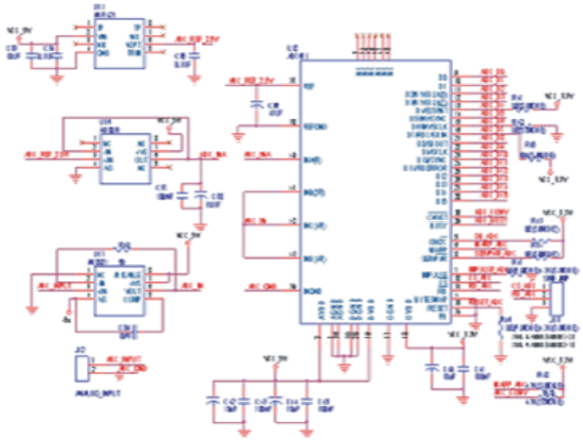


Fig. 2(a): Schematic Diagram Of ADC7671

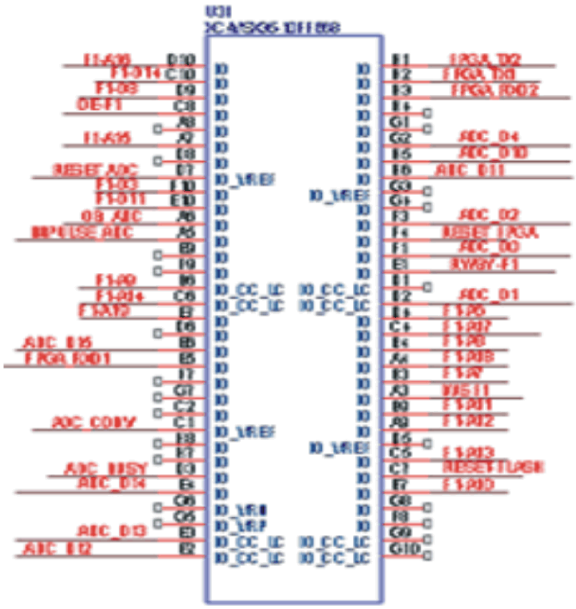


Fig. 2(b): Schematic of small part of virtex4-FPGA in which ADC is connencted

C. PCB Design steps

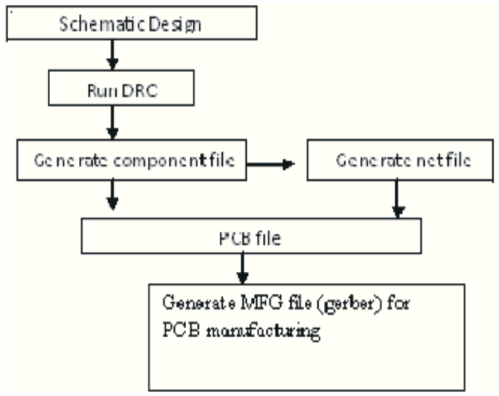


Fig. 3: PCB Design steps

Requirment of Other Components: This card is on board user programmable Xilinx virtex-4SX FPGA for signal processing functionSuch as channelization, modulation and error correction, with the data rates of 600 Mb/s HSTL and SSTL (on all single-ended I/O) and 1 Gb/s LVDS (on all differential I/O pairs). The card has a large number of high speed input output GPIOs, DDS interface and OLED interface that areconnected to FPGA through buffer. Data from ADC is received by dedicated DDS register, which enables high performance data receptions. FPGAs have integrated gigabit serial communications, memory interfaces, immersed processors and a wide range of available core firmware modules. Three software's are used to design this card i.e. ORCAD for designing the Schematic part, MENTOR GRAPHICS for the layout and Xilinx is used for VHDL coding. So after interfacing of ADC with FPGA some other component blocks are also required for signal processing.

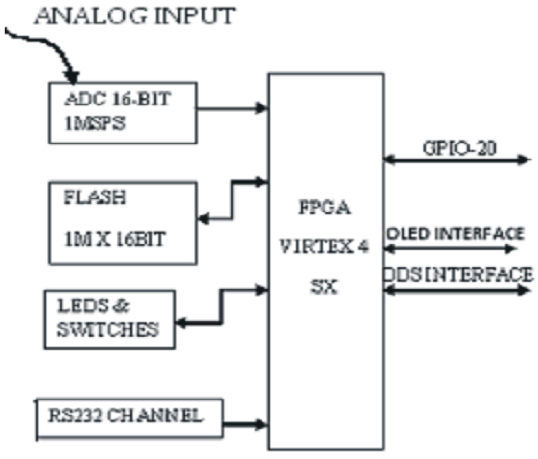


Fig. 4: Block diagram of signal processing card

Block diagram of signal processing card which is shown in Fig. The FPGA interfaced with I/O and other peripheral device. As far as our card specification is concerned:

- Area of the PCB - 70mX130m
- Execution time- 200ms
- Power consumption- 40mw

Input signal- various analog signals ranging from 10mv to 30mv as well as digital signals. Tested for LASER beams incident on a photo diode [3].

Outline Drawing of Fpga Based Signal Processing Card: There are total eight layers in the PCB whose layer wise description is given below: Layer1 (copper top): signal 1, Layer2 (copper inside): signal 2, Layer3 (copper inside): Power1 (Vcc +5V), Layer4(copper inside): Power2 (Vcc +1.2V), Layer5 (copper inside): Power3 (Vcc +3.5V), Layer6 (copper inside): Power4 (Vcc +2.5V), Layer7 (copper inside): signal3, Layer8 (copper bottom): Power (Gnd). There are some of the design protocols which are to be followed while placement and routing [9]. PROM Memory and Flash memory should be placed first and near to the FPGA and routed straight through the shortest path available. This reduces delay as well as noise in the channel. The crystal oscillator must be routed straight and close to the FPGA with a ground pad. Analog and Digital signal tracks should be away from Each other with a Ground track between them. This practice prevents the digital signal to be effected by the noise of analog signal. There must be separate Gnd signals for analog and digital signals and both the Gnd signals should be connected to each other with an inductor at the end.

A. Layer1 (copper top): signal TOP LAYER

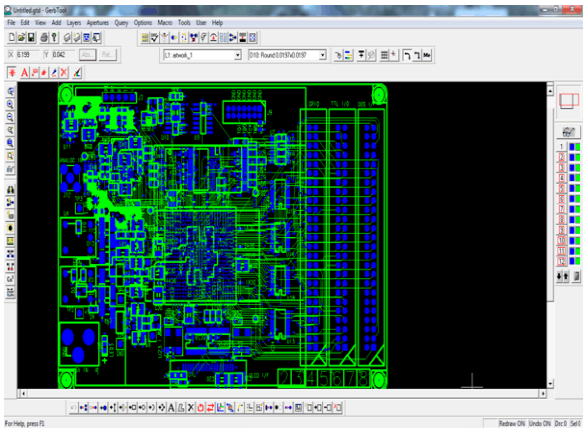


Fig. 5(a): Top Side of FPGA based signal processing Card,

B. Layer2 (copper inside): signal 2

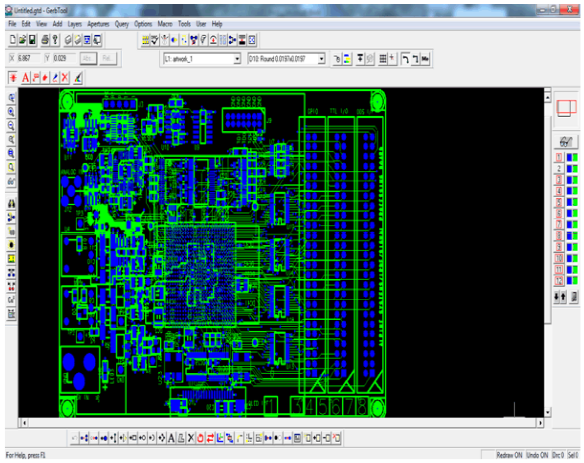


Fig. 5(b): Layer 2 of FPGA based signal processing Card,

C. Layer3 (copper inside): Power1

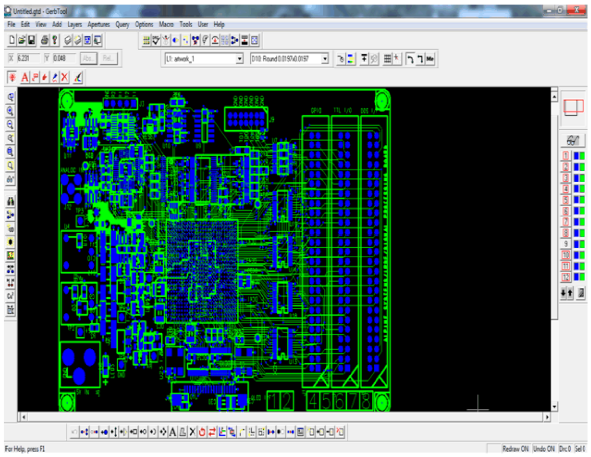


Fig. 5(c): Layer 3 of FPGA based signal processing Card,

D. Layer4(copper inside): Power2

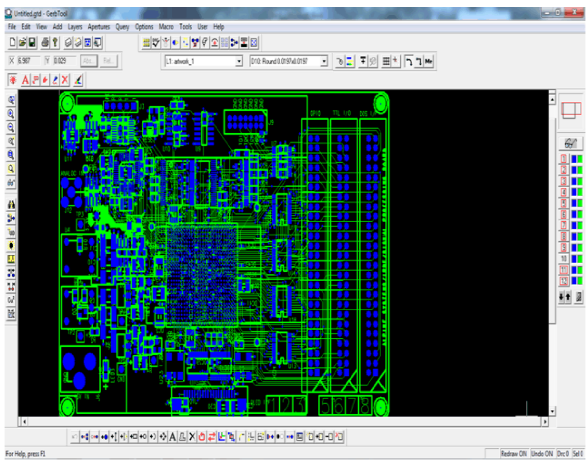


Fig. 5(d): Layer 4 of FPGA based signal processing Card,

E. Layer5 (copper inside): Power3

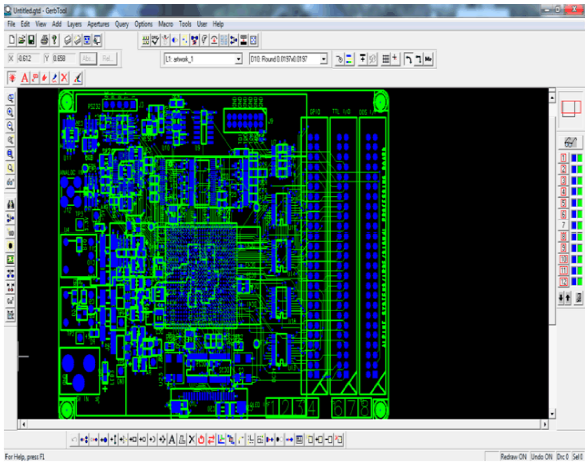


Fig. 5(e): Layer 5 of FPGA based signal processing Card,

F. Layer6 (copper inside): Power4

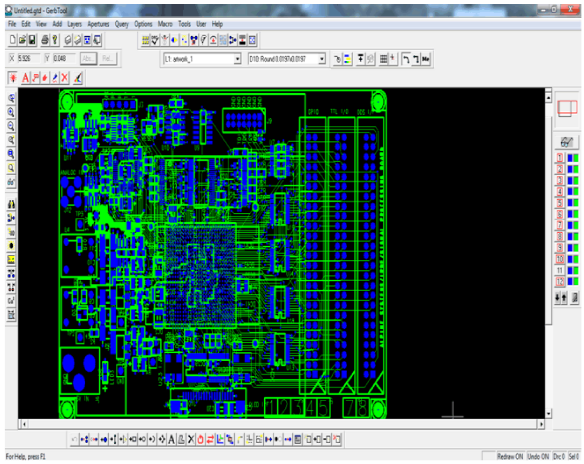


Fig. 5(f): Layer 6 of FPGA based signal processing Card,

G. Layer7 (copper inside): Signal3

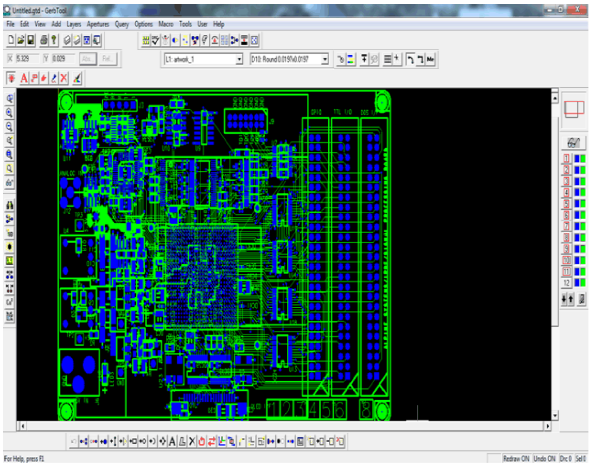


Fig. 5(g): Layer 7 of FPGA based signal processing Card,

H. Layer8 (copper bottom): Power (Gnd)

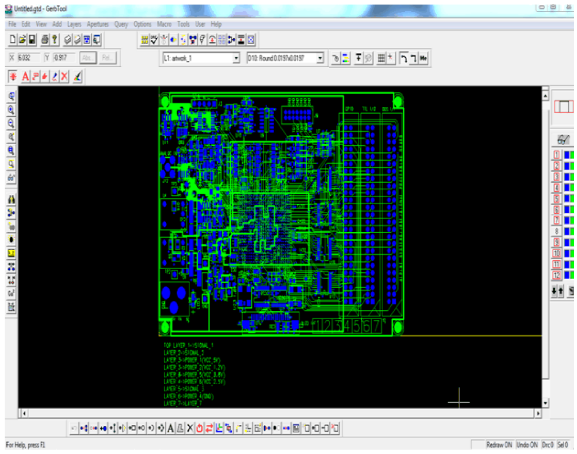


Fig. 5(h): Layer 8 of FPGA based signal processing Card,

Overall Working of Adc: The ADC7671 is capable of converting analog data into 16 bit words at sample rates up to 1MSPS. It has a separate 2.5 Volt power supply for the digital interface that allows low power operation with reduced noise. The ADC7671 also converts analog data into 16 bit words, but itoutputs the data on a single data line. It can be ordered in various speed ranges from 800 KSPS to 1 MSPS and it operates from a single 5v Volt power supply. ADC pins SCLK, BUSY, SDOUT are directly connected to the FPGA and CNVST pin of ADC is connected through a D latch to the FPGA. At power on during the initialization process CNVST should be brought LOW once to initiate the conversion process. The analog signal coming from the photo diode is made available to the input of ADC within range of +-10v. First the FPGA monitors the BUSY pin of the ADC, if it is LOW then the FPGA make the CNVST pin of ADC high to acquire the analog input data then after a specified delay the CNVST pin of ADC is made LOW to start the conversion, once the conversion is started the BUSY pin of ADC remains HIGH till the conversion is completed. Once the conversion is completed the BUSY pin becomes LOW and is monitored by the FPGA.

In this paper FPGA and some of high speed peripherals are used in LASER detection system for missile application and LASER based audio application, light sensors are used to detect the laser beam and the data is then processed and converted into suitable format to be used in various applications. Like light signals other signals can also be used simultaneously depending upon the need, this shows the processing of signal at a high speed. FPGA based platform is addressing the problems by allowing add-on cards to meet application-specific feature and performance requirements.

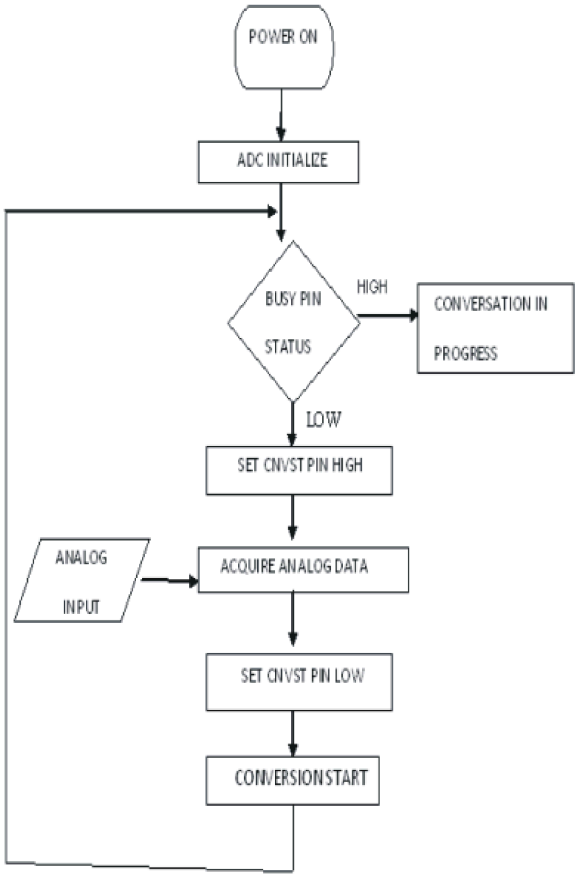
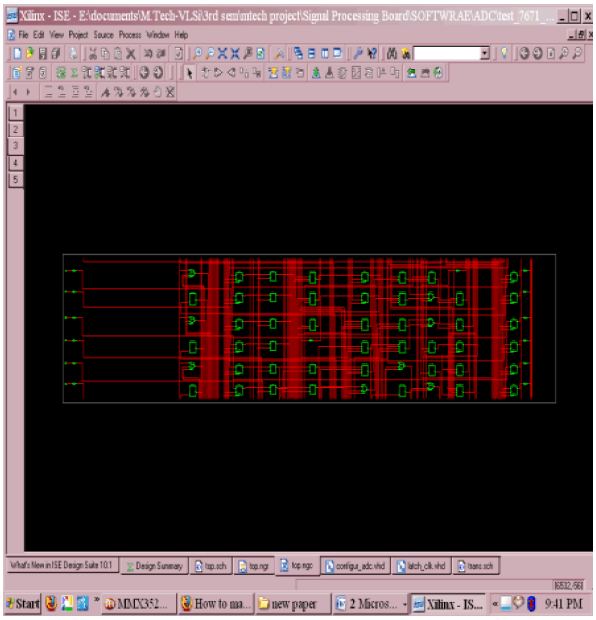
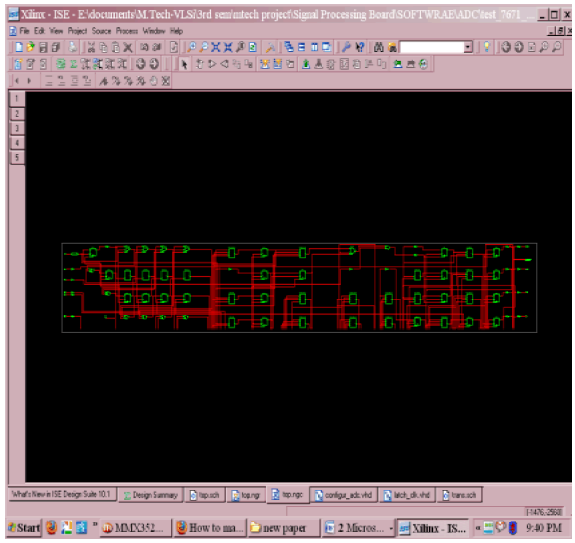
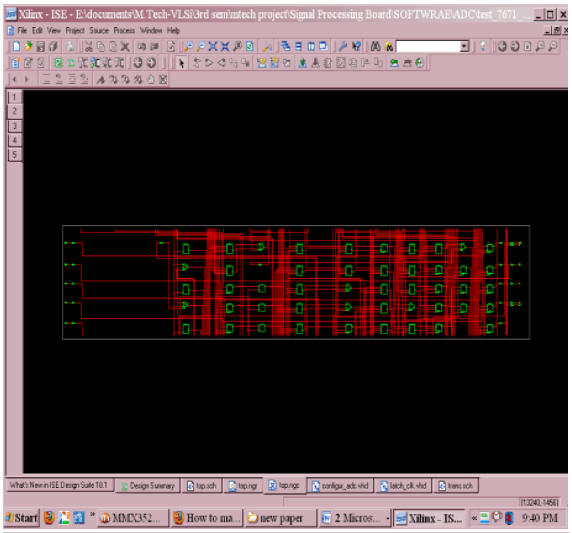


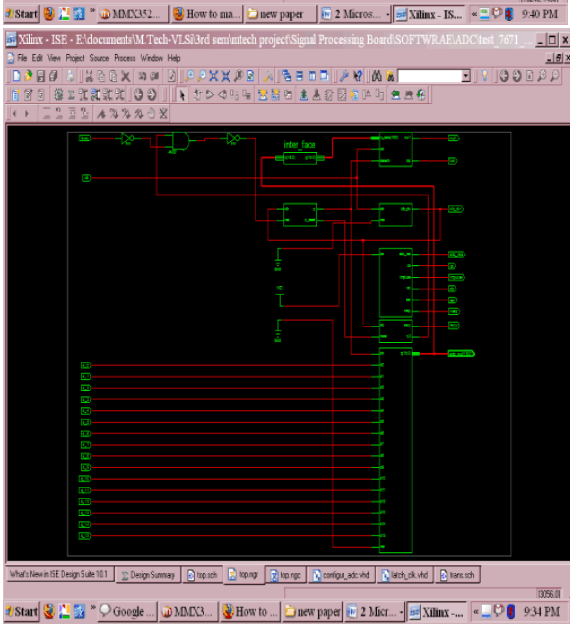
Fig. 6: Working Of ADC

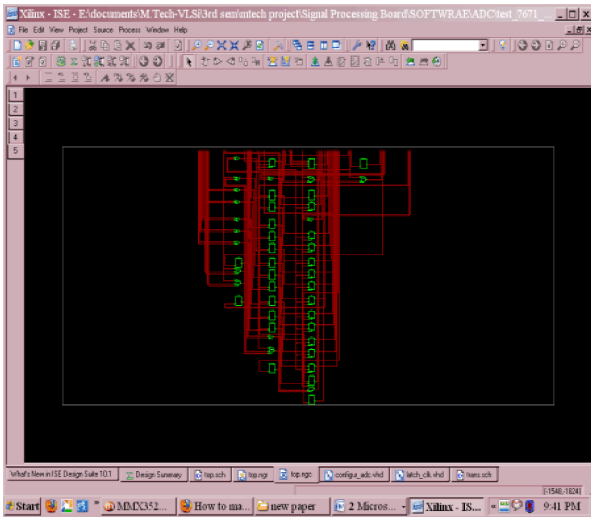
Modeling of Adc Driver Interfacing / Rtl Interfacing: The RTL schematic obtained though the Xilinx tools are shown below.











Working of Signal Processing Card: The following flow chart shows the working of signal processing card (Fig. 4), first the FPGA is initialized for all I/O peripherals. Then analog data is applied to the ADC in the form of LASER beam, where it gets converted to digital form and stored in FLASH memory. This digital signal is then retrieved and processed by FPGA and synthesized by DDS interface, the o/p of this stage is noise free analog signal. This analog signal is then compared with the previous analog signal and is checked for noise removal. If the noise has been removed the signal is transferred to the display. If there is no change in the compared signal then it is again send for processing and synthesizing.

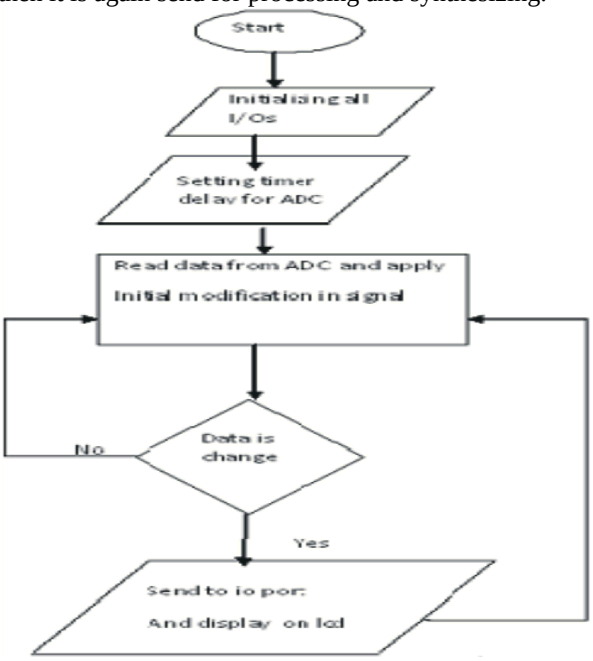


Fig. 7: Working of signal processing card

Table 1: The advance HDL Synthesis Report information

Advanced Hdl Synthesis Report	
Macro Statistics ROMs	4
16x8-bit ROM	4
Counters	8
4-bit up counter	3
13-bit up counter	1
5-bit up counter	2
Registers	33
Flipflop	33
Comparators	1
5-bit comparator less equal	1
Tristates: tristate buffer	2, 16-bit 1, 8-bit
Total no. of Statistics Registers	94
Total no. of Flip-Flops	94

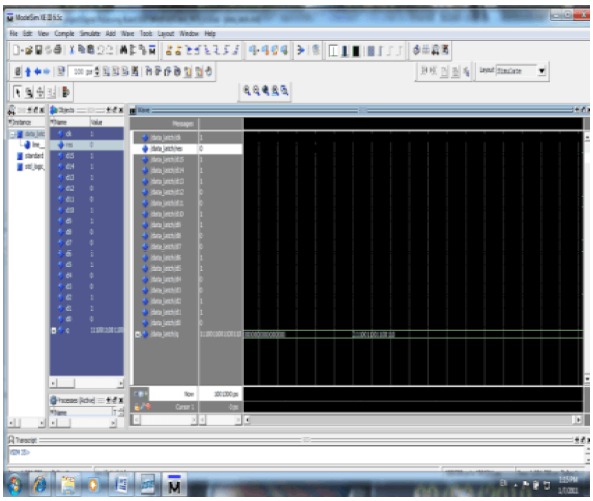
Table 2: The device utilization information

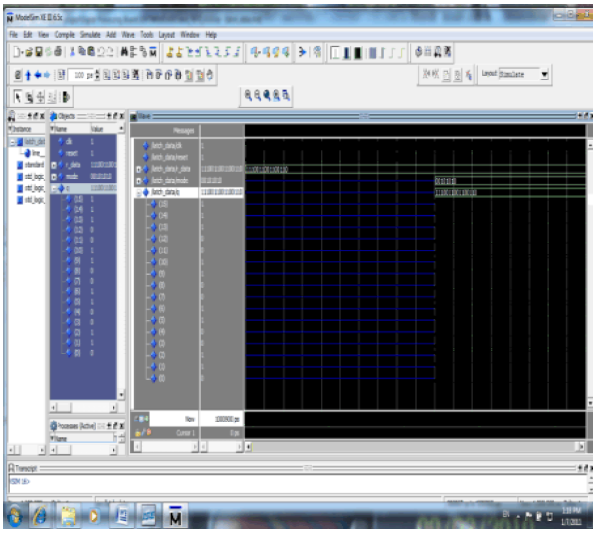
Device Utilization Summary: Selected Device 4vsx35ff668-12	
Number of Slices	70 out of 15360
Number of Slice Flip Flops	78 out of 30720
Number of 4 input LUTs	119 out of 30720
Number of IOs	44
Number of Bonded IOBs	44/448
Number of GCLK	2/32

Synthesis and Simulation Results: The following report shows the synthesis result of ADC7671 which is automatically generated from the designed VHDL coding in Xilinx environment.

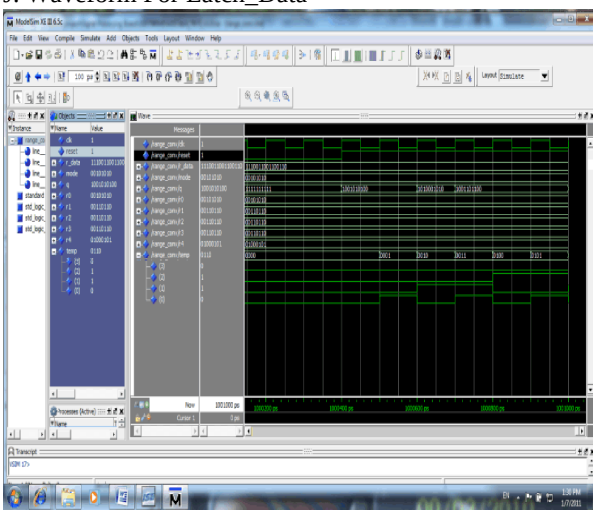
Simulation Results: The proposed technique is implemented in VHDL, simulated on Modelsim and synthesized using Xilinx ISE. The RTL generated is functionally verified for correct operation. The device considered while XC4VSX35-10FF668". The simulation waveform is shown below:

I. Waveform For Data_Latch In ADC





J. Waveform For Latch_Data



K. Waveform For Range_Conv In ADC

CONCLUSION

The design trend in this card is towards small size, high integration and fast real time processing. This paper shows overall working and advantage of using high speed ADC with FPGA in comparison with other general purpose controllers. Using high speed ADC with FPGA can be used for real time processing due to high data rates in FPGA.

The high-speed data transmission seems to work well and theFPGA can handle the high frequency signals as well and the vast amount of data that needs to be processed and transferred, most applications cannot be implemented by using standard DSP's. Most typical high-volume consumer applications are cost sensitive and are better addressed with the usage of a dedicated ASIC.

However the ever increasing cost associated with developing an ASIC and the long development cycles do not work for many of the applications. These applications are better served by using FPGA based platforms. The above described ADC & FPGA interface card is tested for LASER based audio application. Hence this paper comes to conclude that Virtex-4 FPGA interface provide a flexible andversatile platform for building high-speed LVDS signaling interfaces to all the latest ADC and DAC devices on the market.

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