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# Comparative Analysis of Low Power Master Slave Single Edge Triggered Flip Flops

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**Abstract:** In this paper, we compared various previously published master slave Single Edge Triggered D Flip Flops (SET D FFs). Flip Flops are most essential elements in the design of sequential circuits. We did the comparison for their performance and power dissipation. Because power depends on number of transistors in the circuit, so we compared the transistor count of each Flip Flop.

**Key words:** Static · Semi-static · Transmission Gate · Pass Transistor · Edge triggered · Short circuit current · Low voltage swapped body bias · Sub-threshold grounded body bias · No body bias

## INTRODUCTION

In recent years, the demand of mobile devices is increasing. So low power design is the need of today's integrated systems. For instance, wireless communication devices, hand-held and palm-top computers, portable versions of microprocessors, all require low power design [1]. The system on chip (SoC) design will integrate hundreds of millions of transistors on one chip, whereas excess heat removal techniques are limited [2]. Therefore the circuits should be designed for low power. Minimizing power dissipation during the VLSI design flow increases lifetime and reliability of the circuit [3]. Studies show that 40-45% of total power dissipated in integrated system is due to clock distribution network [4]. Power and performance are two essential features which are corresponded with each other, produce main concerns in designing and implementation [5].

Flip flops and latches are the basic storage elements used extensively in all kinds of digital designs. A large portion of the clock power is used to drive these sequential elements. By reducing the clock power of flip-flops and latches, the total chip power can be reduced. Flip-flops appear in various configurations, such as J-K flip-flops, D-flip-flops and T-flip-flops, where the D-flip flop is the most common. A conventional single edge-triggered (SET) flip-flop typically latches data either on the rising or the falling edge of the clock cycle. The SET flip-flops are usually configured as Master-Slave configuration, i.e., a sequential structure using two latches, called master and slave respectively, in cascade [6] as shown in Fig. 1.

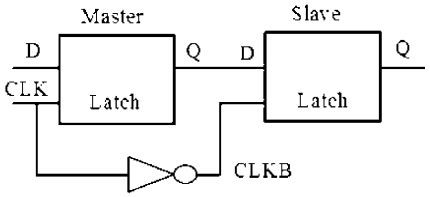

Fig. 1: Representation of MS SET D Flip Flop

**This Paper Is Organized as Follows:** Section II explains different Flip Flop structures. Flip flops are compared on the basis of power consumption, delay and transistor count in Section III. Paper ends in Section IV with our conclusion.

**Master Slave Single Edge Triggered Flip Flops:**

**NAND Flip Flop:** The classical NAND latch based flip-flop is shown in Fig. 2 [7]. When the clock is at logic 'HIGH', the input D is latched to an intermediate node N. Similarly when CLK changes to logic 'LOW', the slave latch gets functional and the logic level at node N is transferred to the output Q. In some conventional flip flops contention occurs. This may cause the functional errors. This NAND latch based flip flop eliminates this problem. But the number of transistors in NAND FF increases. NAND FF has 36 transistors. So NAND FF has large area. In applications where area is of prime concern, this flip flop is not recommended.

**Contention Less Flip Flop (CLFF):** The NAND latch based flip-flop (Fig. 2) eliminates the problem of contention. But the number of transistors in NAND FF increases to 36. The large area of NAND FF can't be

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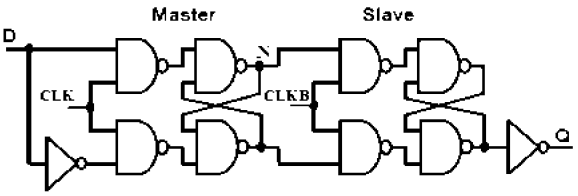


Fig. 2: NAND Flip Flop

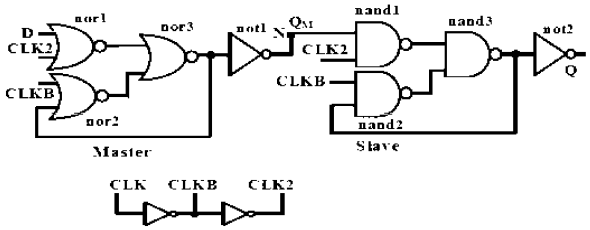


Fig. 3: Contention-less flip flop (CLFF)

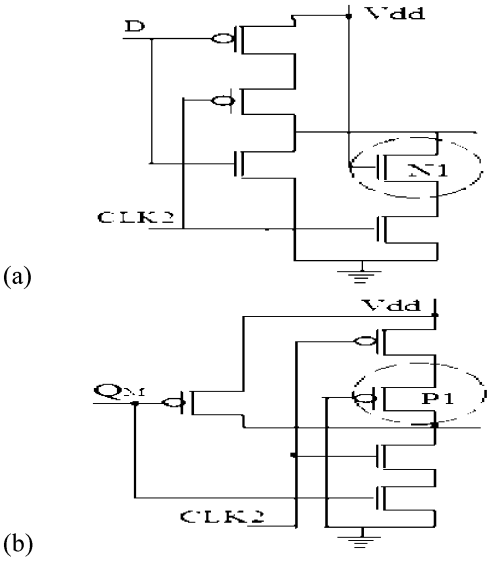


Fig. 4: Internal structure of (a) nor1 (b) nand1

accepted. So [8] proposed an area efficient contention less flip flop (CLFF) which is shown in Fig. 3. This flip flop has master slave latches which are implemented with NOR and NAND gates. When CLK=0, the master latch transfers the input D to an intermediate node N and the slave latch retains data of the previous cycle. Similarly when CLK=1, the master latch retains the latest data and the slave latch transfers the data to the output Q. CLFF has smaller area than NAND FF. NAND FF has 8 two input NAND gates while CLFF has 3 two input NOR gates and 3 two input NAND gates.

But reducing the gates creates a racing problem in this flip flop. To remove the racing problem the authors added an NMOS transistor (N1) in the NOR gate nor1 of master latch as shown in Fig. 4. Similarly the authors added a PMOS transistor (P1) in the NAND gate nand1 of the slave latch. Adding theses two transistors do not increase the switching power of CLFF, because they are normally ON transistors. However the transistor count of CLFF is 30, it has larger area as compare to other flip flops. In applications where area is of prime importance, this flip flop is not recommended.

**TG Flip Flop:** The conventional negative edge-triggered TG (transmission gate) based flip flop consists of two-level sensitive latches with 16 MOSFETs as shown in Fig. 5 [9]. The Master latch is functional on the positive level of the clock. This latch transfers the logic level at input D to the intermediate node N. The feedback loop maintains the logic level at the node N when the clock goes to logic level 'LOW'. Similarly, the Slave latch is functional on the negative level of the clock and transfers the logic level at intermediate node N to the output node Q. Again, the feedback loop maintains the logic level at node Q while clock is at logic level 'HIGH'. The speed of this TGFF is limited by two gate delays (one transmission gate and one inverter) as in Fig. 5. The advantage of this flip flop design is that it involves minimum design risk. This is widely used due to its small area and lesser power consumption. In low power applications where speed is not of prime concern, this TG flip flop can be used.

**Low Area D-Flip Flop:** The conventional TG flip flop requires a relatively large number of clocked transistors. To reduce the clock load of the flip flop the interrupting TG in the feedback loop of both master and slave latches can be removed. This low-area DFF is shown in Fig. 6 [10]. This low-area flip flop has lesser number of transistors and clocked transistor as compare to TGFF, even then it consumes more total power and is slower compared to the conventional TGFF.

**Push Pull Flip Flop:** In order to improve performance of a conventional DFF, [11] proposed addition of an inverter and transmission gate between the outputs of master and slave latches to accomplish a push-pull effect at the slave latch, i.e., input and output of the output inverter (which drives the signal Q directly) will be driven to opposite logic values during switching. This push-pull FF is depicted in Fig. 7. It adds four MOSFETs, but reduces the clock-to-output (C-to-Q) delay from two gates in a TGFF to one gate. One method to reduce the transistor count is to use an NMOS for latch input in place of transmission gate. However, since the output of an nMOS can only reach a voltage level of $V_{dd}$ -$V_t$ when it is at

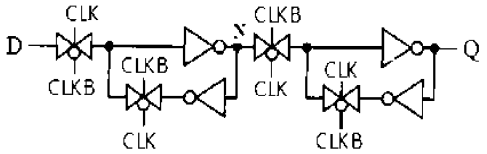


Fig. 5. TG Flip Flop

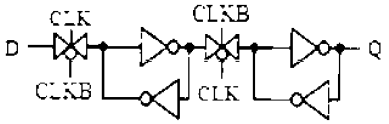


Fig. 6: Low Area D- Flip Flop

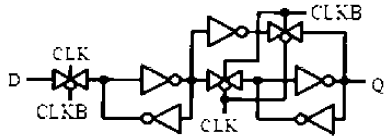


Fig. 7: Push Pull Flip Flop (PPFF)

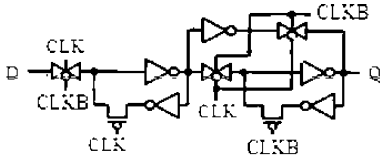


Fig. 8: Push Pull Isolation (PPI) Flip Flop

logic 1, it results in increased power dissipation. So a transmission gate is kept in the push-pull FF. To offset the four added MOSFETs for a push-pull FF, [11] proposed the elimination of two transmission gates from the feedback paths, as shown in Fig 7. Compared to the TGFF, this push-pull FF is 20% faster, but has a 24% power overhead [11].

**Push Pull Isolation (PPI) Flip Flop:** To optimize the proposed push-pull FF for energy usage, [11] added two PMOSFETs to isolate the feedback path, as illustrated in Fig. 8. This PPIFF increases the transistor to 18, but total power dissipation is reduced up to 14% and a speed is increased up to 20% relative to the previous push-pull FF. Compared to the TGFF, PPIFF improves speed by 36% at an expense of 7% more power. In applications where speed is of prime importance, this flip flop is recommended.

**Pass Flip Flop:** The pass flip flop [12] is designed by modifying the TGFF. In this flip flop the number of transistors are reduced that save power. It also improves speed due to reduced load capacitance. This is helpful especially in low voltage operation, where substantial speed improvement is achieved due to reduced capacitance at intermediate nodes. The four transistors in

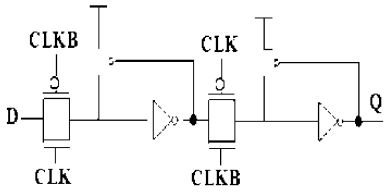


Fig. 9: Pass Flip Flop

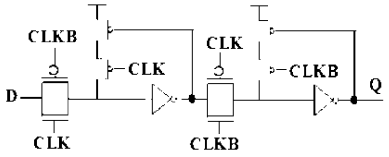


Fig. 10: Pass Isolation Flip Flop

the feedback path are replaced by a single PMOS transistor. Hence, three transistors are saved in each latch. The PMOS transistor in the feedback path maintains the state of the latch when clock (CLK) is OFF. The disadvantage of this flip flop is that there may be short circuit current during change of state of the latch.

**Pass Isolation Flip Flop:** The pass isolation flip flop is an improvement over PPFF structure. This is a semi-static version of PPFF designed by removing both NMOS transistors in the feedback path of latches [12]. When compared with the Pass FF, Pass isolation FF has extra PMOS transistor in the feedback path. But this extra PMOS transistor ensures the feedback path to be activated only during OFF cycle. As a result, short circuit current is reduced during ON cycle and also improves speed. This flip flop occupies lesser area as compared to other flip flops and hence saving power. This is helpful especially in low voltage operation.

**LVSB, STGB, NBB Flip Flops:** The design of 10-transistor negative edge triggered SET D-flip-flop [13] is shown in Fig. 11. [14] Modified the 10-transistor design proposed by [13] by changing the substrate connections. The idea is to reduce the overall area and power consumption such that the design becomes better applicable for the low power applications. Fig. 12 shows Low Voltage Swapped Body (LVSB) bias 10-transistor design. In this design, substrate of all PMOS transistor are connected to ground and substrate of all NMOS transistors are connected to the supply voltage ($V_{dd}$) [15]. In this type of substrate connection, bulk voltage is less than the source voltage ($V_B < V_S$). As a result, all devices receive an amount of forward body bias equal to $V_{dd}$. Fig. 13 shows Sub Threshold Grounded Body (STGB) bias 10-tramsistor design. In this design, substrate of all

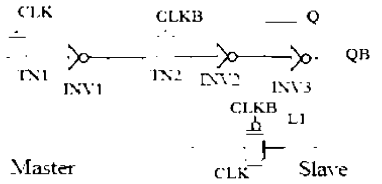


Fig. 11: 10 transistors flip flop proposed by [13]

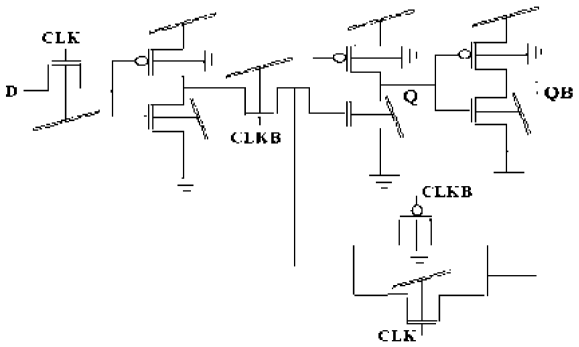


Fig. 12: Low Voltage Swapped Body (LVSB) bias 10-transistor SET Flip Flop

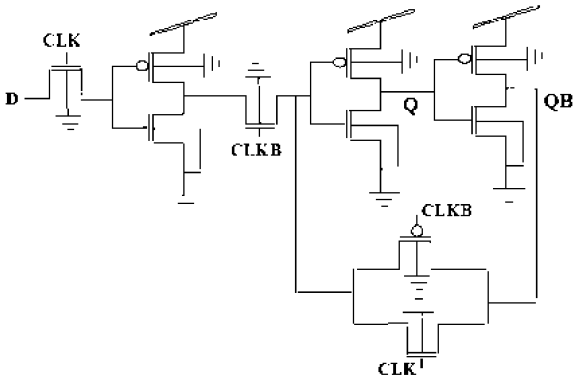


Fig. 13: Sub-Threshold Grounded Body (STGB) bias 10-transistor SET Flip Flop

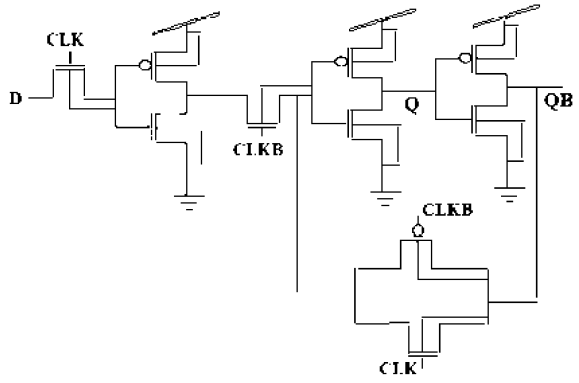


Fig. 14: No Body Bias (NBB) 10-transistor SET Flip Flop

NMOS and PMOS transistors are connected to ground [16]. This type of substrate connection reduces the complexity of the design. All the NMOS transistors are at no body bias condition and all PMOS are at forward body bias condition. STGB design is less sensitive towards supply and ground noise than LVSB design. In No Body Bias (NBB) condition, the substrate of the MOSFET is connected to the source and thus the $V_{SB}$ of the MOS transistor is always zero and thus it is known as No Body Bias (NBB) condition. In NBB connection, threshold voltage of the MOSFET transistor is always constant. Fig. 14 shows No Body Bias (NBB) 10 - transistor negative edge triggered SET flip flop. These Flip Flops have lesser area as compared to other flip flops and hence saving power. These are helpful especially in low voltage operation, where substantial speed improvement is achieved due to reduced capacitance at intermediate nodes.

As reported by the authors that the NBB design of SET flip flop shows better performance in terms of power dissipation and area as compare to LVSB and STGB designs. It is also technology independent. Hence NBB design of negative edge triggered static SET FF design is suitable for portable application, as it is more area as well as power efficient.

**Pass Transistor (PT) Flip Flop:** Pass Transistor (PT) flip flop proposed by[17], is shown in Fig. 15. The master section of this flip flop is the positive level triggered D latch that transfers the logic level at input D to the intermediate node N. When the clock goes to logic level 'LOW' the feedback path consisting of pMOS transistor maintains the logic level at the node N. The slave section consists of a negative level triggered D latch that transfers the logic level at intermediate node N to the output Q. When the clock goes to logic level 'HIGH' the feedback path consisting of pMOS transistor maintains the logic level at the output node Q.

A PMOS transistor is used in the feedback path as it leads to a more compact layout than using a NMOS transistor. But due to this the logic level at the output node Q is being maintained when the clock is logic 'HIGH' and not when the clock is logic 'LOW'. Therefore, when the clock is stopped, this circuit does not show the static behavior. By using NMOS transistor in feedback path instead of PMOS transistor, this limitation can be overcome. Then the circuit will become static without increasing the number of transistor. This flip flop has 12 transistors. In these 12 transistors, 4 transistors are clocked transistors.

**$C^2$MOS Flip Flop:** Fig. 16 shows the static $C^2$MOS flip-flop proposed by [18]. That consists of a weak $C^2$MOS feedback at the outputs of the master and the slave

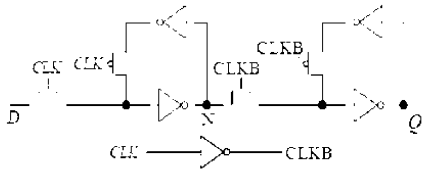


Fig. 15: Pass Transistor (PT) Flip Flop

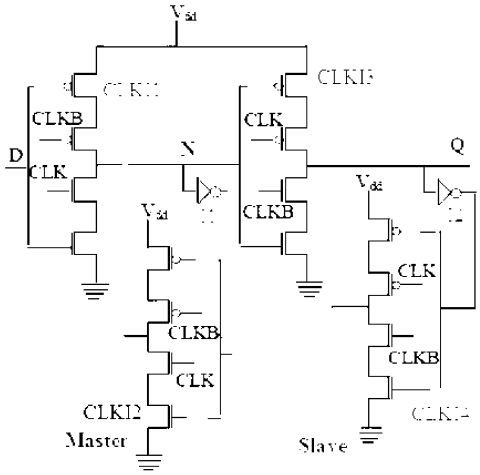


Fig. 16: C²MOS Flip Flop

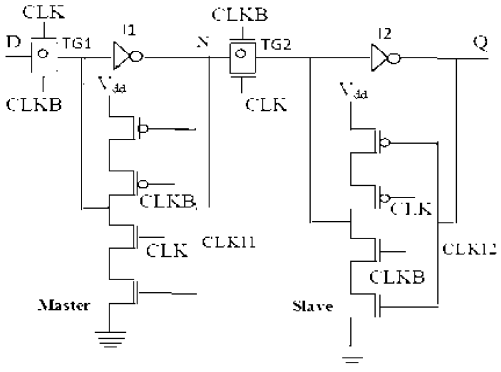


Fig. 17: Power PC Flip Flop

latches. When the clock is at logic 'HIGH', the clocked inverter CLKI1 latches the input at D to an intermediate node N. The feedback consisting of clocked inverter CLKI2 and inverter I1 maintains this logic level at node N when clock is at logic level 'HIGH'. Similarly when CLK changes to logic 'LOW', the slave latch gets functional and clocked inverter CLKI3 transfers the logic level from node N to the output Q. The feedback consisting of clocked inverter CLKI4 and inverter I2 maintains this logic level at output node Q when clock is grounded. There is no Vt-drop at intermediate circuit nodes. So the circuit is more robust to noise with high noise margins in comparison to the previously mentioned circuit (Fig. 15. PTFF). There are 20 transistors in this circuit.

**Power PC Flip Flop:** There is no $V_t$ drop at intermediate circuit nodes in C²MOS FF. This makes C²MOS FF more robust to noise with high noise margins in comparison to the flip flop proposed by [17]. But, in C²MOS FF the number of transistors is increased to 20. So area and power dissipation is increased. The limitation of transistor count can be overcome by using Transmission Gates (TG1 and TG2) in place of C²MOS latches (CLKI1 and CLKI3) in the forward paths as shown below in Fig. 17 [19]. In this flip flop the transistor count is 16. This improves the design as compared to the C²MOS FF.

## RESULTS

In this section, the flip flops are compared for speed and power. The results are shown in Table 1 [11]. The evaluation was done by [11] using a 0.6-µm CMOS technology with a supply voltage of 3.3 V. The time-averaged power dissipation was characterized from SPICE simulation under the condition of 100-MHz clock frequency and 25°C temperature. Because power depends

Table 1: Comparison of Power and Delay of various Flip flops

| Parameters 3.3V, 25°C | TG FF | Low area FF | Push pull FF | Push pull isolation FF |
|---|---|---|---|---|
| Average Power (µW) | 122.9 | 146 | 152.6 | 131.4 |
| C to Q Delay (ps) | 245.0 | 311 | 195.5 | 157.0 |

Table 2: Transistor count of various Flip Flops

| S. No | Flip Flop | Transistor count | S. No | Flip Flop | Transistor count |
|---|---|---|---|---|---|
| 1 | NAND FF | 36 | 8 | Pass isolation FF | 12 |
| 2 | CLFF | 30 | 9 | LVSB FF | 10 |
| 3 | TG FF | 16 | 10 | STGB FF | 10 |
| 4 | Low area FF | 12 | 11 | NBB FF | 10 |
| 5 | Push pull FF | 16 | 12 | PTFF | 12 |
| 6 | Push pull isolation | 18 | 13 | C²MOS FF | 20 |
| 7 | Pass FF | 10 | 14 | Power PC FF | 16 |

on number of transistors in the circuit, so we compared the transistor count of each flip flop. Table 2 shows the transistor count of all discussed flip flops.

The low-area DFF consumes 20% more total power and is 27% slower compared to the TGFF. PPIFF increases the transistor to 18, but total power dissipation is reduced up to 14% and a speed is increased up to 20% relative to the previous push-pull FF. Compared to the TGFF, PPIFF improves speed by 36% at an expense of 7% more power.

## CONCLUSION

We did comparative analysis of various master slave single edge triggered flip flops. The NAND latch based flip-flop (Fig. 2) eliminates the problem of contention. But the number of transistors in NAND FF increases. NAND FF has 36 transistors. [8] Proposed an area efficient contention less flip flop (Fig. 3) which has 30 transistors. CLFF is better than NAND FF. The low-area DFF is slower and also consumes more power as compared to the TGFF. Fig. 18 shows PPIFF increases the transistor count to 18, but achieves a reduction in total power dissipation and a speedup relative to the previous push-pull FF. Compared to the TGFF, PPIFF improves speed but at the expense of power. We find that NAND FF, CLFF and Push pull isolation FF have large transistor count. So when area is of prime concern, these flip flops are not recommended. Although it is found that Push pull isolation FF has less delay and better power dissipation. Pass Flip Flop, Low Voltage Swapped Body (LVSB) Flip Flop, Sub Threshold Grounded Body (STGB) Flip Flop and No Body Bias (NBB) Flip Flop has least transistor count. These flip flops occupy lesser area as compared to other flip flops and hence saving power. It also improves speed due to reduced load capacitance. This is helpful especially in low voltage operation, where substantial speed improvement is achieved due to reduced capacitance at intermediate nodes. In Pass Flip Flop there may be short circuit current during change of state of latch. By adding an extra PMOS transistor in feedback path, the feedback path can be activated only during OFF cycle. So short circuit current is reduced during ON cycle and also it improves the speed. Therefore Pass isolation Flip Flop is better than a Pass Flip Flop.

In PTFF, a PMOS transistor is used in the feedback path as it leads to a more compact layout than using a NMOS transistor. But due to this the logic level at the output node Q is being maintained when the clock is logic 'HIGH' and not when the clock is logic 'LOW'. Therefore, when the clock is stopped, this circuit does not show the

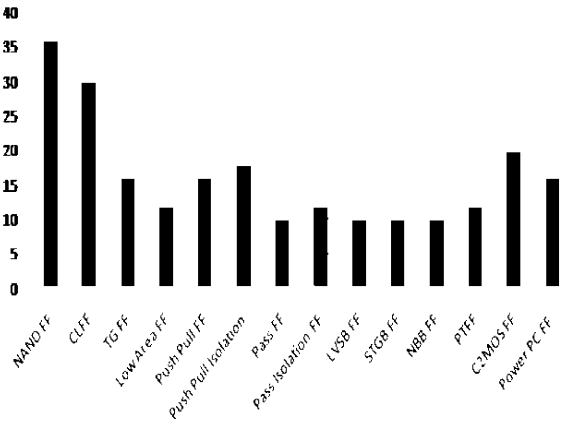


Fig. 18: Transistor count of various Flip Flops

static behavior. By using NMOS transistor in feedback path instead of PMOS transistor, this limitation can be overcome. Then the circuit will become static without increasing the number of transistor.

Due to no $V_t$ drop at intermediate circuit nodes, $C^2MOS$ FF is more robust to noise with high noise margins in comparison to the PTFF. But, number of transistors is increased to 20. The limitation of transistor count can be overcome by using Transmission Gates in place of $C^2MOS$ latches in the forward paths as shown in Fig. 17. Thus transistor count is reduced from 20 to 16. This improves the design in terms of power and area.

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