World Applied Sciences Journal 16 (Special Issue on Recent Trends in VLSI Design): 78-91, 2012
ISSN 1818-4952

Investigation of Low-Power Techniques in Network-on-Chip

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Abstract: The Network-on-Chip (NoC) has emerged as underlying infrastructure for communications between Intellectual Property (IP) cores. Due to ever increasing integration of IPs the need of Network-on-Chip for efficient communication has attracted the attention of researchers for low-power technique. The SoCs available are quite efficient and have high speed operation and parallelism concepts. But the power consumed is a factor of consideration specially seeing their application in different domains. The local orthodox techniques for power saving are not sufficient to address the power issue to reduce the power dissipation in the interconnection network [1]. So there is a quite urgency for specialized power aware techniques, specially, capable of addressing the complex, ever increasing SoC's power and energy issue. In this paper we have investigated various levels where power can be reduced. This paper also presents mathematical model that can be applied to reduce the power.

Key words: Interconnection networks · Network-on-Chip (NoC) · System on Chip (SoC) · Low power · Power and energy modelling

INTRODUCTION

The Network-on-Chip (NoC) is an emerging communication paradigm for integrating large number Intellectual Property (IP) cores on single chip. Broadly, we can classify SoCs as

- Platform based SoCs and
- Fixed function based SoCs.

The Platform based SoCs, are somewhat generic, in nature, as they are able to perform a wide variety of functions; and some of which are not foreseen during the design process. On the other hand, fixed function SoCs are targeting towards any particular task or functions in a range lying in a known domain of application with known properties [2]. The advances in scaling of technology has made possible to integrate large number of processors onto a single chip, forming chip multi-processor (CMP) aiding the high performance system design due to which the interconnection bandwidth requirement has increased [3].

The count of IPs is bound to increase with new advances in the technology. To establish communication among the IPs the number of communication channels need to increase. Simple metal-layer mechanism is not sufficient to provide efficient communication link for the IPs on SoC. The NoC is proving to be best resort for addressing the ever increasing capacity for establishing the required interactions in-between the ever increasing IPs on the chip. [4]. Therefore, NoC is replacing the ad-hoc global wiring interconnects by sending packets within each IPs in SoCs enabling efficient designing of high-performance circuit.

The NoCs can be broadly classified as synchronous and asynchronous switching. In synchronous switching the clock is distributed all over the chip components having two main parts global clock distribution network and local clock distribution network. Asynchronous switching use hand-shaking signals to synchronize the communications in place of clock. These systems require request and acknowledge signal for handshaking and generally use four-phase handshaking to complete the data transfer [4]. Another classification of NoCs can be

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made depending upon the type of network embedded namely, shared medium networks, indirect networks and hybrid networks [5]. We discuss briefly about each of the network as follows:

Types of Network

Shared Medium Network: This type of network is most popular among all the available networks. This can be further classified as single bus network and multiple bus networks. The single bus network architecture is used traditionally for data-path interconnection as it is very simple in design and implementation. On the other hand multiple bus network architecture evolving from crossbar network structure is somewhat better than single bus with large nodes. But comparing with other architecture it is still not very efficient in terms of energy and power.

Direct and Indirect Network: Indirect network, each node is directly connected to the limited neighboring nodes. Hence, it is also called as point to point network. Indirect networks are switched based networks, where the connection between the nodes passes through a set of switches which provide a programmable connection between their ports setting-up the communication path which can change over time. Nowadays the distinctiveness of the two direct and indirect is blurring with absorption of one another's functionality by the routers and switches.

Hybrid Network: Hybrid tends to have a system incorporating the merits of different systems. It provides more flexibility, performance and energy-efficiency. Here hierarchical and heterogeneous architecture are very widely used and are more energy and power efficient. Also a reconfigurable-interconnects concepts aids the performance.

Shared Mechanism Bus: This is commonly used communication architecture for SoC as this is simple, low cost, area efficient and easily extensible. But the monolithic shared bus is not completely efficient in terms of energy efficiency because of large capacitive load of the entire bus and limitation of one component pair to communicate at a given time.

Routers and Switch Networks: This is a fully connected crossbar, which may be optimized utilizing the fact that not every node needs to talk to others nodes. This provides an isolation leading to reduced load capacitance during the transfer, hence proving to be good energy efficient. A brief discussion of the switch architecture technique is as follows:

Crossbar Topology: It uses space division multiplexing for input and output connection where every input-output connection has its own dedicated data-path. So these are interconnecting contention free. Here any of the N input can be connected to any of the N output ports.

Full-Connected Network: It uses MUXes to aggregate the inputs to the outputs which are controlled by the arbiter implemented for controlling the linking. There is no internal buffers needed in the power modeling and this also is interconnecting-contention free.

Banyan Network: This is an isomorphic variation of butterfly topology. This routing is a self routing form and if two packets arrive at same destination at same time then one of them would be buffered. Here different data-path can share same interconnect and hence have interconnect contention problem. So a buffer is required at each internal node switch. The bit energy can be depicted as

$$E_{bit_{Banyan}} = \sum_{i=0}^{n-1} q_i E_{Bit} + 4\sum_{i=0}^{n-1} 2^i E_{T_{bit}} + nE_{S_{bit}}$$

Batcher-banyan Network: This is made to solve the interconnect contention problem in Banyan Network by applying Batcher Sorting Network before Banyan Network leading to dedicated path for each input output connection. Here the bit energy is depicted as

$$E_{bit_{Batcher}} = 4\sum_{j=0}^{n-1}\sum_{i=0}^{j} 2^i E_{T_{bit}} + 4\sum_{i=0}^{n-1} 2^i E_{T_{bit}} + \frac{1}{2}n(n+1)E_{ss_{bit}} + nE_{SB_{bit}}$$

Clustering: It is a pre-processing step of grouping certain identified cores into one identity keeping the global reference of communication between the cores allowing a hierarchical approach of communication. It enables the cores to share the physical communication channels reducing the size, complexity and efficient resource sharing.

Globally Asynchronous Locally Synchronous (GALS): Clock is major source of power dissipation. To address this issue, GALS tries to identify and partition the system

into different optimal Synchronous Blocks (SB) which communicate with each other asynchronously, enabling to change the clock as per the local needs, hence reducing the average frequency of the system and hence the power dissipation.

Importance of Power Efficiency in NOC: The SoCs available are quite efficient and have high speed operation and parallelism concepts. But the power consumed is a factor of consideration specially seeing their application in different domains. Out of the total power substantial amount of power is due to interconnection network. For an example the MIT Raw on chip network consumes 36% of the total chip power and 20% of total power by Apha 21364 microprocessor due to the interconnection network. Hence there is a need for power aware interconnection network design [3]. Local orthodox techniques for power saving are not sufficient to address the power issue to reduce the power dissipation in the interconnection network [1]. So there is a quite urgency for specialized power aware techniques, specially, capable of addressing the complex, ever increasing SoC's power and energy issue. The power issues in NoC can be addressed at different abstract level starting from architecture level to RTL level to implementation/ physical level [2]. And the good news is that many researchers are working to address the complex issue and now some techniques are available using which the process of estimating power consumption in NoCs is made possible and hence reducing the same.

In the previous paper [6] we have discussed some techniques for addressing the energy and power issues in NoC and this paper carry forward this journey of exploring the energy and power aware techniques. The paper is organized as follows: Section 2 power modelling techniques. Section 3 presents an exhaustive investigation of existing power estimation and reduction techniques. In this section we have presented various mathematical models to reduce the power. Finally, a conclusion is presented in the last section.

Power Estimation and Reduction Techniques: The power model for estimating and reducing the power in the NoCs can be broadly classified according to the abstract levels in design process. The lowest level of abstraction is the gate level abstraction which represents the model at transistor level. The model at this level are generally most accurate model as they consider the lowest element in the design i.e. the transistor, but these are very time and resource consuming models. The next level of abstraction is the Register Transfer Level which considers the transfer of data at register level. The system level is the highest level of abstraction, emulating the functionalities performed, without going into the hardware details of the different components. The power models based upon the System level abstraction are the least accurate among themand but advantageously they require less time and resource [3].

The main blocks, culprit for power consumption in NoCs are mainly three, namely buffers section, control Logic section and crossbar section. The power consumption in buffers is the most significant part with contribution factor of around 88% of the total power dissipation [7]. The architecture considered while implementation of the network governs the power model to be used for estimating and reducing the power issues.

Power Modeling: As discussed in the previous section, the power consumption in the on-chip inter-connection network generally counts-in three main sources namely: internal node switch, internal buffer queues and interconnect wires [5]. For estimating the dynamic power consumption many researcher use Bit Energy (E_{bit}), defined as the energy consumed while bit transported from ingress port to egress port. Bit energy is considered as summation of energy consumed on node switch (E_{sbit}), internal buffer (E_{bbit}) and on inter-connects wire (E_{wbit}).

Also $E_{Bbit} = E_{access} + E_{ref}$, where E_{access} is the, energy consumed by each access operation (providing average energy consumed for one bit) and $E_{ref}$is the energy consumed by each memory refreshing operation.

Node Switch Power Consumption: These are located on the intermediate nodes (inside the switches) used to direct the packets from one stage to another stage, until destination is reached. In the process, both header data path and payload data path consume the energy. The power is also dependent upon the presence and absence of the packets on different ports of the node.

Internal Buffer Power Consumption: At the time of conflict between packets; internal buffers are used to store the packet with lower priorities. Generally two types of conflict (namely destination contention and interconnect contention) are occurred. Destination contention occurs due to presence of two or more packets in the ingress port with same destination port at the same time. These issues are application dependent.

Interconnect Contention or internal blocking occurs when at the time of shared interconnect link for two or more packets with different destination. The issues related to interconnect contention are mostly architecture dependent.

Interconnect Wires Power Consumption: Energy dissipated during charging and discharging while toggling of the wires between logic level '0' and logic level '1'is considered here. Also the E_{wbit}, 1->0 and E_{Wbit} 0->1 have some significant bit energy values and on the other hand E_{Wbit} 0->0 = 0, E_{Wbit} 1->1 = 0. The wire bit energy can be depicted as follows :

$$E_{W_{bit}} = \frac{1}{2}C_{wire}V^2 + \frac{1}{2}C_{input}V^2 = \frac{1}{2}C_wV^2$$

where, C_{wire} is wire capacitance C_{input} is total input gate capacitance. Also the total C_{load} capacitance can be depicted as: $C_w = C_{\text{input}} + C_{\text{wire}}$

The crossbar bit is given as follows:

$$E_{bit_{crossbar}} = N \times E_{S_{bit}} + 8N \times E_{T_{bit}}$$

where, E_{Sbit} is the energy in switch and E_{Tbit} is the Thomson bit energy.

Interconnect Wire Length Estimation: As the capacitance depends upon the length of the wire, therefore, it is estimated using Thompson Model, generally.

Different techniquesfor energy and power estimation and reduction are discussed as follows:

Investigation of Available

Technique 1: The power estimation model proposed by the author is meant for the RTL abstraction level and is based upon the average reception rate at each router buffer [7]. Author estimated the power using two steps namely, calibration and application. Parameters used are defined in the first calibration step which begins with synthesizing process using the target technology. This is followed by simulation taking the set traffic scenario and the value change dump (VCD) file generated. The VCD file contains the switching activity corresponding top each signal in under consideration. Using this, authors have estimated the power using the power estimator tool. From the above sequential activities, a table for different injection rate is generated corresponding to each element and activity. Using linear adjustment technique power estimation equations are formed providing the relationship between power consumption as a function of injection rate. In the second step the NoC is simulated. Then thereception rate for each buffer is derived using monitors inserted in every buffer. Applying the power consumption equation along with associated buffer,the associated power is calculated. The power consumption for control-buffer is calculated using the average reception rate of all the buffers. Upon accumulation of these, the total power consumption is obtained. Therefore,this method depends upon the reception rate sampling period. The power equation for the router is given below where 'm' represents the number of buffers in the router and 'n' represents the number of sampling periods.

$$P_{avg} = \sum_{k=1}^{m} \frac{\sum_{i=1}^{n} Pbuffer_{k_i}}{n} + Pcrossbar + Pcontrol$$

Technique 2: The power estimation model proposed by the author is meant for architectural level of abstraction in the design process of NoC. The power estimation model uses reconfigurable interconnect architecture to build a computational engine through spatially programmed connections of process elements called satellites [5]. Author hasused four clusters of tightly connected modules as per kernel benchmark set to minimize the global connections. The clusters have local mesh (with 2 buses per channel) for intra-cluster connections and I nterface ports for inter-cluster connection. The proposed hierarchical network architecture requires limited number buses for implementing sufficient connection with flexibility of good degree of freedom. Author reported a seven times energy cost reduction as compared to the simple crossbar network with flexibility with respect to its application. Measuring the distance expressed by Manhattan Distance (the shortest distance between two points measured along X and Y axes). Author reported that hierarchical mesh network performs the best for both global and local interconnections. In the best case the net cost in hierarchical mesh is ten times lessas compared with the net cost in multiple bus network and in worst case it is one half of the multiple bus cost.

Technique 3: The power estimation model proposed by the author uses Globally Asynchronous Locally Synchronous (GALS) technique. The proposed technique

addressed both the dynamic and static power consumption in NoCs using an adaptive technique. The proposed technique called ALPIN "Asynchronous Low Power innovative NoC" circuit is implemented in 65nm technology. The technique covers the system level to physical level of abstraction addressing the power optimization of interconnection communication in NoCs. The Components of the ALPIN can be summarized as follows [1]:

Power Aware GALS NoC Architecture: ALPIN, a fully power-aware GALS NoC architecture is proposed for power modeling. The synchronous IP units communicate asynchronously on the network on chip. The synchronization between the IP blocks is done using a clock mechanism called Synchronous-to-Asynchronous and Asynchronous-to-Synchronous interfaces (SAS) mechanism and the IPs used is already designed for low power. Author proposed two new techniques for reducing the dynamic power consumption. One is the use of advanced integrated buck-boost inductive DC-DC converter and other locally adaptive voltage and frequency scaling (LAVFS) technique. For reducing the static power consumption, author applied PMOS power switches which are controlled by an ultra-cut-off (UCO) technique. These PMOS switches are inserted on each NoC unit for maintaining the minimum leakage in standby mode.

System Level Power Modeling: Author developed a way to use SystemC Transaction Level Modeling (TLM) platform for modeling power consumption. Upon considering both the statistic and dynamic power the model generates power traces, power/energy stats and an ALPIN power profile to drive the power management policy in accordance to the low power techniques at appropriate level of abstraction.

Power Mode Definition: Six different modes are used to transmit the data packets from nodes to nodes providing advantageous demarcation of the transmitting process.

Local Power Manager: The individual unit's power issues are taken care by the Local Power Manager (LPM) consisting of a set of programmable registers, programmed through NOC.

Local Pause-able Clock Generator: During synchronous-to-asynchronous (S-A), asynchronous-to-synchronous (A-S) data communications and during voltage transition, local Pause-able Clock Generator, individual IP core's clock generation unit, handle the concurrent request from either the A-S, S-A or LPM interfaces.

Power Supply Unit: It manages the individual unit's power requirements according to the selected power modes using supply voltages provided by off-chip DC-DC converters.

Technique 4: The power estimation model proposed by the author is meant for fixed function type SoCs using synchronous network technique and asynchronous router design. Authors have parameterized the technique in input terms namely: Source and destination cores, b-value in the range [0.5, 1.0) indicating burstiness, simulation duration, average bandwidth (i.e. desired total traffic volume), the smallest time-resolution of the burstiness and number of packets per message [2]. Authors design an asynchronous router for better efficiency and simplicity where the switch directs the flits to one of two ports via bidirectional channels resulting in T-router.A single flit containing source-routing bits in parallel on separate wires with the data bits forming the packet which are switched using DEMUXes controlled by the most significant routing bit. A special SoC design generates the hop count determining the number of routing bits. The flit width is determined depending upon the required throughput, power and area constraints. The proposed format has an overhead of routing bits with every flit.

Technique 5: The power estimation model proposed by the author forms a low-power NoC, designed and implemented for high-performance SoC applications for heterogeneous, IPs (such as multiprocessors, memories, FPGA) and off-chip gateway, with different timing references, interconnected in a hierarchical star topology. The authors proposed low power techniques in open system interconnection Layer, Low-swing serial link and source-synchronous schemes in physical layer and low-energy serial link coding in data-link layer for NoCs. Authors also used hierarchical circuit/packet switching, crossbar partial activation technique and Mux-Tree based round-robin scheduler techniques for reducing the power consumption in network layer [8].A brief discussion about the techniques used by the author is:

Low-Swing Signaling: Authors have shown that the differential low-swing signaling scheme and their transceiver circuit reduces the energy consumption.

Mux-Tree Based Round-Robin Scheduler: Authors used Round-robin algorithm as asynchronous transfer mode (ATM) switches and on-chip networks due to its fairness and lightness while implementing. They proposed new way of implementing this in 0.18 micron technology, using Tree based MUX achieving-high modularity and scalability in the process.

Crossbar Partial Activation Technique: To reduce the power consumption authors proposed a crossbar switch with crossbar partial activation technique (CPAT). Using this technique authors implemented a crossbar compared with traditional one attaining 22% power saving for 90% offered load, for 8x8 cross bar and 43% for 16x16 crossbar.

Low-Energy Coding on On-Chip Serial Link: As the serial communication dissipates more energy than the parallel communication so to reduce these, authors has reduced the number of transitions on the serial wire using a coding.

Technique 6: The power estimation model proposed by the author is meant for high level power estimation methodology for a NoC router enabling a cycle accurate power profile. The proposed semi-automated technique is based on the number of flits passing through a router as the unit of abstraction [3]. A high level power macro model for a router was created using multiple regression analysis. The proposed techniques can be summarized as follows:

Power Macro Model: Authors proposed a power macro model for a single router, containing variables, having a strong correlation to power consumption and regression coefficients.

Hierarchical Power Modeling: Authors proposed the use of hierarchical power characterization model for custom IP cores enabling a trade-off among power estimation, accuracy, modeling effort and estimation speed. They also analyzed the performance of the router at 100MHz at 90nm technology.

Multiple Regression Analysis: To increase the accuracy of the proposed power model authors evaluated a power macro model reflecting the contribution of different variables.

Technique 7: The power estimation model proposed by the author uses dynamic frequency scaling (DFS) link technique where the frequency is dynamically adjusted to minimize power dissipation while maintaining the performance demands. The proposed technique focuses on dynamic power consumption in NoCs. As the power dissipated is directly proportional to the frequency, therefore, authors are proposing to change the operating frequency at run time dynamically fulfilling the required performance of the system [9]. Authors proposed a clock boosting router adaptable to the variable frequency requirement by adapting the system clock frequency. The proposed mechanism provides variable frequency link and also increases the interconnection network performance.

The proposed system focuses upon the dynamic power consumption due to charging and discharging of the switched capacitances. The dynamic power consumptions depends upon 1) switching activity factor (α), 2) physical capacitance (C), 3) supply voltage (v) and 4) clock frequency (f), which can be depicted as follows:

$$P_D = \frac{1}{2}\alpha C V^2 f$$

$$f_{\max} = \eta\left(\frac{V - V_{th}}{V}\right)^{\beta}$$

The second equation provide the relationship between the supply voltage and the maximum operating frequency, where V_{th} is the threshold voltage, ç and â are experimentally defined constants.

The proposed system tries to predict the future workload (in terms of switching required) utilizing the previous history. To filter out the transient fluctuations from utilization and to predict future communication workload, history based DVS policy is used which uses exponential weighted average utilization. It uses the current-link $U_L(n)$ and past link utilization history $T_L(n-1)$; to predict the future link utilization $T_L(n)$. Where, weight (W, W+1) is the contribution factor of current link utilization level to the history-based link estimator.

The proposed algorithm shown below dynamically adapts its frequency aiming to conserve power at appropriate levels. It prescribes whether to increase, decrease the frequency or remain as it is. If the link utilization is higher then the threshold value ($T_L(n) \geq Pi_u$), the boosting clock frequency will be increased; on the

other hand if the link utilization falls below certain threshold value ($T_L(n) \leq Pi_l$), the boosting clock frequency is reduced. Otherwise it os kept unchanged.

Dynamic frequency scaling algorithm
while (DFS enable) do
$T_L(n) = (W \times U_L(n) + T_L(n-1)/(W+1)$
if $T_L(n) \geq Pi_u$ then
Increase boosting clock frequency
else if $T_L(n) \leq Pi_l$ then
Decrease boosting clock frequency
else maintain current boosting clock frequency
end if
end while

Technique 8: The power estimation model proposed by the author uses techniques in asynchronous switching for making low power network on chip. The authors have shown that by the use of asynchronous switching technique, there is increase in area byabout 50% but the power consumed is reduce by about 76% as compared to the synchronous implementation. They also reported that with the increase in number of IPs on the SoC the percentage reduction in power consumed increases. The increased area is meant to accommodate the handshaking modules and circuit elements for Globally Asynchronous Locally Synchronous (GALS) [4]. The network power is given by

$$P_{\text{network}} = N_p P_p + P_d + P_c + P_{\text{synchonization}}$$

where,N_p is total number of ports, P_p P_d P_c are power dissipation per port, data link and coupling capacitor. Synchronization is the total power dissipation by the synchronization network.

Technique 9: The power estimation model proposed by the author uses techniques of Serialization which helps in reducing coupling capacitance but it increases the router power. Authors have shown a knee point where thereis an increase in router power due to serialization [10].

Technique 10: The power estimation model proposed by the author uses two techniques namely, adaptive channel buffers; and router pipeline bypassing leading to reduced power consumption and improved performance simultaneously. They have used dual-function channel buffers where flits can be stored on wires, when required. On the other hand,by using Network bypassing technique, authors have shown the bypass process of the router-pipeline by flits and hence avoiding of the router buffers. A 62% power reduction is reported by the authors [11,12].

Adaptive Channel Buffers: Authors have used the different modules, router and repeater in a distinct manner to provide an adaptive configuration thereby reducing the power consumed.

Router Bypass Implementation: The proposed design based upon "per router bypass" can bypass any output port where the input port of crossbar allows flits to have both way linking within the router and the bypass paths simultaneously to two different ports. The proposed arrangement reduces the power consumption in NoC architecture.

Dynamically Allocated Router Buffers: These are design in such a ways that the throughput of the network is maximized without increasing the router latency.

Technique 11: Authors, through the proposed technique tried to reduce the static power targeting the different elements like buffers, switches, links and arbitration units comprehensively using the optimal power down scheme having certain boundaries for traffic patterns associating a holistic approach with them. The authors used PARSEC benchmark suite. Authors optimized the elements via downstream and upstream nodes containing input buffers, crossbar [13].Author have used virtual channel routers with 2 stages pipelined with 4 VC buffers for each input port, with matrix organization using nMOS pass transistors at cross-point as part of Segment Gating. They also used switch allocator with matrix arbiters for each level.

Technique 12: The authors have investigated non-local interconnect architecture aided by the complex network and optimization techniques using the power-law distance dependent wire-length distribution concepts. The used power evaluation mechanism- hardware model (implemented in VHDL) takes each nodes consisting of virtual channel buffers, switch buffers, multiplexers, de-multiplexers, virtual channel arbiters and a routing table. The authors synthesized the architecture for maximum 8 virtual channels, 100 buffers per channel and 16 I/O ports per node, increasing the step size of 10 using 65nm CMOS

technology in Synopsys Design Compiler and Synopsys Power Complier with switching activity of 0.5, source voltage 1 V, 500MHz frequency [14].

Author have used RC delay model for delay of unit distance of nano-wire, power dissipation for inter-connects and nodes, given by the following expressions:

Wire delay = [(0.5 R Per unit length) × (C per unit length) × (Unit length^2)]

$$P_{interconnect} = \left[0.5 \times (C\ per\ unit\ legth)\right] \times V_{dd}^2 \times (switching\ activity) \times \{1/unit\ wire\ dlay\} \times (total\ wire\ length)$$

Pnode = POWER (Buffer, Ports, Channels)

Author modifies the Network model by extending the simple power law model including the parameter *'p'* for randomness of the network or rewiring probability of regular ring in Watts-Strogatz model and 'alpha' parameter as proportion of non-local connections.

Authors have shown through their work, the cost effectiveness of power-law distance dependent wire-length distribution concepts, embedded with small world network and compared with simple small-world topologies, maintaining the same transport characteristics via occupying optimal spots in NOCs design space with better navigability. Hence they showed efficiency of their concept over the original Watts-Strogatz small world model, making it very important for power efficient green computing network and SOC for mass production.

Technique 13: The authors have investigated the NoC architectures partitioned into different voltage frequency domain. The author proposes a novel control algorithm/ methodology for on-the-fly workload monitoring and management which is also capable of handling the parameter-variability for technology and loading changes of the system. The proposed algorithm is dynamic in nature, controlling the different operations of different voltage frequency islands there-by reducing the overall power of the system as guaranteed by the authors with support of their work with some area overheads [15]. They validated the same in 45nm CMOS technology from STMicroelectronics on MIPS R2000 processor node.

Authors have also designed GALS based NoC architecture targeting the CMOS technology, based on asynchronous programmable self timed ring "PSTR" design controller, controlling the dynamic workload and the process variability effects.

Process Variability Robust DVFS GALS-NoC Architecture: Authors proposed new architecture for each voltage frequency islands in the GALS- NoC system which assists in the modeling DVFS as well as local process quality management.

The Speed Sensor: Calculates the real time speed of the processing node.

- Activity monitor-Used to locally evaluate the process quality w.r.t. speed of other nodes
- DC - DC Converter- used for providing the supply voltage
- Asynchronous Programmable Ring-used for generating the desired clock frequency for each local processing node.
- Digital controller-used for managing voltage/ frequency couple for addressing the error between unit speed and speed information extracted from Operating System (OS) within the closed loop system.
- Using the compensator, the system send the required voltage and frequency coded values to the DC-DC converter and clock generator enabling the smooth adaptation for the same. This makes the Asynchronous NoC a reliable communication path.
- The authors have also explored the feedback control techniques (namely Start up regulation techniques and On-line tracking technique) for improving the performance.
- DVFS Control Technique-Authors have used the third party energy efficient algorithm, with two voltage levels as:

$$V_{level} = \{V_{high}, V_{low}\}$$

with three different frequency levels $F_{level} = \{F_{high}, F_{low1}, F_{low2}\}$, where F_{high} and F_{low1} are the maximum possible frequencies at V_{high} and V_{low} respectively, while $F_{low1} > F_{low2}$ and splitting the task into two time intervals. First, (which is need based),running the system at V_{high} and F_{high} for attaining maximum possible speed. Second,completing the task in hand,using the required lower voltage and frequency values. Thisstepped procedure enables the reduction in power consumption of the system.

PSTR Programmability: Authors have explored the benefits of using a programmable stoppable oscillator (PSO) in the clock generation system in the GALS-NoC DVFS system. Through this they are able to provide

adaptation capability to the generated clock in terms of its frequency w.r.t. the current located process variability impact and load. Authors have defined three process variability corners(best, normal and worst) and split the PSO code memory into three main pages providing selection of the pages based upon the activity.

Authors have given a robust architecture based on PSTR. The architecture is adaptable with maximum clock frequency, operating voltage and work-loading with small area overhead.

Technique 14: Authors have presented a new architecture for data and control planes via nano-photonic network-on-chip NoC with scalability (to large scale networks), constant node degree and simple in nature as its advantages. The authors have also proposed new minimal deterministic routing algorithm for data network leading to small and simple photonic switch. They proposed a new novel topology as base for all-optical NoC called 2D-HERT (Two Dimensional Hierarchical Expansion of Ring Topology). 2D-HERT provides passive routing of data streams based on the wavelengths using the Wavelength division Multiplexing (WDM) technique along with the new proposed architecture eliminates the requirement of optical resource reservation at intermediate nodes. It also eliminates the latency and area overheads. Authors, have shown, reduction in data transmission-delay by 18%, 4% and 70% with average per-packet power reduction of 53%, 45% and 95% over optical crossbar, router and electrical Torus, respectively [16].

The proposed architecture uses physical properties of light transmission for routing data streams through photonic switching elements fulfilling the regularity, scalability, constant node degree and simplicity concepts. The new techniques using the wavelength routing method proposes the control packet architecture where the modulation wavelength of the control packet depends on the corresponding transmitter. The proposed 2D-HERT technology uses locally connected optical rings for the cluster of processing cores interconnected hierarchically via 2D rings with 64 optical routers.

Routing Algorithm-Authors have proposed a deterministic Circular first Routing (CR) routing algorithm for the 2D-HERTarchitecture where from source to destination node, circular links traversed first till the destination, followed by radial links via destination to reach target super-node.

All optical Router architecture- Authors have proposed a passive optical switch called WaROS (Wavelength-Routed Optical Switch), using Optical add/drop (OAD) filters for optical wavelength to form the optical transmission stream without any electronic processing.

The WaROS micro architecture contain 4x4 optical switches, interconnects for local IPs and adjacent super node. The proposed architecture is partitioned into two groups for radial and circular switches leading to different architecture as per the CR routing scheme utilizing injection ports and ejection channels.

The proposed architecture limits number of concurrent data received by WaROS to the number of wavelength sets dedicated to the router.

Authors have analyzed the architecture on a 64-node topology with four diagonals, each with four local clusters of four processing cores and targeting the 22nm CMOS technology, 5-Ghz frequency. They have shown improvement in latency by 2.5 and 13 times in low and high traffic network respectively. The Power equationsare:

$$P_{\text{ink}} = P_{CV} + P_{W} + P_{S} + P_{WC} + P_{V} + P_{CR}$$

where, P_{CV} is the coupling coefficient between the photonic source and optical waveguide, P_{W} is the waveguide propagation loss per unit distance, P_{B} is the bending loss, P_{WC} represents waveguide crossing insertion loss, P_{Y} is the Y-coupler loss and $P_{CR}$is the coupling loss from the waveguide to the optical receiver.

$$P_{\text{oprical, data}} = P_{\text{M,R, drop}}\, x\, N_{\text{on}} + P_{\text{MR, through}}\, x\, N_{\text{oFF}} + P_{\text{w}} x (\text{L}_1 x hop\ Count_1 + \text{L}_s\, x\, hop\ Counts) + P_{\text{wC}}\, x\, N_{\text{wc}} + P_{\text{Y}}\, x\, N_{\text{Y}} + P_{\text{CV}} + P_{\text{CR}} + \text{WDM}\, x\, (P_{\text{transmitter}} + P_{\text{Receiver}})$$

Where, N_{ON} and N_{OFF} are the number of 'activated' and 'off' resonance micro-ring resonators passed by the optical message, respectively, L_l and $L_s$are inter and intra super-node optical link lengths (approximately 1.5 and 0.5mm respectively), HopCount_l and HopCount_s are the number of long hops and short hops (intra super-node hops) passed by the optical message, N_{WC} and N_{Y}represents numberof waveguide crossings and Y-couplers passed by the optical message, respectively, W_{DM} is the number of wavelength channels on which corresponding optical data is modulated.

$$P_{\text{optical, Control}} = *(P_{\text{w}} x L_{\text{CW}} + P_{\text{CV}} + P_{\text{CR}} + P_{\text{WC}}\, x\, N_{\text{WC}} + WDM_{\text{CU}}\, x\, (P_{\text{transmitter}} + mx P_{\text{receiver}}))$$

Where, L_{CW} represents length of the optical control waveguide, WDM_{CU} is the number of modulation wavelengths for each optical control packet and 'm' is the

number of control units located on each diagonal. Authors reported a per packet power reduction of 53%, 45% and 95% over optical crossbar, router and electrical Torus systems respectively.

Technique 15: The authors have proposed a power aware selection policy for increasing the performance and power efficiency of a NoC.

Routing algorithm consists of two main functions, routing function and the selection function.The routing function computes all the admissible output ports where the packet can be forwarded towards the destination and on the other hand the selection function selects one output port from thechosen set of admissible output ports. A selection block is not required for a router with deterministic routing algorithm as routing function returns a single output port only. Among these components the authors investigated the selection function enhancing the effectiveness of a routing algorithm with the methodology of power reduction in the system [17]. The proposed algorithm for selection function is:

```
Out put Portselection Function (set<OutputPort>oports,
TFlithflit)
{
if (oports.size()=1)
Oport<- oports[0];
else if (AllReserved(oports) || Nonereserved(oports))
Oport<- SelectionMinpower (oports, hflit);
else
Oport<- selectionMinBuffer (oports);
Return oport;
}
```

The Authors have provided the provision for calculating the power dissipation in all selected / admissible output ports in the selection function itself and then transmits the data via the router chain where the associated power dissipation is least.

The dynamic power dissipated by the link can be given as :

$$P_1 = \left[T_{0\to1}\left(C_s + C_1\right) + T_C C_c\right] V_{dd}^2 F_{clk}$$

Where, V_{dd} is supply voltage, $F_{ck}$is clock frequency, C_s isself capacitance, C_l is load capacitance and Cc is coupling capacitance. $T_{0=>1}$ and T_c are average number of effective transitions per cycle for C_s and C_c respectively. $T_{0=>1}$ counts the number of 0 to 1 transitions in the link in two consecutive transmissions. T_c counts the correlated switching between physically adjacent lines. The coupling transition activity T_c is a weighted sum of the different type of coupling transition contributions as follows:

$$T_c = k_1T_1 + k_2T_2 + k_3,T_3 + k_4,T_4$$

Where the $T_i(i=1,2,3,4)$ are average number of transition and k_i represents the corresponding weights. Author assumed $k_1 = 1$, $k_2 = 2$, $k_3 = k_4 = 0$ and $C_c/C_s = 4$.

Authors have reported a 17% improvement in power with proposed methodology as compared to *XY* and *OE-BL* system for uniform traffic and 20% and 18% improvement in case of transpose traffic with hardware (router with proposed selection procedure) of 3% and 1% larger as compared to with *XY* and *OE-BL*.

Technique 16: Authors have proposed an OCP compliant hardware design for reducing power in 2D mesh NoC targeting the network interface power with the use of stoppable clock technique enabling to shut down the modules which are not required at that particular instant.

They have proposed architecture based on the identification of the key issues of NI design which is designed as a bridge between OCP interface and the NoC switching, synchronizing the IP, OCP and NoC timings, the packetization of OCP transactions into NoC flits and vice versa, the computation of routing information and the buffering of flits. The proposed architecture comply to 2.2 version of the OCP specifications and provide read/write-style transactions for a distributed shared address space providing the support forsingle reads and writes, burst precise (BP) reads and writes [18].

Interface architecture -This is designed for 4-master OCP based network interface MNI cores where each MNI are split into 2-sub module for request and response channel which are loosely coupled i.e. whenever a transaction requiring a response is processed by the request channel, the response channel can be notified; whenever the response is received, the request channel can be unblocked.

Master Network Adapter: Upon receiving the request from the master, it encapsulate the package, allows packet transmission to network, handle receipt for it and response de-capsulation and transmission to the master core.

The proposed architecture has two separate parts, Module Adapter (MA) and Channel Adapter (CA), interconnected via internal bus (IB). The proposed

architecture shows improvement of 63% and 37% in power rating for handshake and credit based control flow with area overhead of 19% and 2% and with reduction in maximum frequency by 21%.

Technique 17: Authors have proposed a multi-objective ant colony algorithm (MOACA) for mapping IP-cores onto 2D mesh-based NoCArchitectures as an efficient alternative for the pareto-optimal front optimizing the energy consumption and hotspot temperature of NoC.

Multi objective ANT Colony algorithm- Authors have proposed a way out methodology for balancing the two objectives of minimizing energy consumption and hotspot temperature having negative impact on each other using multi-objective ant colony algorithm (MOACA) for solving the mapping problem [19]. The algorithm can be depicted as follows:

The proposed algorithm uses the concepts of max-min ant system scheme where at the start an ant colony is constructed and every ant construct a solution of each cycle and attain the optimized solution with two heuristic functions, for minimizing energy consumption and hotspot temperature.

The probability of c_i mapped to tile n_j for objective n can be calculated as:

$$P_k^n(ij) = \begin{cases} \dfrac{\left[\sum_{h=1}^{2} \tau_{ij}^h\right] \times \left[\eta_{ij}^n\right]^\beta}{\sum_0 uellowedk \left(\left[\sum_{h=1}^{2} \tau_{iu}^h\right] \alpha \left[\eta_{iu}^n\right]^\beta\right)} & if\ j\ allowed_k \\ else \end{cases}$$

where,$p_k^n(ij)$ is the probability of ant k for minimizing energy consumption, allowed$k$ is a set of feasible tiles currently not be mapped. For local pheromone update, the pheromone can be calculated as follows:

$$\tau_{ij}^1 = (1-\rho_0).\tau_{ij}^1 + \rho_0.\Delta\tau_{ij}^1$$

$$\tau_{ij}^2 = (1-\rho_0).\tau_{ij}^2 + \rho_0.\Delta\tau_{ij}^2$$

Global pheromone is also updated once all ants have constructed a solution. For global pheromone update, the

Pheromone for best solution can be calculated as follow:

$$\tau_{ij}^1 = (1-\rho_1).\tau_{ij}^1 + \rho_1.\Delta\tau_{ij}^{'1}$$

$$\tau_{ij}^2 = (1-\rho_1).\tau_{ij}^2 + \rho_1.\Delta\tau_{ij}^{'2}$$

Authors have reported experiments carried out on synthesizer *traf_c* and reported improvement in the efficiency, accuracy and scalability of the proposed architecture/ methodology.

Technique 18: The authors have proposed a highly flexible, scalable network design and SoPC (System on a Programmable Chip) design based on multi-core embedded system in which they used a novel dynamically reconfigurable accelerator cores along with the conventional processor cores improving the performance and made a prototype using FPGA and Altera SoPC Builder [20]. The developed NOC use power aware topology algorithm aiming to improve the power and performance with parallel computing capability, leading to larger on chip bandwidth and reduces routing congestion. The developed multi-core system uses two CPU cores, individually optimized for computational characteristics of different application fields, complementing each other to deliver high performance levels with high flexibility at reduced cost.

Technique 19: The authors have proposed the data encoding techniques for reducing the power dissipation and energy consumption of the NOCs which uses the wormhole switching techniques working on end to end bases. In the proposed system flits before putting onto the communication network are encoded and then decoded at the destination NI making the system transparent to the underlying network as the used encoders and decoders are integrated in the NI hence eliminating any need to modify the network / router architecture [21].

As the links dissipates the power due to switching activity as per the data patterns in the communication network, authors focused on the network links and the data encoding techniques aiming to reduce the switching activity of the links, exploiting the pipeline nature of the wormhole switching technique providing capability of end to end encoding and decoding scheme.

Proposed Encoding Scheme- The dynamic power consumed by the interconnects and drivers is given by

$$P = \left[T_{0-1}(C_s + C_l) + T_C C_C\right] V_{dd}^2 F_{clk}$$

Where, V_{dd} is supply voltage, F_{clk} is the clock frequency, C_s is the self capacitance (which includes the parallel-plate capacitance and the fringe capacitance), C_l is the load

capacitance and C_c is the coupling capacitance. $T_{0\to1}$ and T_c are the average number of effective transitions per cycle for C_s and C_c, respectively.

The coupling transition activity T_c is a weighted sum of the different type of coupling transition contributions and can be give as :

$$T_C = (k_1T_1 + k_2T_2 + k_3T_3 + k_4T_4)$$

Where, T_i, = *1, 2, 3, 4,* are the average number of transition k_i are corresponding weights and the assumption made is k_1 = *1,* k_2 = *2 and* $k_3 = k_4 = 0$. That is, k_1 is assumed as reference for other types of transition and therefore the combined equation can be depicted as follows:

$$P \propto T_{0-1}C_S + (k_1T_1 + k_2T_2 + k_3T_3 + k_4T_4)C_C$$

Authors have compared the proposed scheme with different schemes using data streams both synthetic and extracted from real applications and shown that the proposed scheme has reduced the power dissipation by 18% with minimal or ignorable overheads of area and performance.

Technique 20: The authors have proposed a Simulated Annealing with Timing Adjustment (SA-TA) heuristic techniques for system optimization and also extend the Integer Linear programming (IPL) formulation and developed an algorithm for efficient computation of the system wide energy optimal task allocation for heterogeneous MPSoC system [22].

Heuristic algorithm-As with increasing complexity, the computational complexity of the ILP grows rapidly hence authors tried to propose efficient, scalable heuristic algorithm given as under:

```
//Algorithm SA-TA Heuristic Algorithm
//input task graph TG, architecture graph AG
Procedure TaskAllocation (TG, AG)
Step <- 0,T<- T0
Pi= baselineMapping ()
Pi_opt<- Pi, E_opt = computeEnergy(Pi)
While i<N do
    Pi'= neighbor (Pi)
    E=computeEnergy(Pi)
    E'=computeEnergy(Pi')
    If E'<E then
        Pi <- Pi', E<- E'
    Pi_ta= timingAdjustment (Pi')
    E_ta=computeEnergy(Pi_ta)
    If isFeasible(Pi_ta) and E_ta< E_opt then
            Pi _opt<- Pi_ta, E_opt<- E_ta
            endif
    else
            if P(E,E',T) > random () then
            Pi <- Pi', E<- E'
            endif
            endif
            T<- kT, i<- i+1
            end while
            Return: Pi_opt, E_opt
            end procedure
```

The task with highest desirability t_y is first assigned to a processor p_y with lowest processing energy (the preferred type). In case of multiple processors, the processor able to minimize the cost function is to be taken. The next task in the pipeline (denoted by t_i) is allocated to the processor having enough resources enabling minimization of total energy considering the communication with tasksmapped previously. This procedure is done until all tasks are allocated.

Timing Adjustment-For obtaining the timings authors used a level based list scheduling algorithm for scheduling the task graph for exploring the search space near an accepted mapping to find a feasible mapping that minimizes the parameters involved.

The proposed energy aware technique improves the power associated via computing global optimal mapping, but has to trade off in terms of large execution time.

The authors have reported that proposed techniques using SA-TA algorithm attains global optimum even in tight timing constraints (less than 5% above global optimum using 1000-iteration SA-TA) and reduction in the mean time.

CONCLUSION

Through exhaustive literature survey the investigation has shown a need for efficient power reduction technique in NoC design. We have presented power model for estimating and reducing the energy and power in the NoC. We have also discussed various levels where power can be reduced. We also found that the lowest level of abstraction is the gate level which

represents the model at transistor level. The model at this level are generally most accurate model as they consider the lowest element in the design i.e. the transistor, but these are very time and resource consuming models. The main sources of power dissipation in NoC are buffers, control logic section and crossbar section. Buffers power consumption is mainly due to large amount of switching activity in the clock signal and in the stored value and are considered most significant part around 88% of the power dissipation. From the study of different techniques we observed that for power efficient implementation of NoC both the static and dynamic source of energy is to be dealt comprehensively. It is also observed that the techniques are one way or another way application and constraints dependent. The generalized techniques and NoC architecture for power and energy efficient implementation is not much developed and a lot of gaps and elements are open for investigation. For developing and maturing any single generalized low cost, energy efficient technique which can be used for most of the applications if not all, a holistic, probabilistic approach need to be developed.

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