World Applied Sciences Journal 14 (9): 1374-1383, 2011
ISSN 1818-4952

Online-Structural Testing of Routers in Network on Chip

[1]Shahram Babaei, [1]Mansour Mansouri, [2]Babak Aghaei and [3]A. Khadem-zadeh

[1]Department of Computer Engineering, Tabriz Branch, Islamic Azad University, Tabriz, Iran
[2]Department of Computer Engineering, Malekan Branch, Islamic Azad University, Malekan, Iran
[3]Iran Telecommunication Research Center, ITRC, Tehran, Iran

Abstract: The routers are one of the critical components of Network on chip. Occurrence a failure in them causes crucial effects on communication of cores and reliability of NoC. In this paper we will propose a test wrapper for routers that testing the routers online and structurally. The proposed wrapper simulated and the results captured and showed in waveform figures.

Key words: Network on chip · Router · Test wrapper · Online testing · Structural testing

INTRODUCTION

Transistors, the basic composing elements of chips, are decreasing in size and increasing in number. This is demonstrated by the Moore's law in 1965. The Moore's law states that every 18 month the number of transistors and thus hardware blocks doubles on the chip. Due to this incident the density of transistors and hardware blocks are increasing on the chip exponentially. This caused to forming a complete system on a chip that called System on Chip (SoC). As a consequence, in today's chip design, communication between on-chip cores is becoming more expensive than on-chip computation [1]. In other words, providing an interconnect system for the chip is becoming more costly than on-chip blocks. Therefore, the designers has proposed to exchange the conventional on-chip interconnect system (buses) with a new on-chip interconnect, named as Network on Chips (NoC). NoC architecture is composed of routers, Network Interfaces (NI) and links. Links connect the routers together and also the routers to the NIs. Network interfaces are placed between a router and an IP core and is used as a mediator between IP cores and the interconnect network. Routers are responsible for routing data units of transmission from source to destination. Figure 1 shows the general architecture of NoC.

Routers or Switches consist of a combinational circuit for routing packets (referred to as Routing Logic Block (RLB)) and input/output ports. RLB connects the input ports to the proper output ports. Depending on the routing scheme, routers may or may not have buffers.

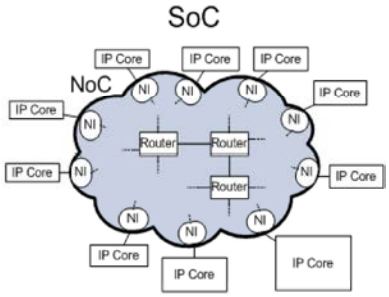

Fig. 1: General architecture of NoC

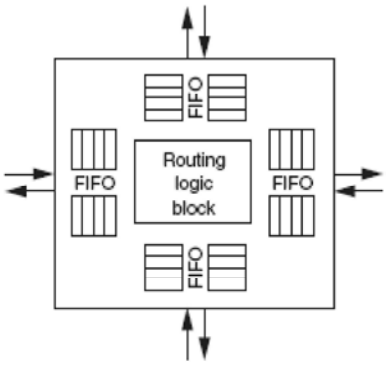

Fig. 2: Router architecture containing buffers [2]

Figure 2 depicts block diagram of a router containing buffers.

The way routers are connected to each other is defined by network's topology. However in irregular topologies there are less control on physical issues, instead it is more efficient in resource usage [3]. Different topologies for NoCs trade off between various characteristics of NoC such as performance, reliability

Corresponding Author: Shahram Babaei, Department of Computer Engineering, Tabriz Branch, Islamic Azad University, Tabriz, Iran. E-mail: hw.tab.au@gmail.com.

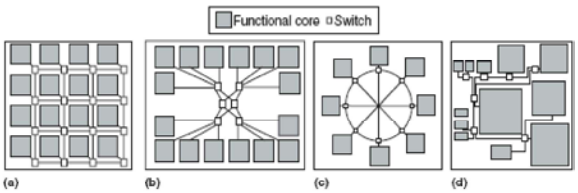

Fig. 3: NoC regular and irregular topologies [2]: Mesh-based (a), Buttery fat-tree (b), Octagon(c), Irregular application-specific (d)

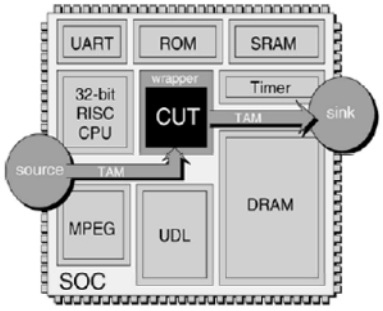

Fig. 4: General test architecture for embedded cores [8]

(QoS), work conservatism, power dissipation and silicon area [2]. Topologies for NoC can be regular like Mesh [4], Buttery fat-tree [5] and Octagon [6] as shown in Figure 2a and 2b and 2c, or it can be a irregular application-specific NoC [7], depicted in Figure 2d.

Special characteristics of NoC (such as scalability, being modular, exibility, etc) make it a perfect choice for today's on-chip communication. But, because of critical responsibility of NoC in today's chips, its testing becomes a crucial task.

SoC testing has two separate parts; testing the existing cores on SoC and testing the interconnect structure that is responsible for connection between cores. Testing the interconnect structure of the system compromises of testing the on-chip interconnection which is either the bus system or the NoC. Since the cores on the SoC are deeply embedded, direct accessing to their I/O pins from the I/O pins of the chip is not possible. Therefore one of the main challenges of testing the cores is to transfer the test data from test generator to the inputs of the core-under-test and also from its output to the response analyzer. This issue can be addressed either by using a dedicated Test Access Mechanism (TAM) or by reusing the on-chip interconnect which is either bus system or NoC.

For embedded core testing, general test architecture is proposed [8-10]. As depicted in Figure 4 This architecture is composed of:

Source: It generates test patterns and can be on-chip or chip. It is also called Test Pattern Generator (TPG).

Sink: It analyzes the test responses and can be on-chip or chip. It is also called Test Response Analyzer (TRA).

TAM: It is responsible for transferring test data from the source to the input of the core-under-test and also from the core-under-test output to the sink. It increases controllability and observability for testing embedded cores.

Wrapper: It covers the core-under-test in order to connect the TAM ports to core-under-test ports. The wrapper is also responsible to switch the router's (The circuit-under-test) operational mode, between test-mode and functional-mode.

In order to test NoC, its three main components (routers, network interfaces and links) have to be tested. Since routers have a critical responsibility in NoC's functionality, in this paper the focus is on router testing. Routers of a NoC can be seen as on-chip cores. Therefore, the same style as that for embedded core testing can be reused to test NoC routers. In order to test an embedded core on the chip, special test architecture should be used. This test architecture is composed of test generator, test analyzer, a mechanism to transport test data to/from the embedded core and a wrapper around the core-under-test.

State of the art methods for testing the routers of NoC use this test architecture for testing routers. From different aspects of testing, testing NoC can be done either functional versus structural or online versus offline. Online testing a device makes it possible to test the device without interrupting its normal functionality. Structural testing, gives us the opportunity to locate the exact place of defect. State of the art methods of NoC testing are using offline-structural or online-functional testing. However, due to the critical responsibility of NoC and its special characteristics, online-structural testing is a promising test method in NoC. In addition to being tested online and without interruption of on-chip connection, it is possible to localize the faults for diagnosis.

Considering to router architecture (depicted in figure 2), different types of faults can happen in combinational logic part and in buffer part of the router. The faults that may occur in combinational logic part are stuck at faults, short/open, the faults related to crosstalk. The faults that are possible to occur in buffers can be due to SEU errors and cause bit corruption in the buffers.

Since errors with different roots may occur in different parts of the router, there should exist specific test pattern to detect each type of fault in the routers. This is the responsibility of the TPG to take care of generating an appropriate test pattern. To stimulate the possible faults that may occur in the router. When appropriate test patterns are prepared, there should exist an appropriate architecture to transport these test patterns to the router-under-test.

In this paper, we focus on the testing of routers. We propose a wrapper for routers that it can to test the routers online and structurally. TPG and TRA are in wrapper and TAM mechanism is bringing to wrapper. Advantage of this wrapper is low packet traffic and high reliability and creation the routing algorithms that is power-efficient. The rest of paper organized as follows; in section 2 we discus about previous work. Our works and advantages and disadvantages of our work are appearing in section 3. Simulation and results bring in section 4. Finally, section 5 concludes the paper.

Related Works: There are quite a large number of papers about techniques used for testing cores in SoCs. In [11, 12, 13], the authors propose the use of NoC as TAM and they have designed a special wrapper to be used with NoC as TAM. Current literatures for router testing consider routers as the on-chip cores on SoC and use the general architecture for embedded core testing in SoC (source, sink, TAM and wrapper). Each of previous works done for router testing proposes architecture for the TAM, for the wrapper or for both of them. There are two types of works done in this respect. One group of works is using a dedicated access mechanism for TAM and the other group is reusing the NoC for TAM. Each of this group of works is explained below.

Dedicated TAM: One of the first works done for router testing is [14]. They use IEEE 1149 boundary scan standard (JTAG standard) in order to transfer test data in router ports and as wrapper for a group of routers-under-test. All routers are full scan. In this way, the full scan provides test access to inside of the routers. In this method, first routers are grouped. Each group of routers have the same test block which consist of a Test Access Port (TAP) controller, boundary scan register, instruction register and other necessary logics (e.g. for decoding the instructions). All of these parts are components used in IEEE 1146 boundary scan standard. However by having more routers in each group, in case of test failure, it is harder to find which router is exactly faulty. The main drawback of this approach is long test time. This means, for a long time the NoC can not be in functional mode and can not be used in application. Moreover, they are adding extra hardware for TAM, which is hardware overhead for system.

In [15], the authors propose to use partial scan for each router and a single modified IEEE 1500 standard as wrapper for the whole NoC. In this method, they have used a single wrapper that covers the whole NoC, but at the same time they provide test access from network interface to inside structure (buffers and flip-flops) of each router by having partial scan chains. In [15], In case of test failure each router can be tested independently and test data will be distributed among them. The modification they did in the wrapper leads to reduction of area overhead and test time (by reduction in the number of shift operations.). The drawback of the proposed method in [15] is that for large scale NoCs that have large number of routers, the fan-out of input pins and scan input pins become large. Moreover there is no method given as TAM for transferring data from source (test pattern generator) to input of network interface and the test is offline.

NoC reused as TAM: In [16], they propose to reuse NoC as TAM for transferring test data to its own routers. For this reason they assume that the links between routers and network interfaces are tested before and they are fault free. In this method, they group routers based on their accessibility via the input ports of the chip in an ascending order in a way that the routers that are closer to the input ports of the chip has the smaller order number. They start testing routers with the smallest order number in each step. The routers in the same group can be tested in parallel. In this way, they are assured about the TAM they are using for transferring test data to router-under-test. The wrapper used in this method is IEEE 1500 that covers each router and the connected core to it. The wrapper can configure each router or each core connected to it, to test mode or functional mode. If the router is in the way of transferring a test vector to a router-under-test (or core-under-test), it will be in functional mode and if it has to be tested, it is in test mode. The method they used for test response analysis is on-chip comparator which compares the responses of the routers that are in the same group of order number. However they do not provide information about the comparator that when a test failure occurs, it can be used for diagnosis of the exact router that is faulty. Using this method for TAM leads to reduction of hardware

overhead, test time (due to using high bandwidth channel and parallel communication of NoC for transferring test data) and number of additional pins in comparison to dedicated TAM like boundary scan, as it was used in [14]. However, in this work they do not consider buffer testing of routers that need additional scan chains to be tested and they only talk about combinational logic part of the routers. Moreover, the test is not done online. When the routers are being tested they are not used anymore for transferring functional packets.

In [9], method for testing an asynchronous NoC is proposed. They reuse NoC as TAM and they employ a modified version of IEEE 1500 as wrapper for routers. In asynchronous NoC, routers might be in different clock domains. For this reason they propose that each router has its own wrappers which are asynchronous to each other. Hence, they have to modify the IEEE 1500 for having handshake signals. In this architecture they introduce another unit, named as Generator-Analyzer-Controller (GAC), which plays the role of source (TPG) and sink (TRA). It can be off-chip or on-chip. Additionally, it has the role of controlling and configuration of asynchronous wrappers. Extra components that they have used in their method are additional channels that transfer the data needed to configure the wrappers by GAC. It should be noticed that, in addition to testing inter-router links, first it is needed to test the configuration channels as well. This is an overhead in test time. This method is similar to the method proposed in [16] that is for synchronous NoCs.

In [17], they propose to reuse NoC as TAM for full scan chained routers. They have proposed a special design for the wrapper that covers each router. The main idea of the method is reusing NoC to transport test data to routers. For this reason, if we consider the network of routers as a graph, the first node that should receive the test vectors from source should be defined. For this reason, they find the router by employing Dijxtra algorithm in the network that has the shortest path to all other of the routers, the so called topological center. When test vector is inserted in the topological center router, it sends the test vector to its own scan chain and also broadcasts it to the next available group of routers. In addition it sends its test response to the next group of routers, so they can compare it with their own responses. All routers repeat this procedure except boundary routers. For realizing this method special wrapper is designed. This wrapper has scan chains for input and output ports of the router, controller and comparator. This is comparable to the method proposed in [16] that they also reused NoC for transferring test data to the routers. However, in [15] the nearest routers to inputs of the chip (that are from boundary routers) are the first receivers of the test data. The advantages of method [17] over [16] are that it is independent of the NoC topology and the test time is less since the test data is inserted to the topological center of the NoC. The disadvantage compared to [16] is larger hardware overhead in the wrapper in comparison to IEEE 1500 which is mainly due to scan register in the input and the output ports of the routers. In this method also, when routers are being tested the NoC can not be used to transfer normal functional packets. Therefore the test is offline.

In [18], they target both combinational logic part of router and testing of buffers in routers. For combinational logic test, they use off-chip source from an ATE machine and they propose reusing of NoC as TAM as in [17] and [16]. They use one boundary router to insert test data to NoC. They propose to compare the results of the routers, so there is no need for off-chip or on-chip response analysis. For testing buffer part, they use full scan and they propose a special march test based on possible faults that may occur in the buffers. The BIST architecture that they use for buffer testing is composed of a shared source and controller for the buffers in all routers and a local response analyzer (sink) for each router that at the end they are derived by a MISR to produce a signature to be analyzed. The reason they used the distributed response analyzer is that it has a smaller area overhead than the centralized response analyzer.

All of the methods discussed above for router testing are structural, since test vectors are being sent to the special part of the router to stimulate the possible faults in those parts and check if they behave faulty or not. In terms of online or offline, methods discussed above are doing router testing offline since while the routers are being tested they can not be used for their normal operation which is routing data packets in NoC. Therefore testing the NoC would be offline. In [19], a new platform is proposed to do online-structural test on NoC. The authors claim that theirs proposed platform helps the system developers with online detection and localization of the errors that may occur in routers. Therefore, it increases NoC's reliability. In this platform, the idle routers of NoC are being tested while the rest of the routers are providing on-chip communication. For testing the router the standard test architecture for testing embedded cores (Test-Access-Mechanism (TAM), wrapper, source and sink) is used. In this architecture it is assumed that source and sink are given. The main contribution of [19] is to

design the wrapper element in such a way that it can be used in the proposed online-structural test platform and reuse NoC as TAM. Their thought is that the limitation of the proposed method is that the number of routers that can be tested at the same time without interrupting NoC's normal functionality depends on topology and size of the NoC. The major cost of this test methods, is related to the wrapper architecture. However, in their proposed platform, idle routers will be tested but we think it imposition great packet traffic to network on chip. In addition, if in the core that is connected to TAM a failure occurs, then test packets could not release in NoC.

So, that we propose a mechanism that solve the problems that are in [19]. We think if we bring the TPG and TRA units inside of wrapper then we could reduce meaningful of NoC traffic and we don't carry about that if in a wrapper or in a core that connected to TAM a failure occurs we can't to testing overall of Network on Chip. Our proposal has imposition great overhead to network butt in application that need to high reliability we can use this NoC.

Proposed Mechanism: In NoC-based systems, NoC have a crucial role in core communications. Due to its specific structure, it is exposed to many faults. This problem will be highlighted when NoC is utilized in the applications that require the capability of high level of reliability and tolerance. Therefore, in order to solve this problem, the researchers proposed a mechanism that increases the chips' reliability and tolerance with determining the exact place of the faults utilizing substituted ingredients. On the other hand, it decreases the packet traffic in NoC. In contrast to previous mechanism in which TAM was placed on the outside of the routers, in the present mechanism, TAM will be located into the wrappers which surround the routers. In this way, some functions such as test pattern generation (TPG) and test response analysis (TRA) will be done inside the wrappers. If necessary the generated patterns will be sent to the router and the responses will be received. Finally the wrapper will be advertised the destruction or authenticity of the router to an adjacent router or an external tester. Figure 5 demonstrates the proposed mechanism in NoC-based Mesh technology.

According to this mechanism, a router can be examined in three steps:

- Preliminary step
- On demand step
- Idle step

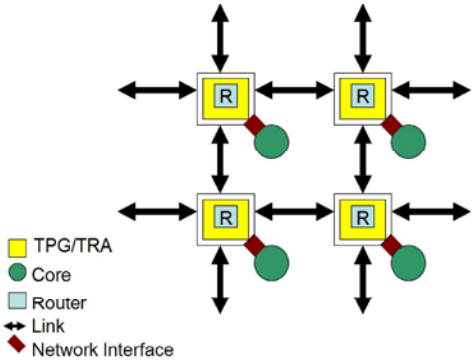

Fig. 5: Proposed mechanism in network on chip

Preliminary Step: This step begins whenever the system on the router (soc) has been reset. In this step, the wrapper begins to test the router as soon as the restart pulse received. To do so, first, it sends a package to the adjacent routers in order to recognize that this router is under the experiment and it could not receive any package. At the end of the experiment, the wrapper sends a package to the adjacent routers which reports whether this router is authentic or destructive. This package is called state package. After sending the state package, the router will continue its normal function.

On Demand Step: At the end of the first step, when the router returned to its normal function, the second step will start its special performance. When the tester or network manager is going to a test a specific router, it will send its request with the title of address of that specific router towards the defined router. After receiving this package, the router will recognize that it should start the testing operation. Therefore it will send a message to the adjacent routers to announce that the testing operation is going to be started. As well as the first step, the wrapper begins testing. The major reason for sending a package to the adjacent routers by the under-testing router is to advertise that they are not allowed to send any message to the under-testing router. Finally, the wrapper will provide the state package and will send it to the tester or network manager.

Idle Step: This step will be run when the router stays idle. The idle router is a kind of router in which there is no package in its buffers. As the buffer becomes empty, a timer will be activated. Although there is a package into the router in order to be routed, after a definite time, the wrapper will begin to test the router. The format of testing is as like as the first and the second steps. If the numerator did not get to the determined amount and if any package entered into router, the numerator is reset again.

The preliminary step and the idle step are online testing because NoC continues its normal function at the moment of running the test. But the on demand step is an offline testing, since the tested router is put away from the network for a determined time.

The advantages and disadvantages of the proposed mechanism are:

Extraordinary in Creasing in Reliability: The tested routes and the destructed routers will be recognized individually at different moments or times.

Increasing in Fault-Tolerance of Network: If a router was recognized as defective, the network will be able to continue its function by utilizing the replaced routers as well as the accessorial routers.

Low Packet Traffic in NoC: Unlike the previous methods, there is only on type of the package. Since the testing patterns are produced inside the package and the responses are received and compared. In this way, the network would not be used as the transferor of the patterns.

In Creasing the Testability: Because the major characteristics of the testability e.g. observability and controllability, are increasing.

In Creasing the Efficiency of NoC: Based on the proposed mechanism, the network will completely be in functionality sequence of the cores. There fore, the packages will delivered to the cores quickly and with minimum losing.

On Line and Structural Testing: It is possible to test the NoC without exiting the routers from it and to determine the exact location of the defective routers. That is the testing process is both online and structured.

High redundancy: The disadvantage of the proposed mechanism is that it imposes high amount of hardware enforcement on the chip's system (SOC).

Proposed Wrapper Architecture: The proposed wrapper is a hardware layer in which surrounds the routers is responsible of controlling the testing process. The responsibility of this wrapper is to connect to a router which is in testing mode in NoC and is able to change the current condition of the router to the testing-mode and the normal-mode. The proposed wrappers should be transparent in testing-mode. The structure of this wrapper is shown in figure 6.

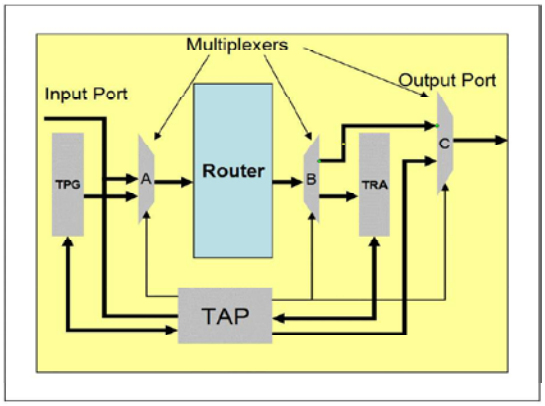

Fig. 6: Proposed wrapper architecture

As it is shown in figure 6, the proposed wrapper is comprises of following components:

Test Pattern Generation (TPG): This pattern produces proper testing patterns to the router. The generated patterns should be able to discover all possible errors in combinational parts and buffers.

Test Response Analyzer (TRA): This pattern is responsible for analyzing the test responses since the testing process is online, TPR and TPG should be included into the chip. There fore, they are considered as the internal components of the wrapper. The design of TPG and TRA will not be investigated in this study.

Multiplexers: A, B and C Multiplexers help the wrapper to modify the testing-modes the normal condition.

Test Access Unit (TAU): This pattern is responsible for scheduling the wrapper. In other words, TAU must control what should be done in every moment. Figure 7 shows an advanced design of TAU. As it is clear in figure 7, TAU consists of the following components; Packet Acceptance unit, Packet decoding unit, Safe/fail packet unit, Text execution unit. In continue each of these components is elaborated in details.

Package Acceptance Unit: When a package enters into the router from a specific port, it will be conducted to the package acceptance unit and will be kept there. It's necessary to mention that the format of the package and the message conform the complimented of AEthereal NoC [20].

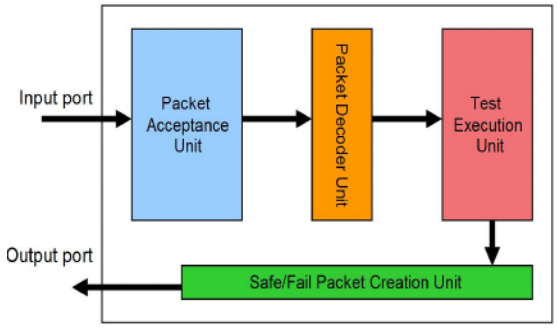

Fig. 7: Test Access Unit

Table 1: Type of packets in proposed architecture

2 bit	Type of packet
00	Data Packet
01	Test command packet
10	Safe/Fail Packet

Package Decoding Unit: There are 3 types of packages in this mechanism:

Data Package: These packages enter to the routers in order to be routed and the wrapper is transparent for them.

Test Command Package: It is a kind of package which contains test-running command for a specific router.

Safe/fail Package: This package is produced after the end of each test and it indicates whether a router is safe or failed. As well this package is sent to adjacent routers by the wrapper.

Therefore, in order to complete the decoding process, it is necessary to subjoin additional two bits. So, the wrapper will be known by the wrapper. Table 1 shows the differentiation of these 3 packages.

Safe/Fail Package Unit: The results of the test should be announced to the adjacent routers after they were analyzed. Accordingly, a package which is called safe/fail package is created in this part. It shows the test results of the router. If a tester sends the demand of the router's test, the results will be forwarded to that tester through inserting the tester's address on the reader of the package.

Test Execution Unit: As it is clear in table 1, the output of decoding package unit enters to test execution unit. This unit is actually a state machine with 6 statuses. The state machine, based on the input signals from contents of the internal control counters, internal control signals and

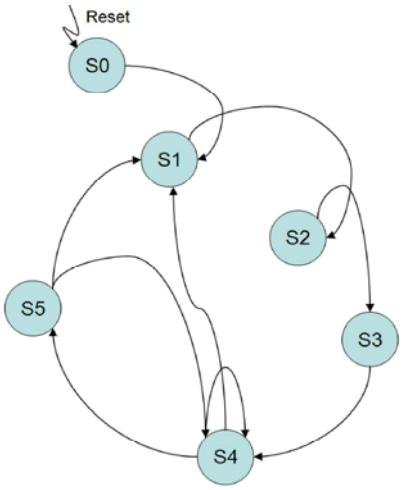

Fig. 8: The block diagram of the state machine

the current state, decides which control signals have to be activated and what the next state of the state machine is. The block diagram of state transition in the proposed machine is depicted in Figure 8.

The state machine enters to the state 0 through reset signal. States 1 to 4 are called testing process, because the running test-operation procedure is finished during these four stages. In order to provide accurate explanation about figure 8 and that what kinds of signals alters the status of the state machine, 7 major states are elaborated as follows:

State 0(S0): This state is the starting point of state machine. When the system on chip is restarted, this state stands in this position. In this case, the sub-testing router declares the adjacent routers of its own testing through sending a package to them. Therefore, the adjacent routers can not send any package to it until the testing procedure finished.

State 1(S1): In this state, the wrapper activates TPG and TRA via forwarding signals. TPG generates the testing patterns and applies it on the combinational circuit of the router. As well, TRA compresses the test responses. In addition, A and B multiplexers provide an appropriate strand (route). When all of the patterns were applied, the state machine moves to the next state, i.e. state 2.

State 2(S2): As like as the state 1, TPG, TRA and multiplexers are utilized in state 2, too. As regards, in this state, the test patterns are applied on the buffers of the router.

State 3(S3): In this state, test results move from TRA unit to test execution unit. According to these test results, test execution. Unit produces the statement package which explains the safety of destruction of the router to the adjacent routers. As well, this package is forwarded to the test applicant unit.

State 4(S4): In the state, testing processes have been finished and it was supposed to the normal situation. Hence, it declares to it's adjacents that it is going to return to its normal situation. So, they would be able to send a package to it in order to be routed. In this state, the wrapper conceals it self and the router continue its normal functions. There might be three occurrences in this stage: first, if a package that contains the data enters to the router, it will be able to route it and select an appropriate port for it. Second, if a package that contains test commands enters to wrapper, the state machine will leave 4this state to state 6 and it will begin testing procedure. And third, the router may not receive any package from its port, so the router will be workless for some times. Then, the state machine is required to move towards the state 5.

State 5(S5): As entering to this state, a counter will begin its function. If the counter becomes a little higher than the specified amount, the idleness period will be utilized for testing the router itself. Therefore, the state machine begins to test the router by moving to state 1. But, if the counter couldn't achieve to a determined amount, the package would not enter to the router. In order to be routed, the state machine moves to state 4 in order to perform its normal function.

SIMULATION RESULTS

Message that is being transferred by the NoC should have a special format. This format is the packet format. Each packet is composed of smaller data transfer units named as flits. Flits are the smallest possible units that can be transferred between hops in the path in NoC [20]. Flits are composed of actual physical words named as phit. Each phit is the actual physical data units that construct the packets. When a packet is being transferred, it will be transferred phit by phit. In AEthereal NoC, each phit is composed of 34 bits. In this paper, two more bits are added to each bit to distinguish the type of the package. Therefore the size of each phit will be 36 bits.

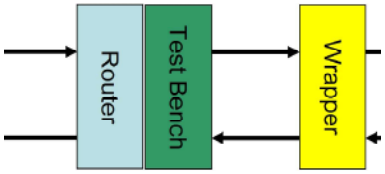

Fig. 9: Top level view of simulation

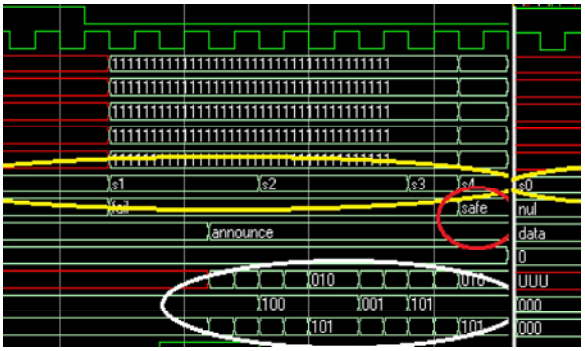

Fig. 10: Testing process (S0-S4) waveform

In order to simulate the proposed wrapper, hardware descriptive language has been used (VHDL). Codes written in this language, executed in ModelSim[1] software and their results are indicated in a waveform in this paper. The simulation has been performed in a hierarchical format. First, a router simulated and then a wrapper has been designed for the router and finally, In order to test the functionality of simulated elements a Test bench has been written. Figure 9 indicates the simulation hierarchical process.

In simulating the router, signals of Hermes router [21] has been used. The router has been simulated as a block which receives the patterns of the test and presents patterns as a response. After simulation of the router, the proposed wrapper was simulated by suggested elements. Then the router and the wrapper were combined and a Test bench designed for testing their function. Fig 10 indicates the function of the wrapper and the router when the signal relocation has been activated.

The orange oval indicates the stages of the state machine and testing process. The red circle indicates the result of the test and the white oval shows the patterns of the test performed upon the router. After the test is completed, the state machine goes to S4 and continues its normal functionality. But if the router idle for a while, a numerator, which its final amount is considered 10 clocks in the simulation, will begin to operate. If it reaches to 10 clocks, the state machine will turn into 5 positions. Fig 11 indicates a typical of the numerator.

[1]URL:http://www.model.com

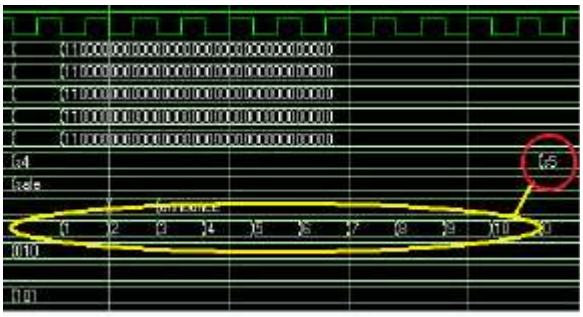

Fig. 11: Numerator of State 4

Fig. 12: Numerator of State 5

Also, in state 5, another numerator which its final amount in simulation is considered 5 clocks. If the numerator reaches to 5 clocks, the state machine will begin the test process. In fact, the wrapper uses the idle time of the router for testing. Fig 12 illustrates a numerator activated in state 5.

CONCLUSION

In this paper, a test wrapper proposed in which a router can be tested in its idle time. With this proposed mechanism, the location of all failed and damaged routers will be identified and also the algorithms designed for NOC will be economic and efficient. Proposed wrapper was simulated in VHDL language and performed in ModelSim software and the results presented in waveforms.

Suggestions for future works can be TPG and TRA architecture or designing a central unit named test manager which is responsible for testing of whole chip.

REFERENCES

1. Benini, L. and G.D. Micheli, 2005. Networks on Chips: A new SoC paradigm, In IEEE Computer, 35(1): 70-78, Jan. 2002. DOI:10.1109/MDT.108.
2. De Micheli, G., P. Pande, A. Ivanov, C. Grecu and R. Saleh, 2005. Design, Synthesis and Test of Networks on Chips, In IEEE Design and Test of Computers, 22(5): 404-413, Sept. 2005. DOI:10.1109/MDT.108.
3. Benini, L. and D. Bertozzi, 2005. Network-on-Chip architectures and design methods In IEEE Proc. Comput. Digit. Tech., 152(2): March 2005. DOI:10.1049/ip-cdt: 20045100.
4. Kumar, S., 2003. On Packet Switched Networks for On-Chip Communications book chapter in Networks on Chip, A. Jantsch and H. Tenhunen eds., Place of publication: Springer US, pp: 85-106. DOI: 10.1007/0-306-48727-6_5.
5. Grecu, C., *et al.,* 2004. Timing Analysis of Network on Chip Architectures for MPSoC Platforms, Microelectronics, 36(9): 833-845, 2004. DOI:10.1016/j.mejo.2005.03.006.
6. Karim, F., *et al*., 2002. An interconnect Architecture for Networking Systems on Chips, IEEE Micro, 22(5): 36-45, Sept. 2002. DOI: 10.1109/MM.2002. 1044298.
7. Benini, L. and D. Bertozzi, 2004. Xpipes: A Network-on-Chip Architecture for Gigascale System-on-Chip, IEEE Circuits and Systems Magazine, 4(2): 2004. DOI:10.1109/MCAS. 2004.1330747.
8. Marinissen, E.J., *et al*., 2002. On IEEE P1500's Standard for Embedded Core Test, In Journal of Electronic Testing: Theory and Applications, 18: 365-383, 2002. DOI:10.1023/a:1016585206097.
9. Tran, X., Y. Thonnart, J. Durupt, F. Bertrand, V. Beroulle and C. Robach, 2006. A Design-for-Test Implementation of an Asynchronous Network-on-Chip Architecture and its Associated Test Pattern Generation and Application, In Second ACM/IEEE International Symposium on Networks-on-Chip, pp: 149-158, IEEE 2006. DOI:10.1109/NOCS.2008. 4492734.
10. Zorian, Y., E. Marinissen and S. Dey, 1998. Testing Embedded-Core Based System Chips, In Proceedings of the 1998 IEEE International Test Conference, pp: 130-143, 1998. DOI:10.1109/2.769444.
11. Aktouf, C., 2002. A Complete Strategy for Testing an on-chip Multiprocessor Architecture. In IEEE Design Test of Computers, 19(1): 18-28, 2002. DOI:10.1109/54. 980050.

12. Aghaei, B. And S. Babaei, 2009. The new test wrapper design for core testing in Packet-Switched Micro-Network on Chip, in proc. Power Electronics and Intelligent Transportation System, pp: 346-352, 2009. DOI: 10.1109/PEITS.2009.5406770.
13. Cota, E., L. Carro and M. Lubaszewski, 2004. Reusing and On-Chip network for the Test of core-based systems, In ACM Trans. Design automation of electronic systems, 9(4): 471-499, Oct. 2004. DOI:10.1145/1027084.1027088.
14. Amory, A.M., E. Cota, M. Lubaszewski and F.G. Moraes, 2004. Reducing test time with processor reuse in Network-on-Chip based systems, In Proc. Integrated circuits and systems design, pp: 111-116, 2004. DOI:10.1109/SBCCI.2004.241289.
15. Wu, Y. and P. MacDonald, Testing ASICs with Multiple Identical Cores, In IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 22(3): 327-336, 2003. DOI:10.1109/TCAD. 2002.807889.
16. Liu, C., Z. Link and D.K. Pradhan, Reuse-based test access and integrated test scheduling for Network-on-Chip, In Proc. Design, Automation and Test in Europe, 1: 303-308, March 2006. DOI:10.1109/DATE.2006.244143.
17. Hosseinabadi, M., A. Banaiyan, M.N. Bojnordi and Z. Navabi, 2006. A Concurrent Testing Method for NoC Switches In Proc. Design Automation and Test in Europe(DATE), 1: 1171-1176, 2006. DOI:10.1109/DATE.2006.244018.
18. Grecu, C., P. Pande, B. Wang, A. Ivanov and R. Saleh, 2005. Methodologies and Algorithms for Testing Switch-Based NoC Interconnects, In Proceedings of the 2005 20th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT05), pp: 238-246, IEEE 2005. DOI:10.1109/DFTVS.2005.45.
19. Gh. Nazarian, 2009. On-line Testing of Routers in Networks-on-Chips, MSc Thesis.
20. Ciordas, C., K. Goossens, T. Basten, A. Radulescu and A. Boon, 2006. Transaction Monitoring in Networks on Chip: The On-Chip Run-Time Perspective, In International Symposium on Industrial Embedded Systems, pp: 1-10, Oct. 2006. DOI:10.1109/IES.2006.357464.
21. Moraes, F., N. Calazans, A. Mello, L.M. oller and L. Ost, HERMES: an infrastructure for low area overhead packetswitching networks on chip, VLSI journal, Elsevier.2004. DOI:10.1016/j.vlsi. 2004.03. 003.