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A Quadrature Voltage Controlled Oscillator Using In-Phase Injection Coupling Network

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Abstract: A Fully integrated 60GHz Quadrature Voltage Controlled Oscillator is proposed. Through a particular symmetrical coupling network formed by diode connected transistors, the in-phase coupling is realized in IPIC-QVCO, which reduces phase noise and phase error. The entire design is implemented in Agilent ADS (Advanced Design Systems) using 180nm technology. The measurement result shows a frequency range of 60GHz.The power consumption of the integrated QVCO is around 16.5mW using 1.8v power supply. Noise Figure is also calculated at the end of the design, which is reduced by 30% when compared with frequency dependent network. The phase noise of the QVCO is -128 ~ -138 dBc/Hz at1MHz offset. The objective of this project is to reduce the area of VCO block by 10% when compared with conventional VCO design and also reduce power consumption suitable for mm wave high data wireless transmissions.

Key words: CMOS · In-Phase Injection Coupled (IPIC) · Quadrature Voltage Controlled Oscillator (QVCO) · PLL

INTRODUCTION

A Quadrature oscillator produces two sine waves with 90° phase difference between them. These are useful to pan signals (particularly in a quadraphonic environment), or to make a frequency-shifter when combined with a pair of identical oscillators. At resonance, the voltage across a parallel L-C network and the current circulating within it are 90 degrees out of phase. In other words it means that the circuit has quadrature voltages for two coupled oscillators.

VCOs are used in Function generators, the production of electronic music, to generate variable tones in synthesizers Phase-Locked Loops frequency synthesizers used in communication equipment. Voltage-to-Frequency converters are voltage-controlled oscillators, with a highly linear relation between applied voltage and frequency. They are used to convert a slow analog signal (such as from a temperature transducer) to a digital signal for transmission over a long distance, since the frequency will not drift or be affected by noise. VCOs may have sine and/or square wave outputs. Function generators are low-frequency oscillators which feature multiple waveforms, typically sine, square and triangle waves. Analog phase-locked loops typically contain VCOs. High-frequency VCOs are usually used in phase-locked loops for radio receivers. Phase noise is the most important specification for them. Low-frequency VCOs are used in analog music synthesizers. For these, sweep range, linearity and distortion are often most important specifications. Phase Locked Loop (PLL) is an important block in a transceiver. Design of the wide range, low phase noise, low phase error and low power CMOS PLL for the 60 GHz direct-conversion transceiver is challenging, due to trade-offs between tuning range, phase noise, phase error and power consumption.

There are many methods for generating mm-wave quadrature LO signals, but they suffer from many problems [1]. (i) The most common method is through a conventional mm-wave parallel quadrature voltage-controlled oscillator (P-QVCO), but its phase noise is poor [2]. (ii) The method of using a divide-by-2 divider after a VCO with double LO frequency prevails in multi-GHz applications, but it is difficult to design a VCO and a divider at very high frequency. Moreover, the power consumption of this method is high.(iii) If passive components such as an RC polyphase filter or quadrature hybrid coupler are used to produce quadrature signals,

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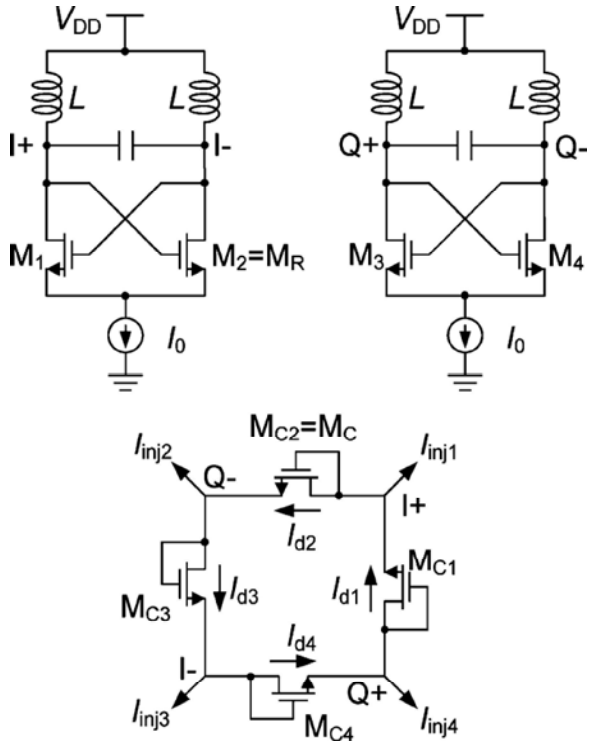

Fig. 1: Schematic of the proposed IPIC-QVCO [1]

we usually need buffers to compensate their loss, so the power consumption is also high [3]. (iv) Using an injection-locked multiplier is a good choice [4], but the disadvantages are limited locking range and intrinsic phase error due to the imbalance of the structure, or quadrature inputs are needed to overcome these two drawbacks [5]. In this work, we present a wide range, low phase noise and low power 60 GHz quadrature VCO. The simplified block diagram of the proposed VCO is shown in Fig. 1.

The paper is organized as follows. Section II discusses the Proposed IPIC-QVCO, including architecture, analysis and circuit design. Section III describes the analysis of oscillation mode. Experimental results are provided in Section IV and conclusions are drawn in Section V.

In-Phase Injectioncoupled QVCO: The proposed QVCO consists of two identical oscillators pulling each other through coupling networks, to lock at a common frequency with quadrature phase. This in-phase coupling can reduce both phase noise and phase error. Injection locking and injection pulling are the frequency effects that can occur when harmonic oscillator is disturbed by a second oscillator operating at a nearby frequency. when the coupling is strong enough and the frequency is near enough, the second oscillator can capture the first oscillator causing it to have essentially identical frequency as second, this is injection locking.

When the second oscillator merely disturbs the first oscillator but does not capture it, the effect is called injection pulling. These phenomenon's are mainly observed in electronic oscillators and laser resonators. In modern day VCO an injection locking signal may override its low frequency control voltage, resulting in loss of control. When intentionally employed, injection locking provides a means to significantly reduce power consumption and possibly reduce phase noise in comparison to other frequency synthesizers and PLL designs. There are many phase shifting techniques which were presented to realize In-Phase coupling [1].But their coupling networks are either RC based or LC based phase shifters which are both frequency dependent.

The In-phase coupling is realized in the proposed IPIC-QVCO [1] by using the frequency-independent network, instead of the frequency-dependent phase shifter.

Tuning of L and C gives the required transient response as shown in Fig. 13 yielding L=0.1uH and C=0.367pF respectively.

Alternate Model of IPIC-QVCO

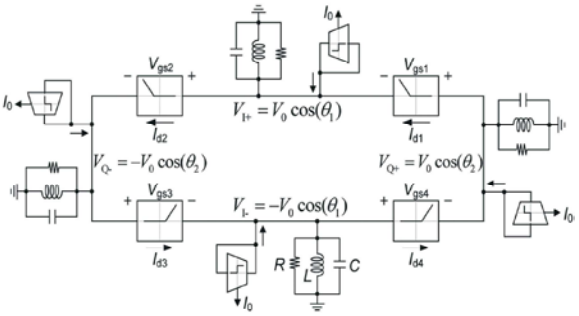

Fig. 2: Alternate Model of IPIC-QVCO [1]

Magnitude and Phase of LC tank circuit:

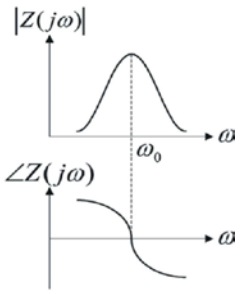

Fig. 3: Magnitude and Phase of LC-tank Circuit [1]

Operation of IPIC QVCO, Analysis of Oscillationmode: The two identical differential *LC* cross-coupled VCOs are coupled through a symmetrical coupling network. In the coupling network, each diode-connected transistor connects two oscillation nodes with $\pi/2$ phase difference [1], like transistor M_{c1} connects node Q+ and node I+. So the four diode-connected transistors form a symmetrical ring. Let us assume that the tank Q is high enough that only the fundamental components need to be considered. When the QVCO is operating, M_{c2}'s gate voltage V_g has a phase of 0 degree and the source voltage V_s has a phase of $-\pi/2$, as shown in Fig. 4(a). Since the amplitudes of V_g and V_s are the same, the gate-source voltage V_{gs} has a phase of $\pi/4$. Therefore, the phase of M_{c2}'s drain current I_{d2} is also $\pi/4$. M_{c2} is turned on only when V_{gs} is larger than its threshold voltage. The conduction angle is less than, so works in Class-C mode.

Similarly, the phase of Mc2's drain current is $3\pi/4$. The Current I_{inj}, injected into the node I+ from the coupling network, is equal to $(I_{d1}-I_{d2})$, as shown in Fig. 4(b). Thus, I_{inj} is shifted by exactly π compared with I_{inj} or V_{I+} [1]. A similar situation exists in the other three nodes V_{Q-}, V_{Q+} and V_{I-}. Therefore, the In-phase coupling is realized in IPIC-QVCO. Since the coupling network does not employ any passive component, it is frequency-independent. As will be demonstrated in simulation and measurement, the parasitic capacitance has little impact on the in-phase coupling even at the mm-wave frequency.

We start with the drain current of a diode-connected transistor in the coupling network. Assuming that its V_s and V_g are $V_0\cos(\theta_1)$ and $V_0\cos(\theta_2)$ respectively, where $\theta_1=\omega t$, $\theta_2=(\omega t+\varphi)$, V_0 is the oscillation amplitude, ω is the oscillation frequency and $0<\varphi<2\pi$. Thus, the gate-source voltage V_{gs} is represented in eq (1).

$$\cos A-\cos B=2\sin\frac{B-A}{2}\sin\frac{B+A}{2}$$

$$=V_0[2\sin\frac{\theta_1-\theta_2}{2}\sin\frac{\theta_1+\theta_2}{2}]$$

If suppose $\theta_2=B$, $\theta_1=$ A

$$=V_0[2\sin\frac{\theta_2-\theta_1}{2}\sin\frac{\theta_1+\theta_2}{2}]$$

Since $\theta_1 t=\omega t$ and $\theta_2=\omega t+\psi$

$$=V_0[2\sin\frac{\theta_2-\theta_1}{2}\cos(\frac{\theta_1+\theta_2}{2}+\frac{\pi}{2})]$$

$$=V_0[2\sin\frac{\omega t+\psi-\omega t}{2}\cos(\frac{\omega t+\psi+\omega t}{2}+\frac{\pi}{2})]$$

$$=V_0[2\sin\frac{\psi}{2}\cos(\omega t+\frac{\psi}{2}+\frac{\pi}{2})] \quad (1)$$

And finally the gate source voltage

$$V_{gs}=2V_0\sin\frac{\psi}{2}\cos\omega t \quad (2)$$

The transistor is on when $V_{gs}>V_t$, so the total conduction angle 2ϕ is given by eq (3).

$$\frac{V_t}{2V_0\sin\frac{\psi}{2}}=\cos\omega t$$

$$\omega t=\cos^{-1}(\frac{V_t}{2V_0\sin\frac{\psi}{2}})$$

$$\text{Then } 2\phi=2\cos^{-1}(\frac{V_t}{2V_0\sin\frac{\psi}{2}}) \quad (3)$$

The transistor is in saturation region when it is turned on. Then Drain Current of diode connected transistor is given by eq (4).

$$I_d=g_{mK}(V_{gs}-V_t)$$

$$=g_{mK}(2V_0\sin\frac{\varphi}{2}\cos\omega t-V_t)-V_t) \quad (4)$$

where $g_{mK}=K\,V_{sat}\,C_{ox}$ W,K is the short–channel effect modulating parameter and V_{sat} is the saturation velocity of transistor. The desired oscillation frequency is given by eq (5).

$$\text{Oscillation Frequency}=\frac{1}{2\pi\sqrt{LC}} \quad (5)$$

which gives oscillation frequency about 60GHz with L=60pH and C=0.11727pF respectively and this constitutes a resonant circuit.

Simulation Results: The practical results of proposed design are performed in Agilent Advanced Design Systems (ADS) 2015.1.0.Version using 180 nm Technology respectively.

When two identical oscillators are cross coupled and connected to the symmetrical network, with respect to Fig. 6.

Supply Voltage Vs Frequency Response: The design and results have been performed in Agilent advanced design Software. The variation of voltage with respect to frequency is given by Fig. 11.

The output waveforms of identical LC-Oscillators along with Symmetrical Coupling network is as shown in Fig. 12.

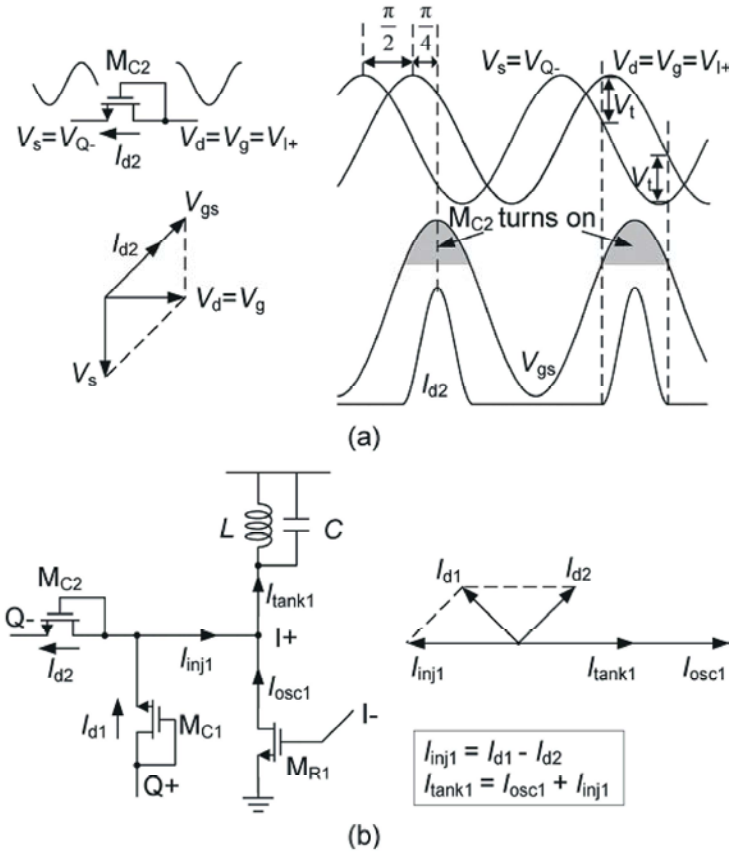

Fig. 4: Analysis of (a) diode-connected transistor and (b) coupling network in IPIC-QVCO

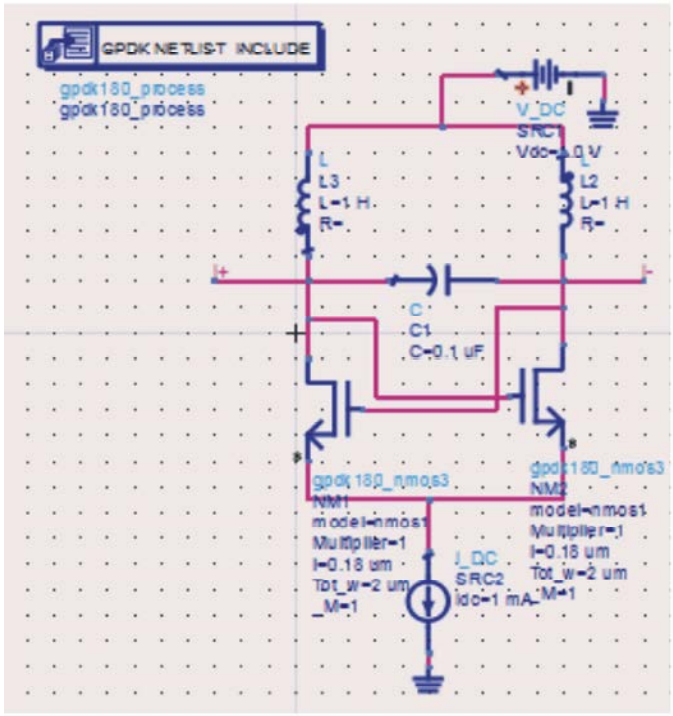

Fig. 5: LC-Oscillator Circuit

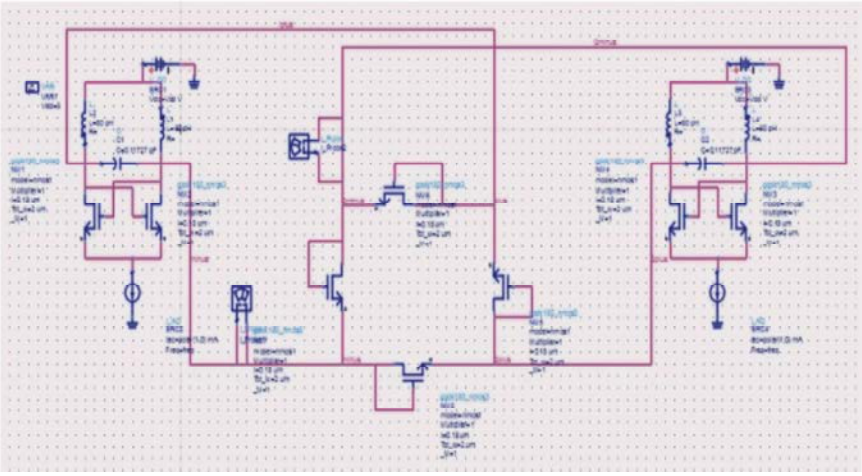

Fig. 6: Proposed Quadrature VCO with Symmetrical coupling network

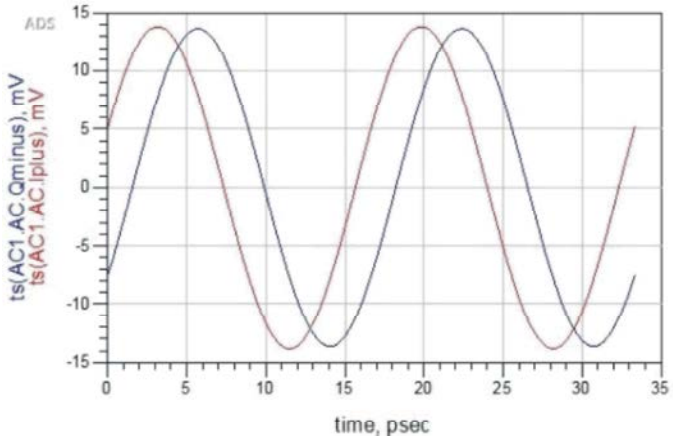

Fig. 7: Analysis of coupling network in IPIC-QVCO

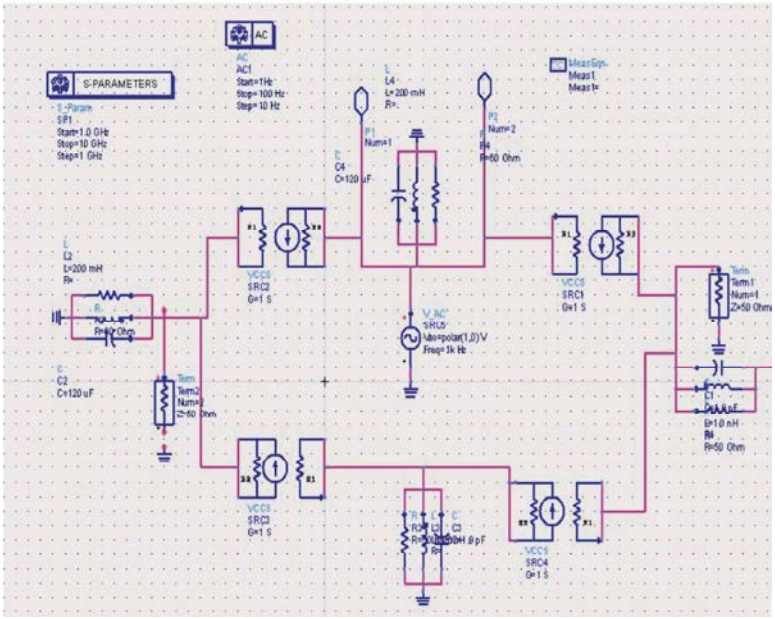

Fig. 8: Alternate Model of IPIC-QVCO

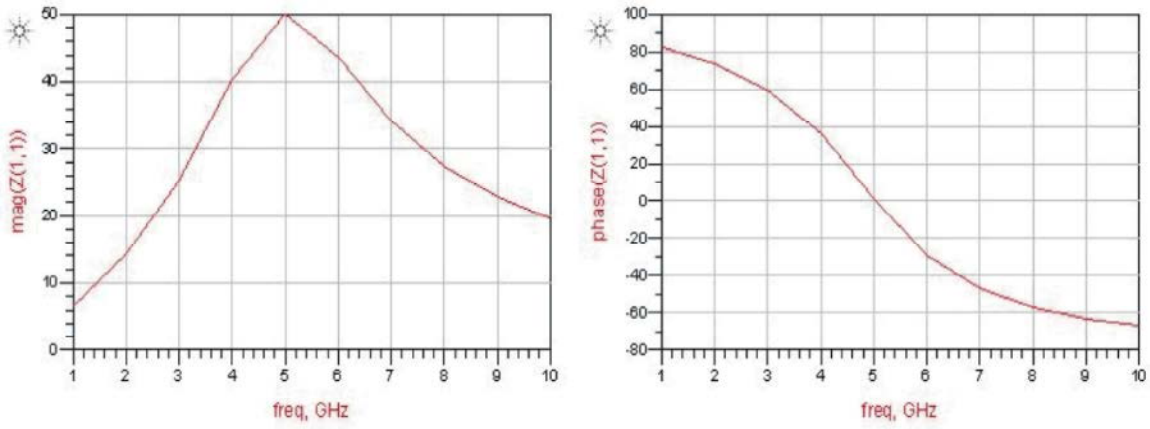

Fig. 9: Magnitude and phase of LC tank circuit

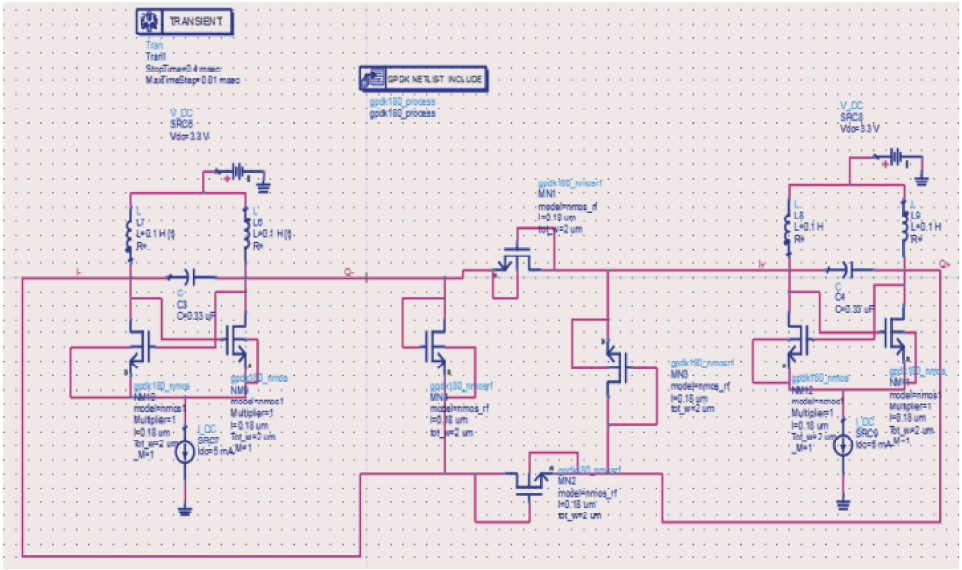

Fig. 10: Schematic of IPIC-QVCO in ADS

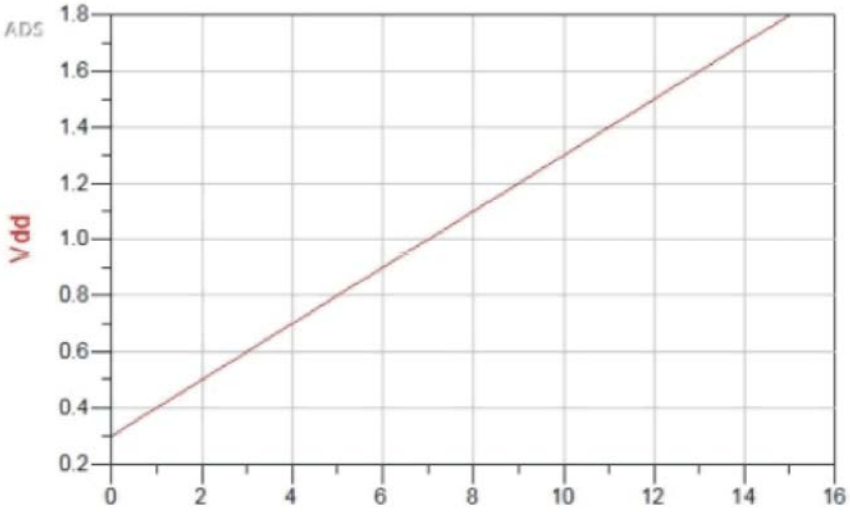

Fig. 11: Supply Voltage Vs Frequency

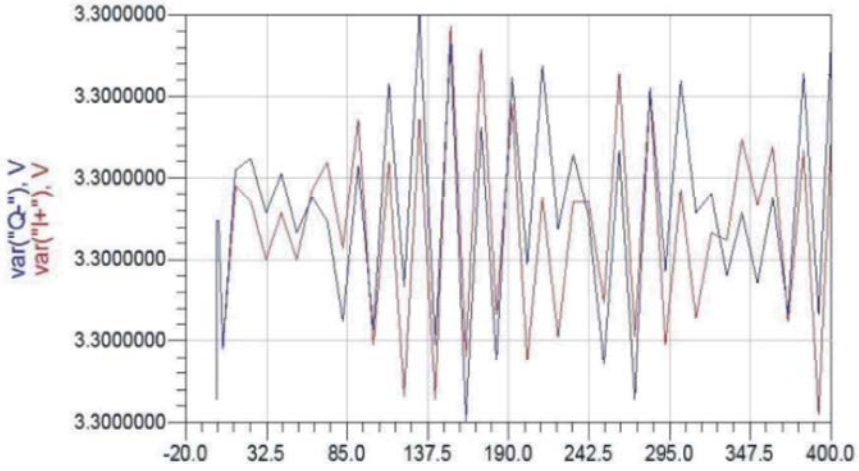

Fig. 12: Transient response of IPIC-QVCO circuit

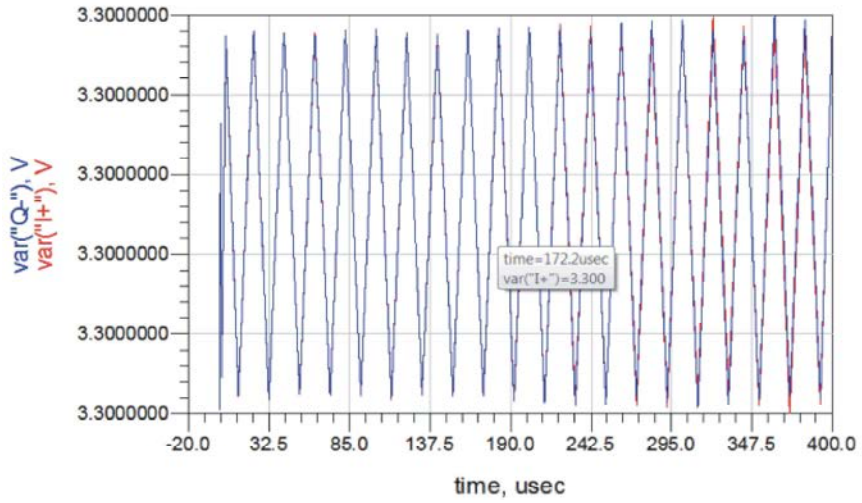

Fig. 13: Transient Response of LC-Oscillator after Tuning of LC elements

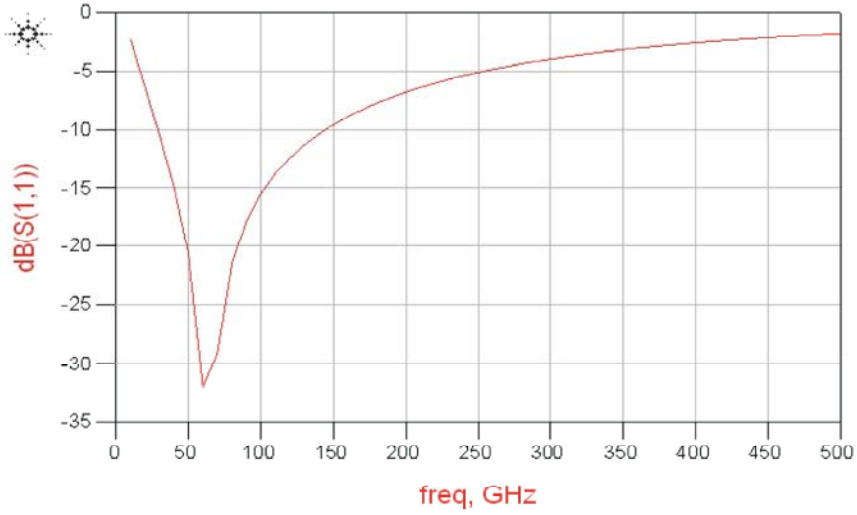

Fig. 14: S (1, 1) Input Reflection Coefficient

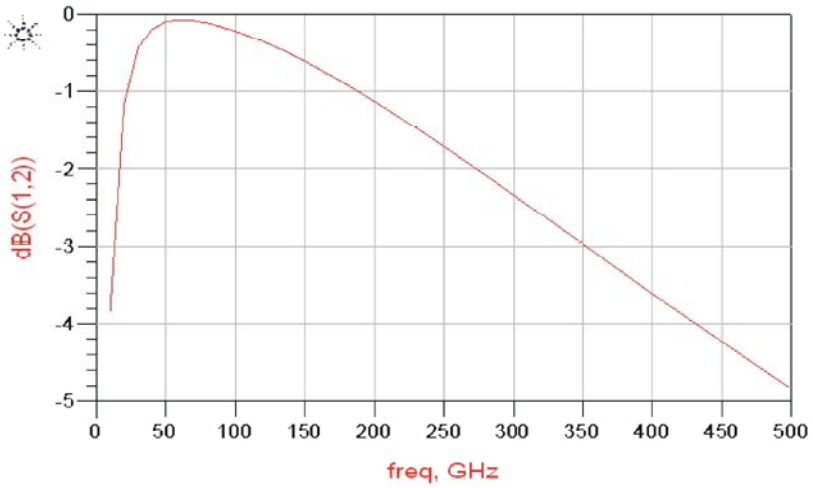

Fig. 15: S (1, 2) Reverse Transconductance Gain

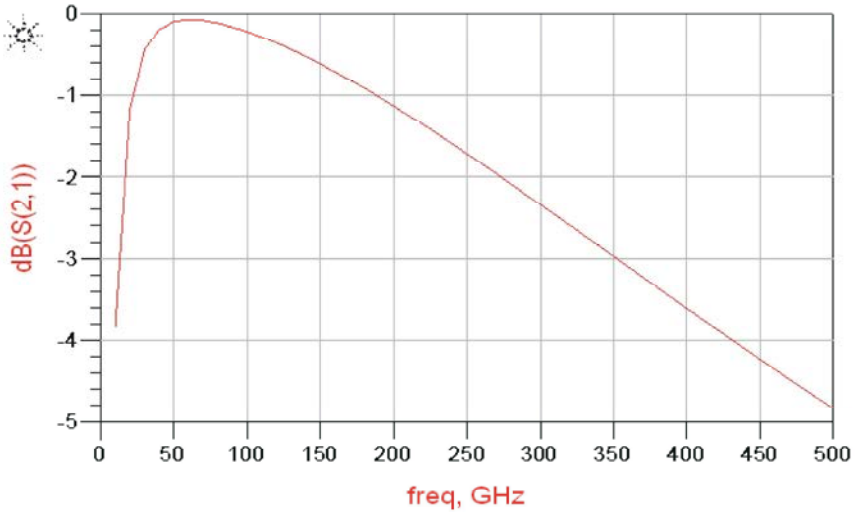

Fig. 16: S (2, 1) Forward Transconductance Gain

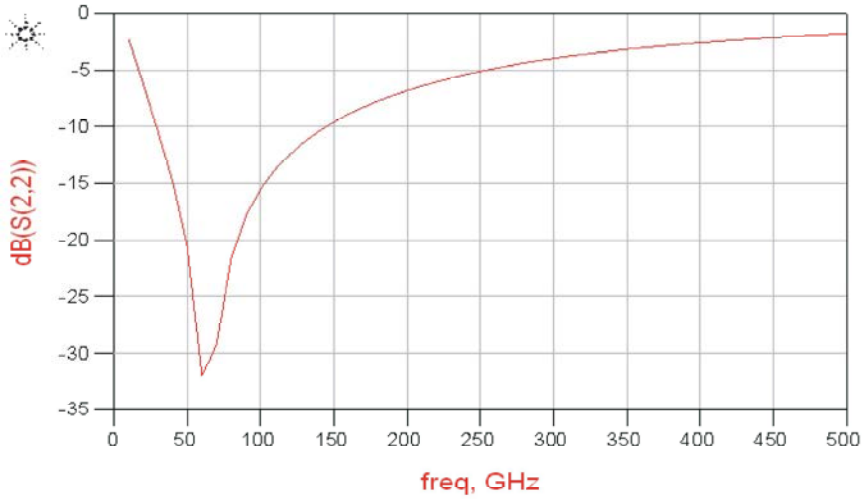

Fig. 17: S (2, 2) Output Reflection Coefficient

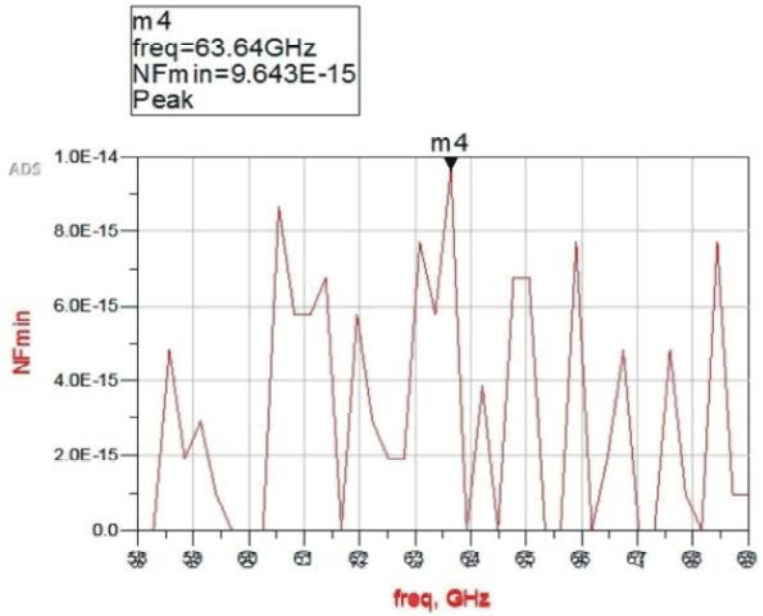

Fig. 18: Noise Figure of QVCO

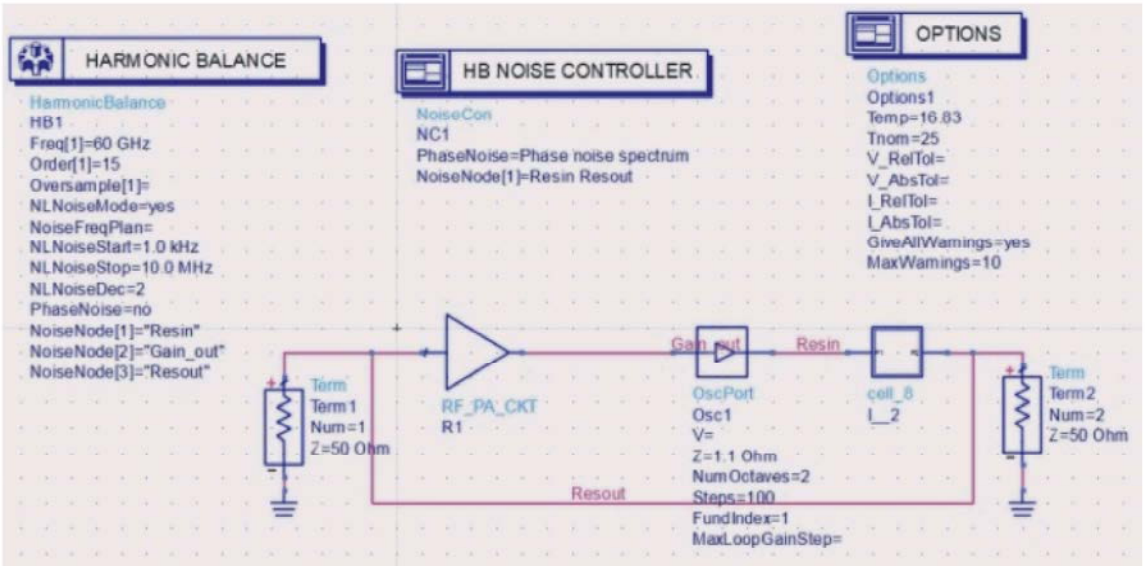

Fig. 19: Schematic of finding phase noise in ADS.

Transient Response of LC Oscillator: Tuning of L and C parameters in Oscillator circuit gives us the required oscillatory response with a phase difference of $\pi/2$ between two oscillation nodes I_{plus} and Q_{minus} respectively as shown in Fig. 13.

Parameters Analysis: For a distributed network or RF circuits we deal with incident and reflected waves in terms of power and hence we prefer s – parameters to analyze port matching's or to find reflections at the ports in the circuit. S parameter graphs are determined by using simulation-S parameters in ADS.

The S_{11} also called as input reflection coefficient whose value is around less than 10dB(in Fig. 14), S_{12} also called as reverse gain, sometimes called as isolation is always a negative value (in Fig. 15), S_{21} called as forward transconductance gain that can be up to -5dB(in Fig. 16), S_{22} is called as output reflection co-efficient whose accurate value is less than -10dB(in Fig. 17).

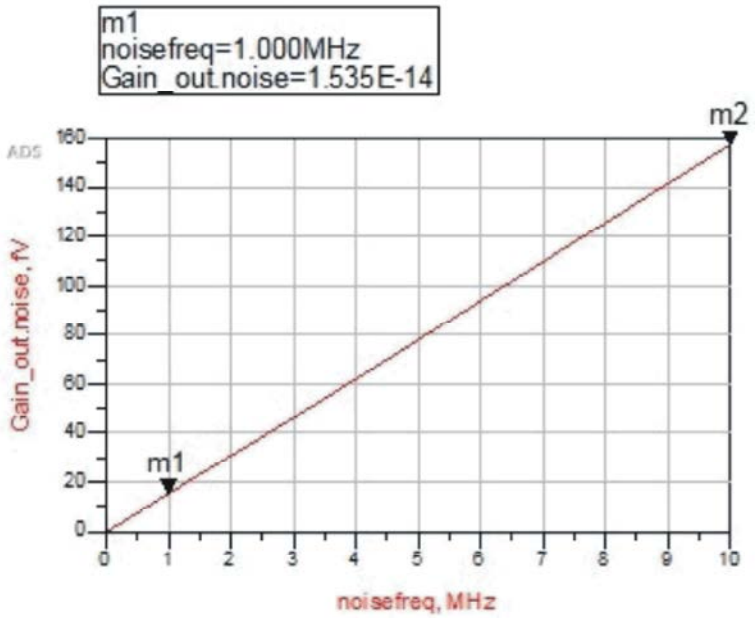

Fig. 20: Phase Noise of QVCO in ADS

The S-parameter for the IPIC-QVCO is obtained as shown in Fig. 14, Fig. 15, Fig. 16, Fig. 17 respectively for the proposed QVCO.

With respect to Fig. 14 and Fig. 17 it is clearly seen that S(1,1) and S(2,2) are identical, which means that input and output are perfectly matched. Similarly in Fig. 15 and Fig. 16 it is observed that the S(1,2) and S(2,1) are also matched since both of them contribute same graph. From this it is clearly understood that ports of symmetrical coupling network are perfectly matched.

Noise Figure: The noise performance of an RF oscillator is represented by its noise factor or noise figure. The noise factor accounts for the degradation of the signal's SNR due to the transmission of signal from input to output. It is defined as the SNR at the input of the network divided by the SNR at them output of the network.

$$F = (SNR_{IN}/SNR_{OUT}) \quad (6)$$

where SNR_{IN} and SNR_{OUT} are the SNR's at the input and output of the amplifier, respectively. The noise factor represents the signal's quality in terms of noise before and after the network. The noise figure is the same as the noise factor expressed in dB in eq. (6).

$$NF\ (dB) = 10 \log F \quad (7)$$

Phase Noise: Phase noise is the difference between ideal and practical oscillators. The fluctuations in the output signal due to noise causes signal energies spread across the harmonics of fundamental frequency, which is known as phase noise.

Phase noise is calculated by using harmonic balance and HB noise controller by taking various parameters into consideration like respective nodes, freq, order, phase noise etc in display of the corresponding simulators.

The measured phase noise is around -128dBc/Hz ~- 138dBc/Hz respectively at 1MHz offset as shown in Fig. 20.

CONCLUSION

In this paper a 60GHz QVCO has been proposed, based on the diode connected symmetrical coupling network. In this regard we have made an attempt to design a QVCO with reduced area which reduces the power consumption required for the circuit since there are no inductor and capacitor in this network. This circuit has been implemented in 180nm CMOS technology and simulated by using ADS. The large frequency span helps to mitigate impact of variability, which can pose a significant challenge in mm-wave designs. An analysis of transient response, noise Figure along with s-parameter model graphs are being analyzed to verify the functionality respectively. The phase noise of the QVCO

is -128~-138 dBc/Hz at1MHz offset. The power consumption of the proposed QVCO is 16.5mW which is reduced about 50% when compared with QVCO with inductors and capacitors along with frequency dependent network.

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