Middle-East Journal of Scientific Research 24 (7): 2302-2308, 2016
ISSN 1990-9233

DOI: 10.5829/idosi.mejsr.2016.24.07.23750

Design, Modeling, Analysis and Simulation of a SEPIC Converter

[1]J. Leema Rose and [2]B. Sankaragomathi

[1]Department of Electrical and Electronics Engg,
Loyola Institute of Technology & Science, Thovalai, Tamil Nadu, India
[2]Department of Electronics and Instrumentation Engg,
National Engg College, Kovilpatti, Tamil Nadu, India

Abstract: This paper presents the design and modeling of a SEPIC DC-DC converter (Single Ended Primary Inductance Converter). The SEPIC converter allows a range of dc voltage to be adjusted to maintain a constant voltage output. SEPIC converter is used to overcome the limitation of conventional buck boost converter like inverted output, pulsating input current, high voltage stress make it unreliable for wide range of operation. MATLAB simulation is being used to validate the method and show the effectiveness of the design.

Key words: DC-DC Converter · SEPIC Converter · Modeling

INTRODUCTION

There are many types of dc-dc converters. Buck converters can only reduce voltage, boost converters can only increase voltage and buck-boost, Cúk and SEPIC converters can increase or decrease the voltage. Buck-boost converters can be cheaper because they only require a single inductor and a capacitor. This often makes the buck-boost expensive or inefficient. Cúk converters solve both of these problems by using an extra capacitor and inductor. Both Cúk and buck-boost converter operation cause large amounts of electrical stress on the components, this can result in device failure or overheating. SEPIC converters solve both of these problems. The single-ended primary-inductor converter (SEPIC) is a type of DC/DC converter allowing the electrical potential (voltage) at its output to be greater than, less than, or equal to that at its input. The output of the SEPIC is controlled by the duty cycle. The conventional power converter such as buck, boost and buck-boost converters cannot maintain a wide operation range with high efficiency, especially if up-and-down voltage conversion has to be achieved. These characteristics can be obtained in a Single Ended Primary Inductor Converter (SEPIC). Also, the SEPIC converter provides positive regulated output voltage for the given input voltage unlike the buck-boost converter which provides negative regulated output voltage. Isolation is provided by series coupling capacitor which protects the converter when short circuit occurs. Non- inverted output, low equivalent series resistance (ESR) of coupling capacitor minimizes ripple and prevent heat build up which make it reliable for wide range of operation. Some of the drawbacks in conventional buck-boost converter like inverted output, pulsating input current, high voltage stress and floating switch make it unreliable for the wide range of operation. So in order to overcome this, SEPIC converter is used.

Literature Review: In their work, Jaw-Kuen Shiau [1] and team had focused on the development of a circuit simulation model for maximum power point tracking (MPPT) evaluation of solar power that involves using different buck-boost power converter topologies; including SEPIC, Zeta, and four-switch type buck-boost DC/DC converters. Reeto Jose [2] and their coworkers, had presented their work on DC-DC SEPIC Converter Topologies. They had mentioned that the conventional SEPIC converter needs capacitance with high value and high current handling capacity. The bulk inductor has been used in conventional SEPIC converter, so it is increases the component size and reduces the response speed. These characteristics reduces passive component size, improves response speed. Also, Soft switching can be achieved for a wide input and output voltage ranges. They had simulated the new resonant SEPIC converter using MATLAB/Simulink for 3.6V.

Corresponding Author: J. Leema Rose, Dept. of EEE, Loyola Institute of Technology & Science, Thovalai, Tamil Nadu, India.

Venkatanarayanan and Saravanan [3], had performed a study to design and analyze a Proportional-Integral (PI) control for SEPIC, which is the start-of-the-art DC-DC converter. The single Ended Primary Inductor converter performs the voltage conversion from positive source voltage to positive load voltage. Their study proposed a development of PI control capable of providing the good static and dynamic performance compared to Proportional-Integral Derivative (PID) controller. Wael A. Salah and their team [4], had presented their work on the implementation of PWM control strategy for torque ripples reduction in brushless DC motors. Results had shown a smoother output torque and current produced in comparison with that using conventional PWM control technique with an average of 50% reduction in the generated torque ripples. Antonietta De Nardo and coworkers [5], had designed a mixed electrolytic/ceramic filter capacitor in DC–DC converters. This study presents a symbolic method for the design of filter capacitors in DC–DC switching converters, using a combination of a ceramic and an electrolytic capacitor.

Yuh-Shyan Hwang and their team [6], had worked on a continuous conduction mode low-ripple high-efficiency charge-pump boost converter. In this work, a new continuous conduction mode (CCM) low-ripple high-efficiency charge-pump boost converter had been presented. Umamaheswari and their team [7], had presented their work on the analysis and design of digital predictive controller for PFC Cuk converter. Dewei and coworkers [8], had analyzed the emerging technologies to power next generation mobile electronic devices using solar energy. Mobile electronic devices such as MP3,mobile phones and wearable or implanted medical devices have already become a necessity in peoples' lives. However, the further development of these devices is restricted not only by the inconvenient charging process of the power module, but also by the soaring prices of fossil fuel and its downstream chain of electricity manipulation.

Kavitha and Uma [9], had presented their work on the control of Chaos in SEPIC DC-DC Converter. DC-DC converters are widely used in power electronic systems where there is a need for stabilizing a given dc voltage to a desired value. It had been reported that DC-DC converters exhibit different non-linear phenomena including bifurcations, quasi-periodicity and chaos under both voltage mode and current mode control schemes. In their work, current mode controlled SEPIC converter operating in continuous conduction mode had been considered and by varying the reference current Iref, the converter exhibits chaos. The circuit may be used either as a standalone IC controller or as controller circuit that is technology-compatible with on-chip switching power converters and on-chip loads for future powered Systems on Chip.

Design of Sepic Converter

Duty Cycle Calculation: The amount that the SEPIC converters step up or down the voltage depends primarily on the Duty Cycle and the parasitic elements in the circuit.The output of an ideal SEPIC converter is given by

$$V_0 = \frac{D * V_i}{1 - D} \tag{1}$$

However, this does not account for losses due to parasitic elements such as the diode drop VD. These make the equation

$$V_0 + V_D = \frac{D * V_i}{1 - D} \tag{2}$$

This becomes

$$D = \frac{V_0 + V_D}{V_0 + V_i + V_D} \tag{3}$$

The maximum Duty Cycle will occur when the input voltage is at the minimum. The maximum Duty cycle is

$$D_{\max} = \frac{V_0 + V_D}{V_0 + V_{i\min} + V_D} \tag{4}$$

Inductor Selection: For determining the inductance is to allow the peak-to-peak ripple current to be approximately 40% of the maximum input current at the minimum input voltage. The ripple current flowing in equal value inductors L1 and L2 is given by

$$\Delta I_L = I_i X 40\% = I_0 x \frac{V_0 x 40\%}{V_{i\min}} \tag{5}$$

The inductor value is calculated by

$$L_1 = L_2 = L = \frac{V_{i\min}}{\Delta I_L x f_{sw}} x D_{\max} \tag{6}$$

where fsw is the switching frequency and Dmax is the duty cycle at the minimum V in . The peak current in the inductor, to ensure the inductor does not saturate, is given by

$$I_{L1peak} = I_o x \frac{V_o + V_D}{V_{i\min}} x(1 + \frac{40\%}{2}) \quad (7)$$

$$I_{L1peak} = I_o x \frac{V_o + V_D}{V_{i\min}} x(1 + \frac{40\%}{2}) \quad (8)$$

If L1 and L2 are wound on the same core, the value of inductance in the equation above is replaced by 2L due to mutual inductance. The inductor value is calculated by

$$L_1' = L_2' = \frac{L}{2} = \frac{V_{i\min}}{2x\Delta I_L x f_{sw}} x D_{\max} \quad (9)$$

Power MOSFET Selection: The parameters governing the selection of the MOSFET are the minimum threshold voltage Vth(min), the on resistance RDS(ON), gate-drain charge QGD and the maximum drain to source voltage, VDS(max). Logic level or sublogic-level threshold MOSFETs should be used based on the gate drive voltage. The peak switch voltage is equal to Vin + Vout. The peak switch current is given by

$$I_{Q1peak} = I_{L1peak} + I_{L2peak} \quad (10)$$

The RMS current through the switch is given by

$$I_{Q1rms} = I_0 \sqrt{\frac{(V_0 + V_{i\min} + V_0) x (V_o + V_D)}{V_{i\min}^2}} \quad (11)$$

$$P_{Q1} = I_{Q1rms}^2 x R_{DSON} x D_{\max} + (V_{i\min} + V_0) x I_{Q1peak} x \frac{Q_{DO} x f_{sw}}{I_G} \quad (12)$$

PQ1, the total power dissipation for MOSFETs includes conduction loss (as shown in the first term of the above equation) and switching loss as shown in the second term. IG is the gate drive current. The RDS(ON) value should be selected at maximum operating junction temperature and is typically given in the MOSFET data sheet. Ensure that the conduction losses plus the switching losses do not exceed the package ratings or exceed the overall thermal budget.

Input Capacitor Selection: The SEPIC has an inductor at the input. Hence, the input current waveform is continuous and triangular. The inductor ensures that the input capacitor sees fairly low ripple currents. The RMS current in the input capacitor is given by:

$$I_{cinrms} \frac{\Delta I_L}{\sqrt{12}} \quad (13)$$

The input capacitor should be capable of handling the RMS current. Although the input capacitor is not so critical in a SEPIC application, a 10 ìF or higher value, good quality capacitor would prevent impedance interactions with the input supply.

Output Capacitor Selection: When the power switch Q1 is turned on the inductor is charging the output current is supplied by the output capacitor. The RMS current in the output capacitor is

$$I_{corms} = I_0 \sqrt{\frac{V_0 + V_D}{V_{i\min}}} \quad (14)$$

The ESR, ESL and the bulk capacitance of the output capacitor directly control the output ripple. Assume half of the ripple is caused by the ESR and the other half is caused by the amount of capacitance.

$$ESR \le \frac{V_{ripple} x 0.5}{I_{L1peak} + I_{L2peak}} \quad (15)$$

$$C_0 = \frac{I_0 x D}{V_{ripple} x 0.5 x fsw} \quad (16)$$

In surface mount applications, tantalum, polymer electrolytic and polymer tantalum, or multi-layer ceramic capacitors are recommended at the output.

Output Diode Selection: The output diode must be selected to handle the peak current and the reverse voltage. In a SEPIC, the diode peak current is the same as the switch peak current $I_{Q1(peak).}$ The minimum peak reverse voltage.

$$V_{RD1} = V_{i\max} + V_{o\max} \quad (17)$$

The power dissipation of the diode is equal to the output current multiplied by the forward voltage drop of the diode. Schottky diodes are recommended in order to minimize the efficiency loss.

SEPIC Coupling Capacitor Selection: The selection of SEPIC capacitor, Cs, depends on the RMS current, which is given by

$$I_{corms} = I_0\sqrt{\frac{V_0 + V_D}{V_{i\min}}} \tag{18}$$

The SEPIC capacitor must be rated for a large RMS current relative to the output power. The voltage rating of the SEPIC capacitor must be greater than the maximum input voltage. The peak-to-peak ripple voltage on Cs

$$\Delta V_{cs} = \frac{I_o x D_{\max}}{C_s x f_{sw}} \tag{19}$$

Modelling of Converter: Modeling of a particular converter is done by either Circuit Averaging method or State Space Averaging method. Analytical and circuit based models that become complicated for fourth order and some second order systems [3]. The simplest approach is to use the state space analytical method. Mathematical model determines the voltage, current and signal transfer function of the switching converter.

State Space Analysis: State Space Analysis of SEPIC converter for continuous conduction mode can be done in two modes of operation. For a given network has two states in CCM, S1 on, S2 off and S1 off, S2 on, the response of the network in each state may be time weighted and averaged. The state equations can be expressed in matrix form as,

$$\dot{X} = A_1 x + B_1 u \tag{20}$$

$$Y = C_1 x + D \tag{21}$$

where X is the time derivative of the state variable vector, $A1$ is the state matrix, x is the state variable vector, $B1$ is the input matrix, u is the input and Y is the output.
The state variables are taken as,

$x_1 = i_{L1}$, $x_2 = i_{L2}$, $x_3 = V_{C1}$, $x_4 = V_{C2}$

Mode 1: Switch S- ON (0< t < DT)

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{RC_2} \end{bmatrix} B_1 = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{22}$$

Mode 2: Switch- OFF (DT < t < (1-D)T)

$$A_2 = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & -\frac{1}{L_1} \\ 0 & 0 & 0 & -\frac{1}{L_2} \\ -\frac{1}{C_1} & 0 & 0 & 0 \\ \frac{1}{C_2} & \frac{1}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} B_2 = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{23}$$

The state space averaged equation is given as,

$X = [A_1 d + A_2 (1\text{-}d)] x + [B_1 d + B_2 (1\text{-}d)] u$]

Therefore, the large signal model is expressed as,

$$\begin{bmatrix} i_{L1} \\ i_{L2} \\ \dot{v}_{C1} \\ \dot{v}_{C2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{d-1}{L_1} & \frac{d-1}{L_1} \\ 0 & 0 & \frac{d}{L_2} & \frac{d-1}{L_2} \\ \frac{1-d}{C_1} & \frac{-d}{C_1} & 0 & 0 \\ \frac{1-d}{C_2} & \frac{1-d}{C_2} & 0 & \frac{-1}{RC_2} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} [u] \tag{24}$$

Analysis and Simulation of Converter

Analysis: The analysis and simulation of SEPIC converter is in progress using MATLAB. The circuit diagram of SEPIC converter is given in Figure 1. All dc-dc converters operate by rapidly turning on and off a MOSFET, generally with a high frequency pulse. What the converter does as a result of this is what makes the SEPIC converter superior. For the SEPIC, when the pulse is high/the MOSFET is on, inductor 1 is charged by the input voltage and inductor 2 is charged by capacitor 1. The diode is off and the output is maintained by capacitor 2. When the pulse is low/the MOSFET is off, the inductors output through the diode to the load and the capacitors are charged. The greater the percentage of time (duty cycle) the pulse is low, the greater the output will be.

This is because the longer the inductors charge, the greater their voltage will be.

Simulation: Here open loop and closed loop SEPIC converter is analyzed and the circuits are given in Figure 2 and 5. Compared to open loop closed loop system is more efficient. The PI control is for closed loop system.

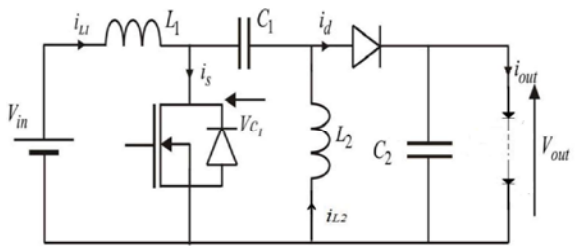

Fig. 1: Equivalent Circuit diagram of SEPIC converter

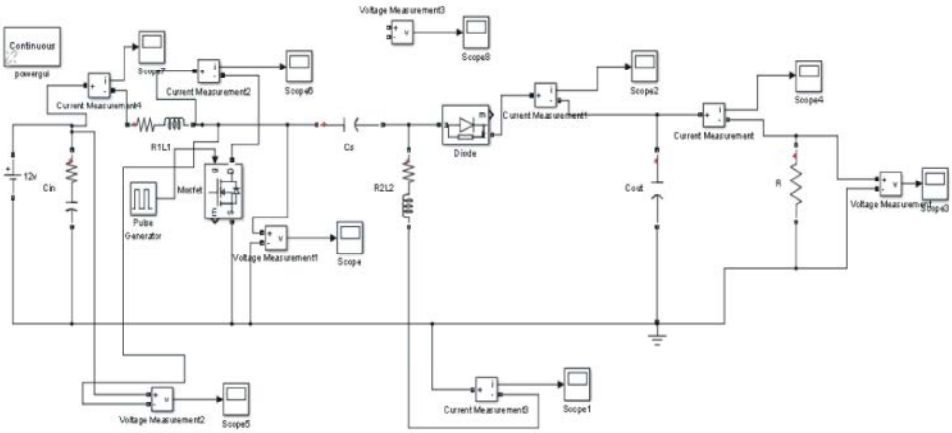

Fig. 2: Open loop simulation of SEPIC converter

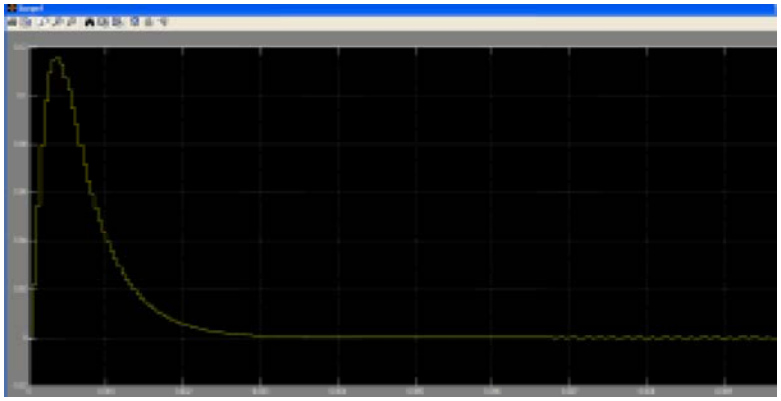

Fig. 3: Voltage waveform of Open loop SEPIC Converter

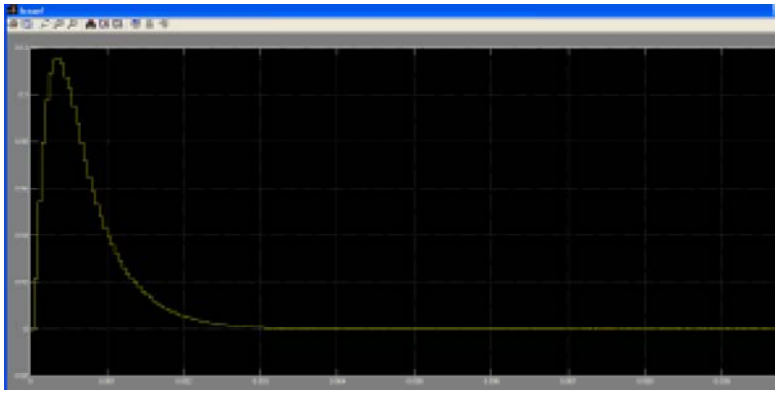

Fig. 4: Current waveform of Open loop SEPIC Converter

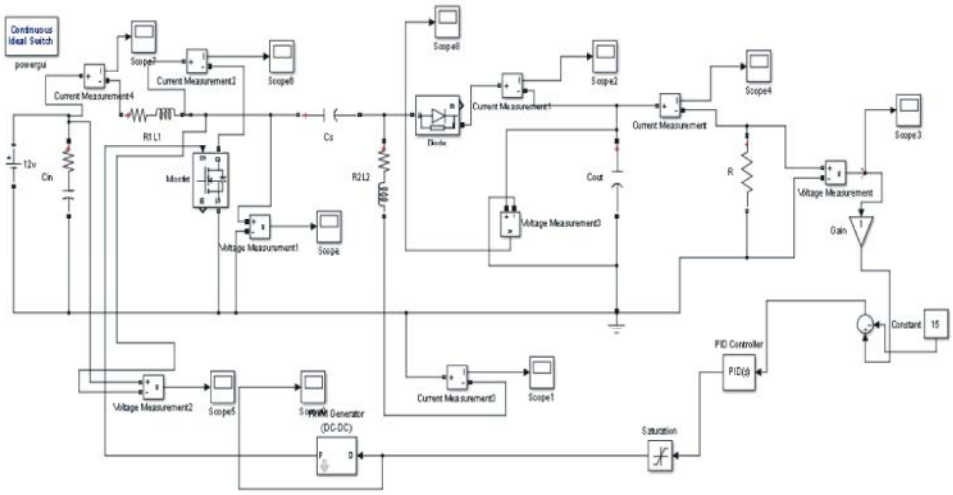

Fig. 5: Closed loop simulation of SEPIC converter

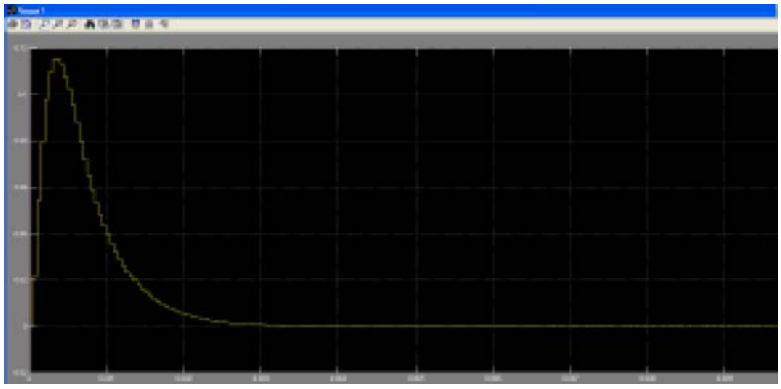

Fig. 6: Voltage waveform of Closed loop SEPIC Converter

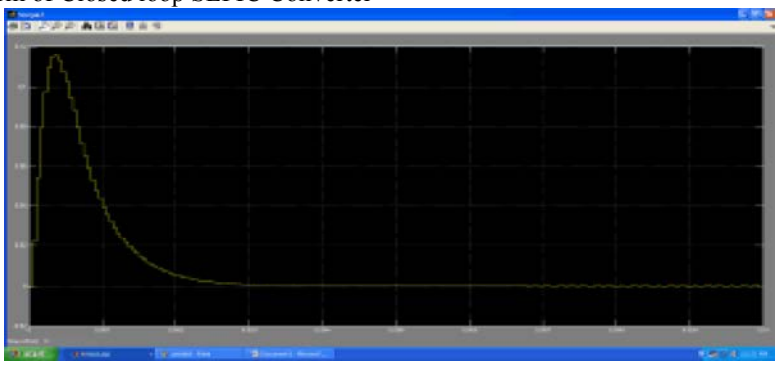

Fig. 7: Current waveform of Closed loop SEPIC Converter

The simulation output of voltage and current for closed loop is given in Figure 3 and 4 and for open loop is given in Figure 6 and 7.

RESULTS AND DISCUSSION

The analysis and simulation of SEPIC converter has been carried out using MATLAB. The resistances in the inductors and the capacitors can also have large effects on the converter efficiency and ripple. Inductors with lower series resistance allow less energy to be dissipated as heat, resulting in greater efficiency (a larger portion of the input power being transferred to the load). Due to the difficulty in control of its 4th-order and non linear property, it is still not well-exploited.

REFERENCES

1. Jaw-Kuen Shiau, Min-Yi Lee, Yu-Chen Wei and Bo-Chih Chen, 2014. Circuit Simulation for Solar Power Maximum Power Point Tracking with Different Buck-Boost Converter Topologies, Energies, 7: 5027-5046.
2. Reeto Jose. K, Anisha Shivanandan, Vani Venugopal and Kshemada Devi, 2015. V, DC-DC SEPIC Converter Topologies, Int. Jnl. of Research in Engg. and Technology, 04(05): 20-23.
3. Venkatanarayanan, S. and M. Saravanan, 2014. Proportional-integral Control for SEPIC Converter, Research Jnl. of Applied Sciences, Engineering and Technology, 8(5): 623-629.
4. Wael A. Salah, Dahaman Ishak, Basem Abu Zneid, Amir Abu_Al_Aish, Mohd Shawal Jadin and Anees Abu Sneineh, 2015. Implementation of PWM control strategy for torque ripples reduction in brushless DC motors, Electr Eng., 97: 239-250.
5. Antonietta De Nardo, Nicola Femia and Walter Zamboni, 2012. Designing a mixed electrolytic/ceramic filter capacitor in DC–DC converters, Analog Integr Circ Sig Process, 73: 3-45.
6. Yuh-Shyan Hwang, An Liu, Chia-Hsuan Chen, Yi-Tsen Ku, Jiann-Jong Chen and Cheng-Chieh Yu, 2014. A continuous conduction mode low-ripple high-efficiency charge-pump boost converter, Analog Integr Circ Sig Process, 79: 355-369.
7. Umamaheswari, M.G., G. Uma and L. Annie Isabella, 2014. Analysis and design of digital predictive controller for PFC Cuk converter, J Comput Electron, 13: 142-154.
8. Dewei Jia, Yubo Duan and Jing Liu, 2009. Emerging technologies to power next generation mobile electronic devices using solar energy, Front. Energy Power Eng. China, 3(3): 262-288.
9. Anbukumar Kavitha and Govindarajan Uma, 2010. Control of Chaos in SEPIC DC-DC Converter, Int. Journal of Control, Automatio n and Systems, 8(6): 1320-1329.