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Reduced Clock Allocation Network for On-Chip Compression Format in VLSI Design

[1]*Ms.C. Suganya and* [2]*V. Pushpalatha*

[1]Saveetha Engineering College, VLSI Design, Chennai, India
[2]Saveetha Engineering College, Department of ECE, Chennai, India

Abstract: Now-a-days power dissipation is a vital subject in elevated presentation digital routes, because the amount of transistors has increased significantly. Several methods have been planned to decrease the switching activity. This paper presents a new examination data compression technique based on a Huffman compression code that uses a viterbi decoder. Huffmann compression is used to compress the data in the clock tree method. In the proposed system, the power and clock skew are reduced by using the huffman compression technique. Experimental result indicates the flexibility and efficiency of the proposed method. This method simulated in modelsim software.

Key words: Clock Tree Design · *S*witching Activity · Huffmann Compression

INTRODUCTION

Power dissipation is an vital issue in today's chip design, because the amount of transistors has increased significantly. Some methods have been proposed to reduce the switching activity. Power dissipation in cmos circuits is comparative to the switching movement in the circuit. In the existing method of grouping algorithm uses a minimum spanning tree to guesstimate the interrelate capacitance and slice the finished wire capacitance in the routing stage. It is based on the minimization of the flip-flops alone, [1-4] it is one of the important technique to reduce the switching movement. Which check attainable power savings? For more power savings using the pulsed latch in the clock tree concept. In the clock tree relocation process that can travel a flip-flop based clock tree into a pulsed latch for power reduction. Which also check attainable power savings? [5-6]. Power consumption is one of the main factors to optimize the clock tree. The clock node consumes more power than any other node on a chip. Clock tree should use no power beyond the clock tree load. Clock tree can dissipate up to 40% of total power. The main plan to reduce the clock tree power, the chip power can be wholly reduced. Further diminish the chip power the proposed structural design employing the huffmann compression method to compact the data in the clock tree system.

Related Work: Power consumption is one of the essential factor in the today's chip design. Clock tree minimization, timer gating and various supply voltages techniques have been proposed. The major goal of the above techniques is to reduce the clock tree power. The above three techniques is totally based on the flip-flops alone. Flipflops are the most general storage element in the sequential circuits. The pulsed designs have gains of together the flip-flops and the latches. It needs a lesser amount of power and timing confirmation is easy. By using the pulsed latch in the timer tree, the continuing method of timer tree relocation method include mutually a flip-flop and the pulsed latch to decrease the switching action in the dynamic power, by decreasing the dynamic power in the clock tree process the chip power can be greatly reduced.

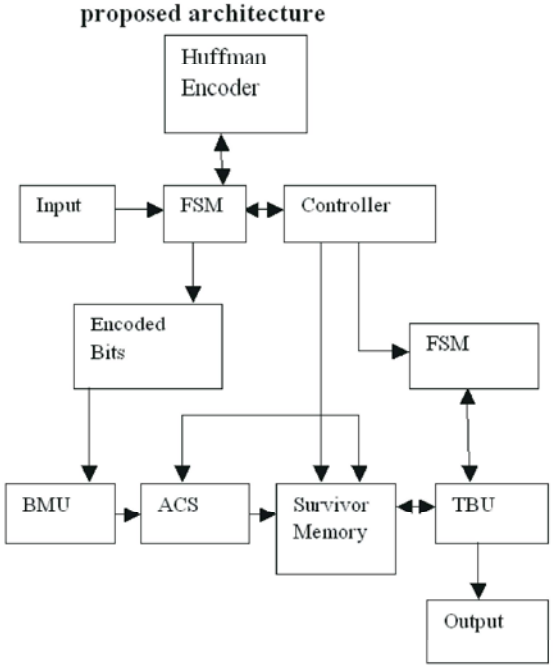
Clock Allocation Network: The clock allocation network (or clock tree) is the metal and buffer network that distributes clock to all clocked elements. Clock trees are regularly built by clock tree synthesis tools. The main aim of clock tree synthesis is to differ routing paths and placement of clocked cells and clock buffer to meet maximum speed specification. Clock skew is the variation in arrival time of a clock edge at any two flip-flop clock inputs. Clock skew adds directly to clock phase times reducing the system clock speed. Clock signal is

Corresponding Author: Ms.C. Suganya, Saveetha Engineering College, VLSI Design, Chennai, India.

generated externally (pll) in the clock distribution network.pll denotes phase locked loop it is used to generate the on-chip clock signal.

Overview of Proposal: In the proposed architecture the input is given to the finite state machine. Where the inputs are the flipflops and latches. The flip flops and latches are compressed by using the huffmann encoding technique. Huffman coding uses a detailed method for choosing the representation for each symbol, resulting in a prefix code (occasionally called "prefix-free codes", so as to be, the small piece sequence in place of a particular symbol is never a prefix of the small piece sequence representing any other symbol). Huffman coding is such a common method for creating prefix codes that the term "huffman code" is widely used as a synonym for "prefix code" even when such a code is not produced by huffman's algorithm.

Huffmann Compression Technique: Huffman compression is an inconsistent time-taken coding that assigns tinier codes for additional oftentimes utilized acts are better codes for fewer oftentimes utilized acts in order to cut the size of files being compression and transferred.



Proposed architecture in the planned architecture a huffmann compression method employing viterbi decoder for frank (not punctured) program normally consists of the pursuing main blocks:

- Finite state machine
- Huffmann encoder
- Branch metric unit (bmu)
- Add compare select (acs)
- Trace back unit(tbu)
- Controller
- Survivor memory

The main purpose of the planned architecture is to compact the quantity of data in the clock tree manner. Input data is given to the finite state mechanism. The finite state machine checks the bits and then the bits will be encoded in the huffmann encoder. The branch metric unit is used to calculate the minimum distance. The trace back unit decodes the data and get the retrieved original data, the entire original data will be displayed in the output.

Branch Metric Unit (BMU): It too computes the hamming distances (i.e branch metric) among the established symbol and estimated symbol. Branch metric unit is otherwise called as division metric constituent.

Huffmann Encoder: Huffmann encoding an algorithm designed for the lossless compression of records based going on the regularity of occurrence of a character in the file that is being condensed. The huffmann algorithm is based on arithmetic coding which means that the possibility of a symbol has a straight behaviour on the time-taken of its representation. Huffmann codes are obtained by constructing a huffmann tree. Huffmann encoding further enchances compression.

Finite State Machine (FSM): Finite state mechanism is in purely single condition at a instance. The condition it is in at particular period is shouted the present state. A state machine is each mechanism that supplies the class of something at a specified period and be able to job on input to change the rank and or/cause an action or output to seize locale for every certain change.

- An early status or proof of something stored place.
- A position of feasible input events.
- A position of original states that could outcome from input.
- A position of feasible actions or amount produced actions that outcome from a latest position.

Trace Back Unit (TBU): Trackback mechanism includes the manipulation constituent, trace back mechanism and decomposing trace back way for reading the stored survivor path information.

The trace back mechanism reads stored survivor path data according to the commencing gesture and the address gesture from the manipulation constituent and performs trace back established on the survivor trail information.

The stay decomposing constituent sequentially delays decoded data from the trace back mechanism up to the predetermined bit according to commencing signal. From the manipulation constituent to output one byte decoded data each one period trace back.

Add Compare Select (ACS): Add compare select constituent endowed a viterbi decoder for decoding convolution data. The convolution data includes punctured data and non punctured data.

The decoder includes the branch metric constituent for computing division metrics of a consented convolution data.

From the branch metrics and a previous state metric. A trace back unit traces the current and the next path selection information selected in the add compare select unit to find a maximum likelihood path from which the convolution data was received and output decoded data.

Controller: A controller generates a plurality of decoding control signals to the branch metric constituent the add contrasting constituent and the trace back unit.

Survivor Memory: Survivor memory is used to store the bits.

EXPERIMENTAL RESULTS

Using the huffmann techinique the power dissipation can get reduced comparing the migrated clocktree technique.

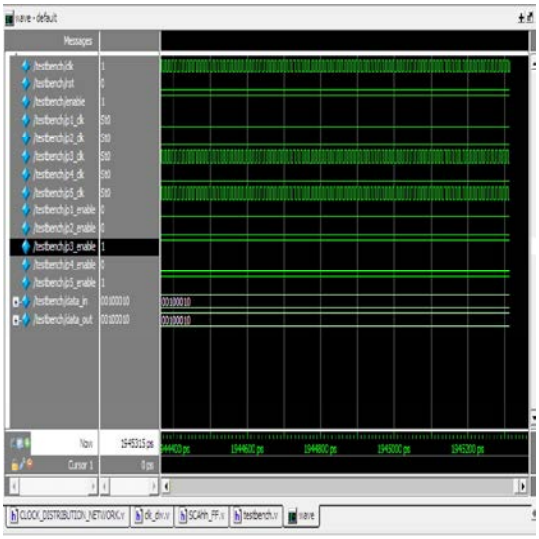
Table1: Experimental result for migrated clock tree shows how much power is available in the core

Power	Unit
Total power dissipation	71.54mw
Dynamic power dissipation	10.62mw
Static power dissipation	46.16mw
I/o power dissipation	14.76mw

Table 2: Experimental result for huffmann compression shows how much power is available in the core

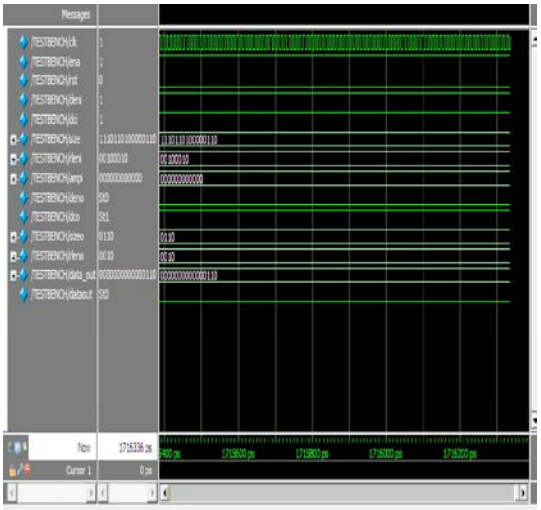
Power	Unit
Total power dissipation	64.52mw
Dynamic power dissipation	5.12mw
Static power dissipation	46.12mw
I/o power dissipation	13.28mw

Simulation Result for Migrated Clock Tree



In the migrated clock tree simulation we assigned the 5 pages of memory in the input.the pages are p1-p5.each page contain 5 rows and the 8 columns of memory. The memory's are the latches and the flipflops.if we give the input as 1 in the p1 and p3 means. The respective output will be displayed depend upon the input.

Simulation Result for Huffmann Compression



In the above simulation result the compression technique includes the selection and the mux line. It assigned 100 memory element as the input, the proposed architecture reduce the output as 50.it is the better result compared with the previous techniques.

Application:

- Huffmann compression is requested in computer webs, modems and fax machines
- Employing huffmann coding in vlsi, fast video streaming on internet is possible.
- Computer storage machine such as hard disk drives.

CONCLUSION

In this thesis we suggest an huffmann compression method based on a viterbi decoder model is used to compress the data and to decrease the total power dissipation in the clock tree method.the power and the clock skew are reduced by using the huffmann compression technique. Experimental results indicate the flexibility and efficiency of the clock tree method. It is the better result compared with the previous papers.

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