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Implementation of High Efficiency Interleaved DC–DC Boost Converter with Voltage Doubler Cell and Clamped Circuit

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Abstract: DC-DC boost converters are mostly employed in renewable energy system such as photovoltaic system, fuel cell and so on, because these systems generate low output voltage which is not suitable for grid connected power applications. This paper proposes an interleaved boost converter which consists of voltage doubler cell and clamped circuit to achieve large output voltage gain without extremely increasing the duty ratio compared to the conventional boost converter. Furthermore, the energy stored in the leakage inductance of the coupled inductor is recycled and voltage stress across the main switch is minimized by using clamped circuit which leads to increase the output voltage gain. It is a non isolated converter topology which reduces the high voltage spikes on the switches. The voltage gain, efficiency, voltage stress across the switch of the proposed topology is investigated and compared with the existing topology. Results are obtained using MATLAB simulation and validated by hardware implementation.

Key words: DC-DC boost converter · Interleaved boost converter · Voltage doubler cell · Clamped circuit

INTRODUCTION

Today, high output voltage gain DC-DC converters plays an important role in many applications such as UPS (Uninterrupted Power Supplies), Photovoltaic power generation systems, fuel cell, electric traction and so on. In those applications the conventional boost converter is used but it has some disadvantages such as the voltage stress of the main switch is equal to the output voltage of the converter which leads to increase in the voltage rating of the switch and high voltage gain is obtained by extremely large duty ratio. As well, the transient response is low due to the large turn off period of main switch which in turn creates the output diode reverse-recovery problem. Furthermore, electromagnetic interference problem is severe. Since the conventional boost Converter produces the output voltage eight times greater than the input voltage but it is not considered to be efficient. Therefore, many topologies were used for improving the efficiency of DC-DC boost converter. First was to achieve high voltage gain by adjusting the turn's ratio of the transformer which increases the system cost. Furthermore, the leakage inductance of the transformer introduces large voltage spike across the switch and also create some energy losses [1-4]. In order to prevent the large voltage spike, the snubber circuit can be used but energy stored in the leakage inductance of the transformer is dissipated [5]. The system cost is reduced and efficiency of the converter is increased by employing the non- isolated DC/DC converters [6-11]. Another family of topology is DC/DC converter with active Clamped circuit. It is used to minimise the voltage stress across the main switch which in turn reduces the voltage rating of the switch. Since the cost of the switch is reduced [12-14]. Then the output voltage of the DC-DC boost converter is increased by varying the turns ratio of the coupled inductor [15-20].

The coupled inductor and clamped circuit are implemented in conventional boost converter which increases the output voltage gain but input current ripple is high. Consequently, the efficiency of the converter is reduced.

Furthermore, number of passive element is high whereas the cost can be increased. In proposed system, coupled inductor and clamped circuit are employed in conventional interleaved boost converter whereas the input current ripple is reduced so that converter efficiency is increased.

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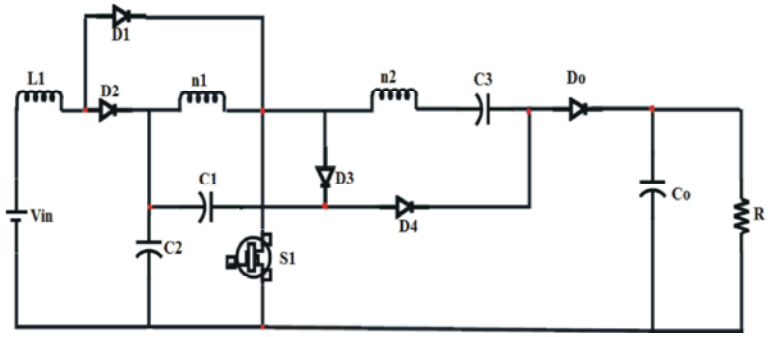

Fig. 1: Circuit diagram of DC-DC Converter with integrating coupled inductor and diode-capacitor

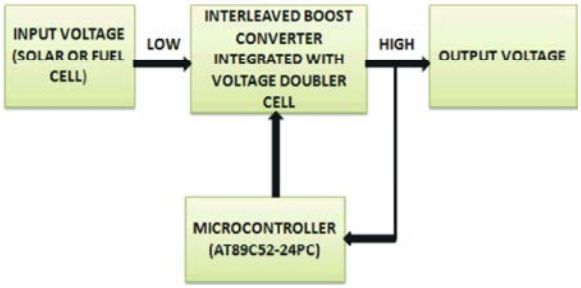

Fig. 2: Block diagram of the interleaved boost converter with voltage doubler cell

Block Diagram of the Proposed System: Block diagram of interleaved boost converter with voltage doubler cell is shown in Figure 1. Here the interleaved boost block consists of coupled inductor and clamped circuit.

Operating Principle of Proposed Converter: The proposed converter consist of input inductor L_1 and L_2, active switches Q_1 and Q_2, coupled inductor M, clamped circuit comprising of capacitors and diode, output capacitor C_O, voltage doubler cell consists of diode and capacitor. Fig. 2. shows that proposed interleaved boost converter with voltage doubler cell.

The advantages of proposed converter are as follows:

- The output voltage gain is increased by using coupled inductor.
- The voltage stress on the switch is reduced by using active clamped circuit. Consequently, low voltage rating and low on-state resistance R_{DS} (ON) switching devices can be used which leads to minimization of the cost.
- An input current ripple can be reduced so that output capacitor ripple current is minimized.

Design Methodology of Proposed System

Selection of Input Inductor: The renewable energy system produces the high input current ripples such as PV and fuel cell. So the proposed converter is designed for continuous conduction mode (CCM) and input current ripple is 15% of average output current. Because of the input current is divided into two path and 180 degree out off phase shift can be introduced between the two inductor so that the input current ripple should be cancelled.

$$Input\ inductor = \frac{\frac{V_{out}}{2} \times D}{I_{peak} \times 0.3 \times f_s} \tag{1}$$

$$I_{peak} = \frac{P_{out(\max)} \times \sqrt{2}}{V_{in}(\min)} \tag{2}$$

where f_s is switching frequency, I_{peak} is peak current and D is duty cycle.

Selection of Duty Ratio: The duty ratio can be selected based on the turn's ratio of the coupled inductor and input ripple current. The input ripple current ripple will be minimized at 50% of the duty ratio. So that the duty cycle can be choose 0.5. This is derived by,

$$R(D) = \frac{1-2D}{D} if\ D \le 0.5 \tag{3}$$

$$R(D) = \frac{2D-1}{D} if D > 0.5 \tag{4}$$

$$D = 1 - \frac{\sqrt{2+N}}{M} \tag{5}$$

where N is turns ratio of the coupled inductor and M is voltage gain.

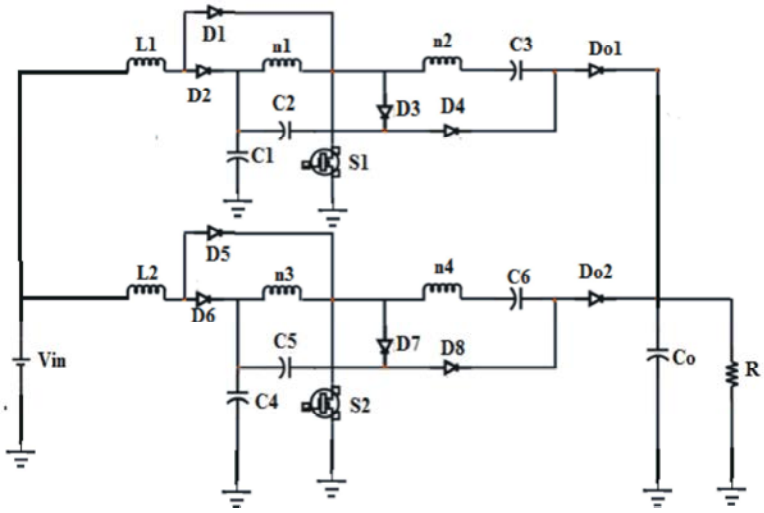

Fig. 3: Circuit diagram of proposed system

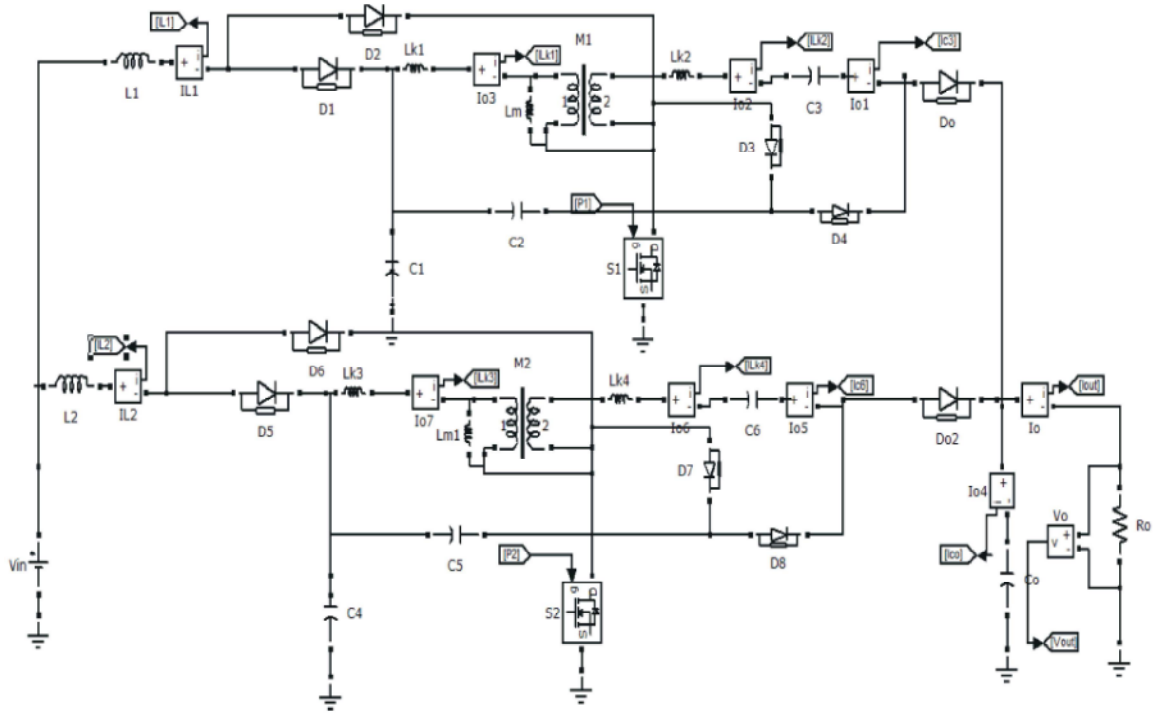

Fig. 4: Simulation diagram of proposed converter

Design of Capacitors: The clamped capacitor C_1 is used to suppress the voltage ripple across the switch and capacitor C_2 is used for further extending the output voltage gain. The capacitors C_1, C_2, C_O values are derived from following equation,

$$C \geq \frac{2P_{MAX}}{V_C{}^2 f_s} \quad (6)$$

where P_{MAX} is output power.

RESULTS AND DISCUSSION

Simulation is performed by using MATLAB. The design value of input inductor L_1 and L_2 are 30µH, input voltage is V_{in} = 36V, coupled inductor (M_1) L_1 and L_2 values are 10µH and 50µH, magnetizing inductor L_m=150µH, switching frequency is 40 kHz. MOSFET power device is chosen because it has high switching frequency and there is no secondary break down.

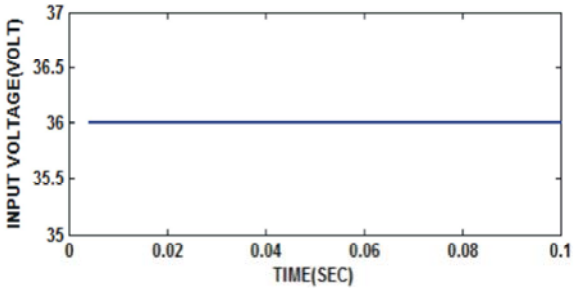

Fig. 5: Input voltage waveform of proposed converter

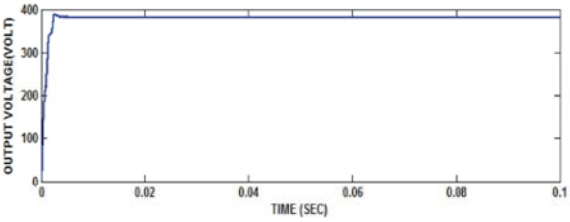

Fig. 6: Output voltage waveform of proposed converter

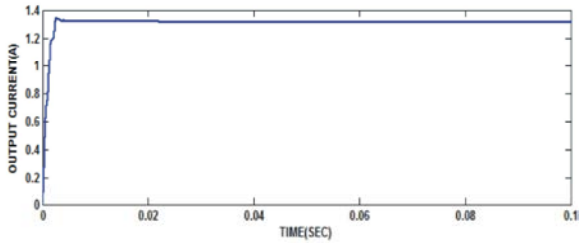

Fig. 7: Output current waveform of proposed converter

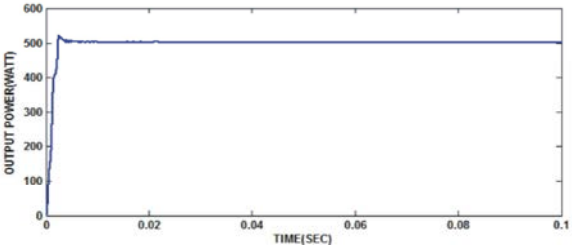

Fig. 8: Output power waveform of proposed system

In proposed boost converter the output voltage gain is 11 times greater than the input voltage compared to conventional boost converter. In conventional boost converter the voltage across the main switch is equal to output voltage which leads to increase in the voltage rating of the device. But in proposed system the voltage drop across the switch is not equal to output voltage of the converter by using active clamped circuit. The voltage stress in reference [20] of the switch is determined by duty cycle and turns ratio of the coupled inductor. But in proposed system the voltage stress of the switch is mainly determined by turn's ratio of the coupled inductor and output voltage.

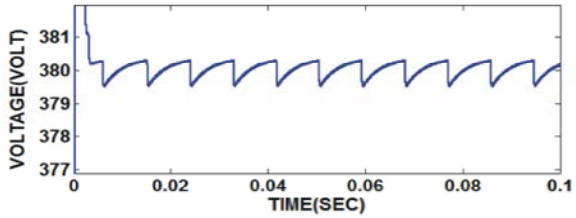

Fig. 9: Output voltage ripple waveform of proposed converter

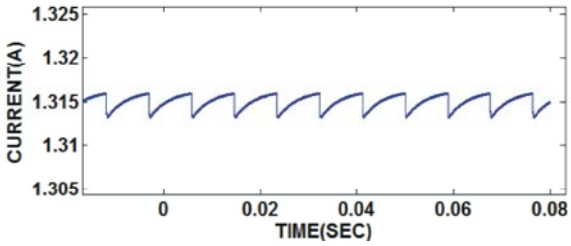

Fig. 10: Output current ripple waveform of proposed converter

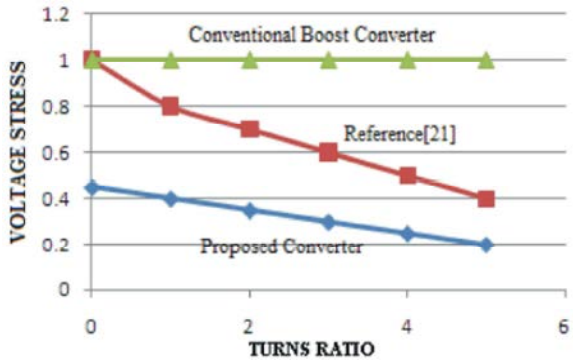

Fig. 11: Comparision of voltage stress across the switch

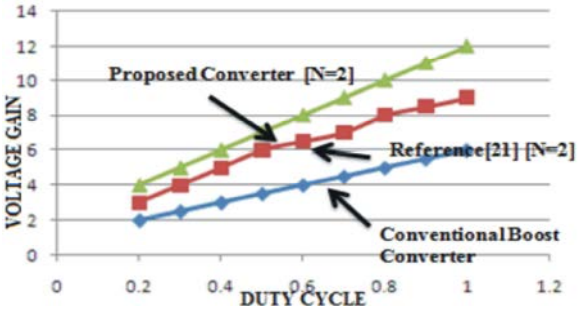

Fig. 12: Comparison of voltage gain

In conventional boost converter the voltage across the switch is equal to output voltage and the high output voltage gain is obtained when the duty ratio is near to one, which leads to increase in the conduction losses of the main switch and also the efficiency is decreased. In proposed system the output voltage is 400V and voltage stress across the switch is 150V.

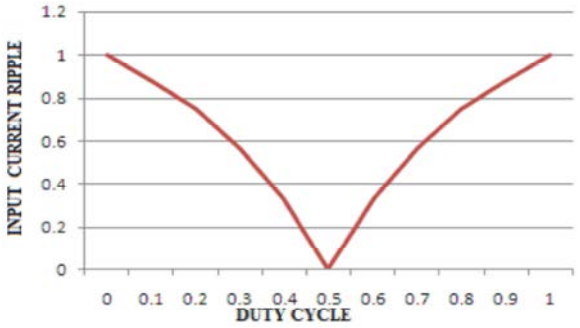

Fig. 13: Input ripple current reduction

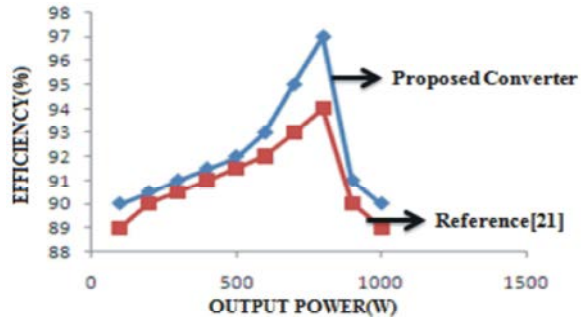

Fig. 14: Efficiency chart

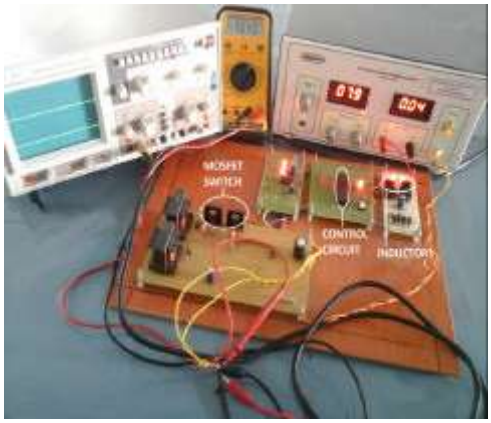

Fig. 15: Interleaved Boost Doubler with voltage doubler cell and clamped circuit

The high output voltage is obtained at 0.5 duty ratios which decrease the conduction losses and also reduce the cost of switching devices because the voltage rating of the switch is reduced. The efficiency of the converter is determined by turn's ratio of coupled inductor because it depends upon the turn's ratio only the duty cycle can be calculated. If the duty cycle is above 0.5 means the efficiency is decreased.

In existing system contains large amount of input and output current ripples. Therefore, in order to overcome that the voltage doubler cell and clamped circuit are implemented in interleaved boost converter.

Table 1: Parameters of interleaved boost converter with voltage doubler cell and clamped circuit

Components	Parameters
Maximum Output Power P_o	500W
Input Voltage V_{in}	18-36V
Output Voltage V_o	380V
Switching Frequency f_s	40kHZ
Input Inductor L_1 and L_2	30µH
Capacitor(C_1)	47µF
Capacitor(C_2)	47µF
Capacitor(C_o)	47µF
Coupled Inductor L_1 and L_2	10µH and 70µH
Microcontroller	AT89C52-24PC

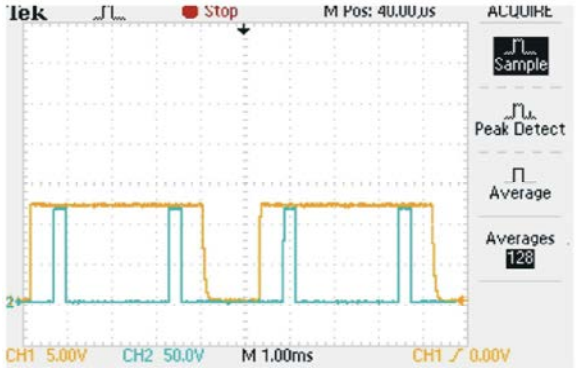

Fig. 16: Gate Pulse of MOSFET in interleaved boost converter

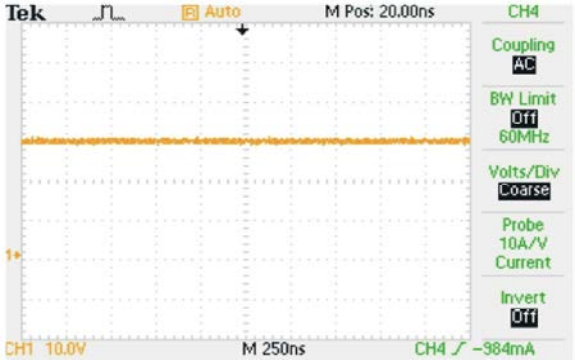

Fig. 17: Output voltage waveform

The input current ripple can be minimized at 0.5 duty cycle.

Comparison Between Existing and Proposed Topology

Parameters	Existing Topology	Proposed Topology
OUTPUT VOLTAGE RIPPLE (%)	0.78%	0.15%
OUTPUT CURRENT RIPPLE (%)	0.83%	0.13%

Hardware Implementation: The hardware is implemented by using microcontroller (AT89C52-24PC) for generating gate pulse. The input voltage given to the microcontroller

is 5V. The pulse generated from microcontroller and given to the converter. The duty ratio is 0.5 because of it the input current ripples reduced. The MOSFET switch is used for the converter topology. The voltage doublers circuit and clamped circuit are included to increase the output voltage gain and reduce the voltage stress across the switch. The output power obtained is 850watts and efficiency is found to be 97%.

Figure 16 shows the interleaved boost converter with voltage doubler cell and clamped circuit. An output voltage is improved 400V from an input voltage of 18V at duty cycle of 50%. Since the conduction period of switch is reduced which leads minimize the conduction losses[21].

CONCLUSION

A high efficiency interleaved DC-DC boost converter is proposed in this paper which combines conventional interleaved boost converter and coupled inductor with diode-capacitor. The voltage stress on the switch is reduced by connecting clamped circuit to primary side of the coupled inductor and output voltage is increased by using coupled inductor. The MOSFET switch is used for improving the system reliability. Since the maximum efficiency is obtained around 97%. The main advantage of the proposed system is continuous input current and input current ripple is reduced. Consequently, system efficiency should be improved.

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