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Vlsi Based Accident Information and Car Security System

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Abstract: VLSI based Accident information and car security system deals with the concern of saving the victim, who gets trapped in accident and also about the car security. Accident of the car is detected using pressor sensors which are fixed in car. Accident information to the nearest hospital is carried out with the help of RF communication. The location of the car is found using the GPS technique. The security of car is ensured by using password. The theft information is sent to the owner's mobile using GSM module. The ultimate design of the project is in VLSI. FPGA is used to interface these modules.

Key words: Very Large Scale Integration · Global Positioning System · Global System for Mobile Communication

INTRODUCTION

The existing methods of car security are,Remote starters for car doors, Car with door lock module facility, Using motion sensors, Using tilt sensors and etc., The drawback of these methods is that they fail to provide almost the higher security to the car. Similarly there is only manual information of accident to the hospital. There is no automatic accident information system. So our work fulfils these requirements. Our system uses the FPGA as the basic module to interface the GPS, GSM, RF modules.

Global Positioning System: The Global Positioning System (GPS) is a location system based on a constellation of about 24 satellites orbiting the earth at altitudes of approximately 11,000 miles. GPS was developed by the United States Department of Defense (DOD), for its tremendous application as a military locating utility. GPS has proven to be a useful tool in non-military mapping applications as well. GPS satellites are orbited high enough to avoid the problems associated with land based systems, yet it can provide accurate positioning 24 hours a day, anywhere in the world. Uncorrected positions determined from GPS satellite signals produce accuracies in the range of 50 to 100 meters. When using a differential correction technique, the users can get accurate positions within 5 meters or less [1].

Triangulation: In a nutshell, GPS is based on satellite ranging - calculating the distances between the receiver and the position of 3 or more satellites (4 or more if elevation is desired) and then applying some good old mathematics. Assuming the positions of the satellites are known, the location of the receiver can be calculated by determining the distance from each of the satellites to the receiver. GPS takes these 3 or more known references and measured distances and "triangulates" an additional position [2].

Location Determination by GPS Satellites: GPS satellites are orbiting the Earth at an altitude of 11,000 miles. The DOD can predict the paths of the satellites vs. time with great accuracy. Furthermore, the satellites can be periodically adjusted by huge land-based radar systems. Therefore, the orbits and the locations of the satellites, are known in advance. Today's GPS receivers store this orbit information for all the GPS satellites in an almanac. Consider the almanac as a "bus schedule" advising you about the position of each satellite at a particular time. Each GPS satellite continually broadcasts the almanac. The GPS receiver will automatically collect this information and store it for future reference [3].

Calculation of the Position from the Gps Satellites: GPS determines the distance between a GPS satellite and a GPS receiver by measuring the amount of time taken by a radio signal (the GPS signal) to travel from the satellite to the

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receiver. Radio waves travel at the speed of light, which is about 186,000 miles per second. So, if the amount of time it taken by the signal to travel from the satellite to the receiver is known, then the distance from the satellite to the receiver (distance = speed x time) can be determined. If the exact times of the transmission, reception of the signal are known, the signal's travel time can be determined.

In order to do this, the satellites and the receivers use very accurate clocks which are synchronized so generate the same code exactly at the same time. The code received from the satellite can be compared with the code generated by the receiver. By comparing the codes, the time difference between the satellite generated the code and the receiver generated the code can be determined. This interval is the travel time of the code. Multiplying this travel time, in seconds, by 186,000 miles per second gives the distance from the receiver position to the satellite in miles.

Increased Accuracy by Using Differential Gps: A technique called differential correction is necessary to get accuracies within 1 -5 meters, or even better, with advanced equipment. Differential correction requires a second GPS receiver, which is a *base station,* collecting data at a stationary position at a precisely known point (typically it is a surveyed benchmark). Because the physical location of the base station is known, the correction factor can be computed by comparing the known location with the GPS location determined by using the satellites. The differential correction process takes this correction factor and applies it to the GPS data collected by a GPS receiver in the field. Differential correction eliminates most of the errors listed in the GPS Error Budget discussed earlier.

Global System for Mobile Communications: The Global System for Mobile Communications (GSM) is the most popular standard for mobile phones in the world. GSM service is used by over 2 billion people across more than 212 countries and territories. The ubiquity of the GSM standard makes international roaming very common between mobile phone operators, enabling subscribers to use their phones in many parts of the world. GSM differs significantly from its predecessors in that both signaling and speech channels are Digital call quality, which means that it is considered a second generation (2G) mobile phone system. From the point of view of the consumers, the key advantage of GSM systems has been higher digital voice quality and low cost alternatives to making calls such as text messaging Like other cellular standards GSM allows network operators to offer roaming services which mean subscribers can use their phones all over the world.

The modulation used in GSM is Gaussian minimum shift keying (GMSK), a kind of continuous-phase frequency shift keying. In GMSK, the signal to be modulated onto the carrier is first smoothed with a Gaussian low-pass filter prior to being fed to a frequency modulator, which greatly reduces the interference to neighboring channels (adjacent channel interference).

Radio Frequency Communication: RF itself has become synonymous with wireless and high-frequency signals, describing anything from AM radio between 535 kHz and 1605 kHz to computer local area networks (LANs) at 2.4 GHz. However, RF has traditionally defined frequencies from a few kHz to roughly 1 GHz. If one considers microwave frequencies as RF, this range extends to 300 GHz. A wave or sinusoid can be completely described by either its frequency or its wavelength. They are inversely proportional to each other and related to the speed of light through a particular medium. As frequency increases, wavelength decreases. For reference, a 1 GHz wave has a wavelength of roughly 1 foot and a 100 MHz wave has a wavelength of roughly 10 feet.

Operation at Higher Frequencies: Typically, data is structured and easily represented at low frequencies; how can we represent it or physically translate it to these higher RF frequencies? For example, the human audible range is from 20 Hz to 20 kHz. According to the Nyquist theorem, we can completely represent the human audible range by sampling at 40 kHz or, more precisely, at 44.1 kHz (this is where stereo audio is sampled). Cell phones, however, operate at around 850 MHz.

Field-programmable Gate Array: A field programmable gate array (FPGA) is an integrated circuit (IC) that includes a two-dimensional array of general-purpose logic circuits, called cells or logic blocks, whose functions are programmable. The cells are linked to one another by programmable buses. A field-programmable gate array comprises any number of logic modules, an interconnect routing architecture and programmable elements that may be programmed to selectively interconnect the logic modules to one another and to define the functions of the logic modules. The basic device architecture of an FPGA consists of an array of configurable logic blocks (CLBs) embedded in a configurable interconnect structure and surrounded by configurable I/O blocks (IOBs). An IOB allows signals to be driven off-chip or optionally brought

onto the FPGA onto interconnect segments. The IOB can typically perform other functions, such as tri-stating outputs and registering incoming or out-going signals. The configurable interconnect structure allows users to implement multi-level logic designs. In addition, FPGAs typically include other specialized blocks, such as block random access memories (BRAMs) and digital signal processors (DSPs). These specialized blocks perform more specific tasks than the CLBs, but can still be configured in accordance with a variety of options to enable flexible operation of the FPGA. Field programmable gate arrays may be classified in one of two categories. One category of FPGA devices is one-time programmable and uses elements such as antifuses for making programmable connections. The other category of FPGA devices is reprogrammable and uses devices such as transistor switches as the programmable elements to make non-permanent programmable connections. An FPGA can support hundreds of thousands of gates of logic operating at system speeds of tens of megahertz. To implement a particular circuit function, the circuit is mapped into the array and the appropriate programmable elements are programmed to implement the necessary wiring connections that form the user circuit. The FPGA is programmed by loading programming data into the memory cells controlling the configurable logic blocks, I/O blocks and interconnect structure.

A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by the customer or designer after manufacturing—hence "field-programmable". The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC) (circuit diagrams were previously used to specify the configuration, as they were for ASICs, but this is increasingly rare). FPGAs can be used to implement any logical function that an ASIC could perform. The ability to update the functionality after shipping and the low non-recurring engineering costs relative to an ASIC design (not withstanding the generally higher unit cost), offer advantages for many applications.

FPGAs contain programmable logic components called "logic blocks" and a hierarchy of reconfigurable interconnects that allow the blocks to be "wired together"—somewhat like a one-chip programmable breadboard. Logic blocks can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory.

FPGA Comparisons: Historically, FPGAs have been slower, less energy efficient and generally achieved less functionality than their fixed ASIC counterparts. A combination of volume, fabrication improvements, research and development and the I/O capabilities of new supercomputers have largely closed the performance gap between ASICs and FPGAs.

Advantages include a shorter time to market, ability to re-program in the field to fix bugs and lower non-recurring engineering costs. Vendors can also take a middle road by developing their hardware on ordinary FPGAs, but manufacture their final version so it can no longer be modified after the design has been committed.

Xilinx claims that several market and technology dynamics are changing the ASIC/FPGA paradigm:

- IC costs are rising aggressively
- ASIC complexity has bolstered development time and costs
- R&D resources and headcount is decreasing
- Revenue losses for slow time-to-market are increasing
- Financial constraints in a poor economy are driving low-cost technologies.

These trends make FPGAs a better alternative than ASICs for a growing number of higher-volume applications than they have been historically used for, to which the company attributes the growing number of FPGA design starts.Some FPGAs have the capability of partial re-configuration that lets one portion of the device be re-programmed while other portions continue running.

FPGA versus CPLDs: The primary differences between CPLDs and FPGAs are architectural. A CPLD has a somewhat restrictive structure consisting of one or more programmable sum-of-products logic arrays feeding a relatively small number of clocked registers. The result of this is less flexibility, with the advantage of more predictable timing delays and a higher logic-to-interconnect ratio. The FPGA architectures, on the other hand, are dominated by interconnect. This makes them far more flexible (in terms of the range of designs that are practical for implementation within them) but also far more complex to design for.

Another notable difference between CPLDs and FPGAs is the presence in most FPGAs of higher-level embedded functions (such as adders and multipliers) and embedded memories, as well as to have logic blocks implement decoders or mathematical functions.

Security Considerations: With respect to security, FPGAs have both advantages and disadvantages as compared to ASICs or secure microprocessors. FPGAs' flexibility makes malicious modifications during fabrication a lower risk.For many FPGAs, the loaded design is exposed while it is loaded (typically on every power-on). To address this issue, some FPGAs support bitstream encryption.

Applications of FPGAs: FPGAs have gained rapid acceptance and growth over the past decade because they can be applied to a very wide range of applications. A list of typical applications includes: random logic integrating multiple SPLDs, device controllers, communication encoding and filtering, small to medium sized systems with SRAM blocks and many more. Other interesting applications of FPGAs are prototyping of designs later to be implemented in gate arrays and also emulation of entire large hardware systems.

Universalasynchronous Receiver/Transmitter: A *universal asynchronous receiver/transmitter* (usually abbreviated **UART**) is a type of "asynchronous receiver/transmitter", a piece of computer hardware that translates data between parallel and serial forms. A UART is usually an individual (or part of an) integrated circuit used for serial communications over a computer or peripheral device serial port. UARTs are now commonly included in microcontrollers. A dual UART or **DUART** combines two UARTs into a single chip. Many modern ICs now come with a UART that can also communicate synchronously; these devices are called **USARTs** (universal /asynchronous receiver/transmitter).

Transmitting and Receiving Serial Data: The Universal AsynchronouReceiver/Transmitter (UART) controller is the key component of the serial communications subsystem of a computer. The UART takes bytes of data and transmits the individual bits in a sequential fashion. At the destination, a second UART re-assembles the bits into complete bytes. Serial transmission of digital information (bits) through a single wire or other medium is much more cost effective than parallel transmission through multiple wires. A UART is used to convert the transmitted information between its sequential and parallel form at each end of the link. Each UART contains a shift register which is the fundamental method of conversion between serial and parallel forms. The UART usually does not directly generate or receive the external signals used between different items of equipment. Typically, separate interface devices are used to convert the logic level signals of the UART to and from the external signaling levels. External signals may be of many different forms. Examples of standards for voltage signaling are RS-232, RS-422 and RS-485 from the EIA. Historically, the presence or absence of current (in current loops) was used in telegraph circuits. Some signaling schemes do not use electrical wires. Examples of such are optical fiber, IrDA (infrared) and (wireless) Bluetooth in its Serial Port Profile (SPP). Some signaling schemes use modulation of a carrier signal (with or without wires). Examples are modulation of audio signals with phone line modems, RF modulation with data radios and the DC-LIN for power line communication.Communication may be "full duplex" (both send and receive at the same time) or "half duplex" (devices take turns transmitting and receiving).

Asynchronous Receiving and Transmitting: In asynchronous transmitting, teletype-style UARTs send a "start" bit, five to eight data bits, least-significant-bit first, an optional "parity" bit and then one, one and a half, or two "stop" bits. The start bit is the opposite polarity of the data-line's idle state. The stop bit is the data-line's idle state and provides a delay before the next character can start. (This is called asynchronous start-stop transmission). In mechanical teletypes, the "stop" bit was often stretched to two bit times to give the mechanism more time to finish printing a character. A stretched "stop" bit also helps resynchronization. The parity bit can either make the number of "one" bits between any start/stop pair odd, or even, or it can be omitted. Odd parity is more reliable because it assures that there will always be at least one data transition and this permits many UARTs to resynchronize. Asynchronous transmission allows data to be transmitted without the sender having to send a clock signal to the receiver. Instead, the sender and receiver must agree on timing parameters in advance and special bits are added to each word which are used to synchronize the sending and receiving units. When a word is given to the UART for Asynchronous transmissions, a bit called the "Start Bit" is added to the beginning of each word that is to be transmitted. The Start Bit is used to alert the receiver that a word of data is about to be sent and to force the clock in the receiver into synchronization with the clock in the transmitter. These two clocks must be accurate enough to not have the frequency drift by more than 10% during the transmission of the remaining bits in the word. (This requirement was set in the days of mechanical teleprinters and is easily met by modern electronic equipment).

After the Start Bit, the individual bits of the word of data are sent, with the Least Significant Bit (LSB) being sent first. Each bit in the transmission is transmitted for exactly the same amount of time as all of the other bits and the receiver "looks" at the wire at approximately halfway through the period assigned to each bit to determine if the bit is a 1 or a 0. For example, if it takes two seconds to send each bit, the receiver will examine the signal to determine if it is a 1 or a 0 after one second has passed, then it will wait two seconds and then examine the value of the next bit and so on.

The sender does not know when the receiver has "looked" at the value of the bit. The sender only knows when the clock says to begin transmitting the next bit of the word. When the entire data word has been sent, the transmitter may add a Parity Bit that the transmitter generates. The Parity Bit may be used by the receiver to perform simple error checking. Then at least one Stop Bit is sent by the transmitter. When the receiver has received all of the bits in the data word, it may check for the Parity Bits (both sender and receiver must agree on whether a Parity Bit is to be used) and then the receiver looks for a Stop Bit. If the Stop Bit does not appear when it is supposed to, the UART considers the entire word to be garbled and will report a Framing Error to the host processor when the data word is read. The usual cause of a Framing Error is that the sender and receiver clocks were not running at the same speed, or that the signal was interrupted.

Regardless of whether the data was received correctly or not, the UART automatically discards the Start, Parity and Stop bits. If the sender and receiver are configured identically, these bits are not passed to the host. If another word is ready for transmission, the Start Bit for the new word can be sent as soon as the Stop Bit for the previous word has been sent. Because asynchronous data is "self are synchronizing", if there is no data to transmit, the transmission line can be idle. A data communication pulse can only be in one of two states but there are many names for the two states. When on, circuit closed, low voltage, current flowing, or a logical zero, the pulse is said to be in the "space" condition. When off, circuit open, high voltage, current stopped, or a logical one, the pulse is said to be in the "mark" condition. A character code begins with the data communication circuit in the space condition. If the mark condition appears, a logical one is recorded otherwise a logical zero.

The start bit is always a **0** (logic low), which is also called a **space**. The start bit signals the receiving DTE that a character code is coming. The next five to eight bits, depending on the code set employed, represent the character. In the ASCII code set the eighth data bit may be a parity bit. The next one or two bits are always in the **mark** (logic high, i.e., '1') condition and called the stop bit(s). They provide a "rest" interval for the receiving DTE so that it may prepare for the next character which may be after the stop bit(s). The rest interval was required by mechanical Teletypes which used a motor driven camshaft to decode each character. At the end of each character the motor needed time to strike the character bail (print the character) and reset the camshaft.

System Design

Accident Information and Car Security System

System Functions:

- To start the engine of the car, the password should be given.
- If it is correct, the car will be started normally.
- Whenever the engine gets started, the alert message is sent to the owner's mobile.
- Second attempt will be given incase of misspelt of password in first attempt.
- If it is continued in second attempt also, the doors will be locked, buzzer will start to beep and alert message will be sent to the owner's mobile.
- If the password is given in reverse manner, the theft information will also be sent to nearest police station.
- The accident is detected by the pressure sensors.
- GPS receiver sends the data via RF modem to the nearest hospital.

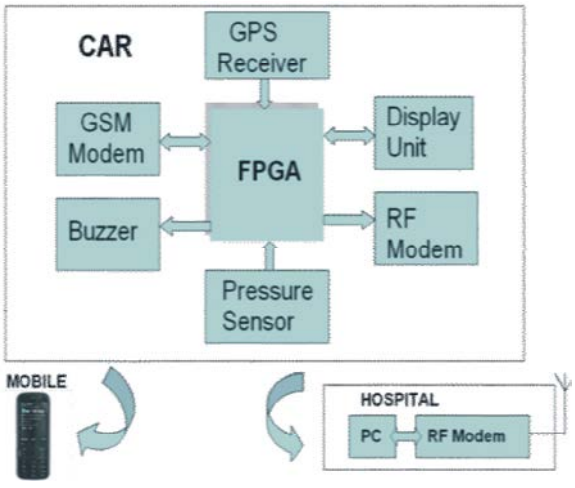

Fig. 1: Block diagram

Advantages of the System:

- Able to rescue the persons who get trapped in the accident as soon as possible.
- Car security is maintained perfectly.
- Car theft is detected and avoided before it happens.

Future Scope of the System:

- Automatic information to the traffic police, to clear the accident spot, as soon as possible.
- Avoiding the alert message to the hospital when there is none in the car.

CONCLUSION

Thus the accident location will be detected (using GPS) and will be communicated to the nearest hospital (using RF communication).Theft information is sent to mobile (using GSM modem).

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