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Effective Routing Technique Based on Decision Logic for Open Faults in Fpgas Interconnects

S.P. Vijayaragavan, B. Karthik and T.V.U. Kiran Kumar

Department of EEE, Bharath University, Chennai, India

Abstract: In this paper, different routing techniques using decision logic with identity circuit to identify the faulty element in FPGA interconnects are presented. The fault model we use here is stuck-open and resistive-open for interconnects. This technique is implemented in FPGA chips and verified using fault emulation. Failure analysis and the yield enhancement process are done by using high resolution routing. Open faults are the most common type of defect in deep sub-micron technology. An open fault is discontinuity in the connection between two circuit nodes that should be completely connected. A minor discontinuity results in resistive connection. A fault can be avoided by using another configuration which implements the same functionality but avoids the faulty elements. So a fast and high resolution routing technique is exploited to allow the use of defective chips and can also be used as fault tolerant schemes.

Key words: Decision logic · Identity circuitry · Remove/Reroute techniques

INTRODUCTION

The resistive-open and complete-open fault models for wires and the stuck-open model for programmable interconnect points (PIPs) are used. A PIP stuck-open fault causes the PIP to be permanently open regardless of the value of the SRAM cell controlling the PIP. In this paper, a two-step routing technique to precisely identify the faulty element(s) in FPGA interconnects [1-8]. The coarse-grain step localizes the fault to a small portion of the FPGA or a set of resources (e.g. a routing path), whereas the fine-grain step precisely locates the fault inside that portion of FPGA or that set of resources. An efficient search technique is exploited in the fine-grain step so as to minimize the number of configurations required. This technique can be used either by the manufacturer during failure analysis or by an FPGA user for application-specific diagnosis or fault tolerance.

Diagnosis of Open Fault in FPGA: The FPGA model used in this paper is a two dimensional array of *configurable logic blocks* (CLBs) consisting of logic blocks and switch matrices [9]. There are four logic blocks in each CLB connected to the switch matrix through input and output MUXes (IMUX and OMUX). Each logic block consists of lookup tables (LUTs) and programmable sequential elements. Switch matrices provide the connectivity to different CLBs, while logic blocks contain the combinational and sequential programmable logic.

Coarse-Grain Diagnosis: The goal of the coarse-grain diagnosis phase is to isolate the fault to a small portion of the FPGA. For some applications, such as some fault tolerance techniques in FPGAs, this phase is sufficient, where as in others, such as failure analysis, a fine-grain localization of the fault is necessary after this phase. Test-configuration generation for FPGAs is typically decomposed into test generation for logic and test generation for interconnects. In the test configurations for interconnects only *decision logic* (i.e. identity function) followed by a flip-flop is implemented in logic blocks.

An example of such an interconnect test configuration is shown in Fig. 1. The test configuration consists of several wires under test (WUTs) in the entire FPGA. Note that this test configuration can be viewed as parallel shift registers. The logic value of a WUT will be captured in the flip-flop connected to it in the next clock cycle. Hence, if a WUT is faulty, the content of the flip-flop connected to it is also faulty. By observing the output of the flip-flops after applying test vectors, the

Corresponding Author: S.P. Vijayaragavan, Department of EEE, Bharath University, Chennai, India.

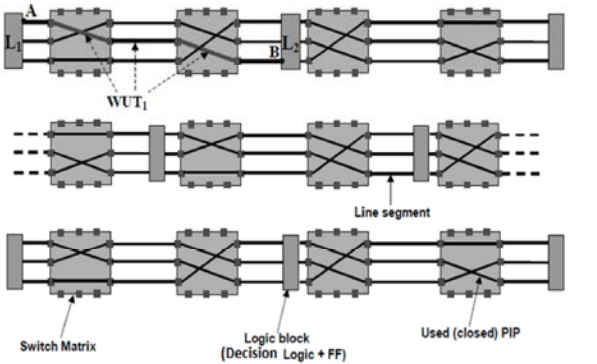

Fig. 1: A test configuration for interconnect with decision logic

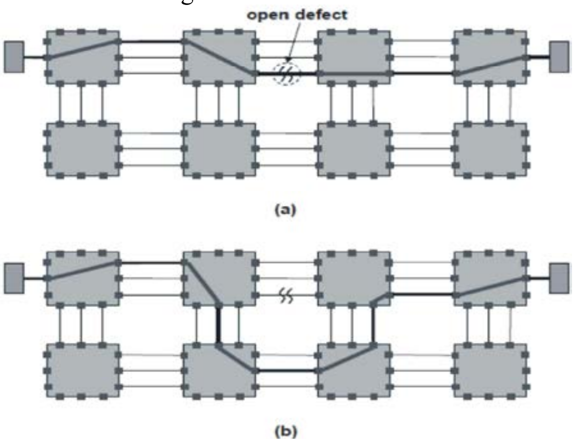

Fig. 2: (a)A WUT diagnosed to be defective (b)new WUT after removing and rerouting

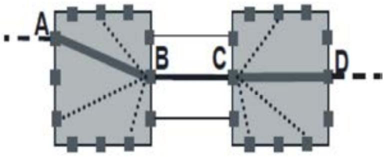

Fig. 3: A portion of a WUT

faulty WUT(s) can be identified. This output observation can be done by either scanning out the contents of flip-flops or by exploiting the *readback* feature of Xilinx FPGAs. In the first case, the value observed at the PO connected to each chain corresponds to the content of a unique flip-flop in the chain at each test clock cycle. Hence, the test clock cycle at which the fault is observed at the PO identifies the faulty WUT.

In the second case, which is a faster mode, the content of all flip-flops after applying each input vector can be read out and the faulty WUT can be identified much faster. In this technique, the fault is localized to a WUT. The diagnosis granularity depends on the length of the WUT, in terms of the number of resources used in each WUT in the test configurations. This length is proportional to the distance between two consecutive used flip-flops in the test configuration. Note that in this diagnosis phase, no extra test configuration is generated or additional test vector applied. This phase in performed just by post-processing the tester data for the set of test configurations and test vectors that have already been applied for interconnect testing (only for failing parts).

Fine-Grain Diagnosis: The input to the fine-grain diagnosis flow is a defective WUT, which is the result of the coarse-grain diagnosis scheme. The goal of this part of the diagnosis flow is to exactly identify the faulty resource [10], i.e. PIP or line segment, on the faulty WUT. Because open faults in different resources of a WUT have the same logic effect, they are equivalent faults and therefore the exact location of the fault cannot be identified using traditional logic diagnosis techniques. For example, if an open fault happens on any PIP or line segment on the *WUT1* shown in Fig. 1, the same effect is captured in the flip-flop of logic block *L2* and all these open faults are indistinguishable from the fault effect captured in that flip-flop. Thus, the reconfigurability and programmability features of FPGAs to solve this problem are exploited A new technique which is called *Remove/Reroute* is proposed

In Fig. 2.a, a WUT is shown as a part of a test configuration which is diagnosed to have an open fault. In Fig. 2.b, a portion of this WUT is removed and the WUT is rerouted without using those removed resources. In this example, the fault is located in the removed resources, therefore the new rerouted WUT will pass the test.

There are some implementation issues with this technique. Typically line segments are not directly programmable; the only programmable resources in the FPGA interconnects are PIPs. Hence, to remove a line segment from a WUT, both incoming and outgoing PIPs for that line segment must be removed from the WUT. For example in Fig. 3, to remove the line segment between *B* and *C*, both the PIPs *(A,B)* and *(C,D)* must be removed from the WUT. The dotted PIPs inside the switch matrix are those connected to *B* and *C* but not used (i.e. turned off) in this configuration.

In the implementation, both remove and reroute phases are automated using some features of an internal place and route tool at Xilinx Inc. In this tool, some PIPs of the FPGA can be marked so as to be not used by the place-and-route tool in completing the rerouting of the design. Although the new configuration for this WUT does not use either PIP *(A,B)* or *(C,D)* from the original

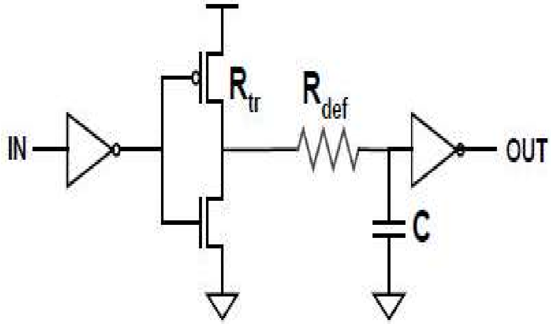

Fig. 4: A three-stage inverter chain

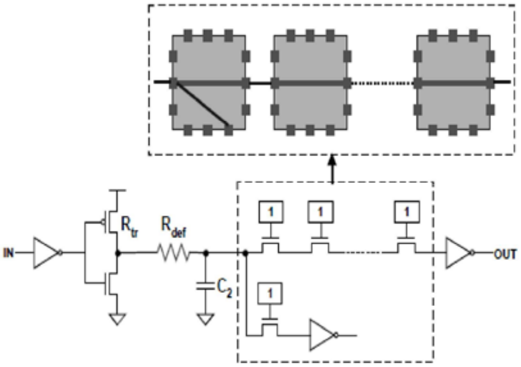

Fig. 5: A path of unbuffered PIPs

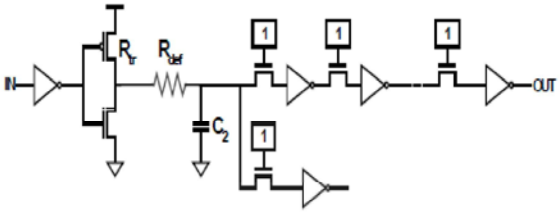

Fig. 6: A path of buffered PIPs

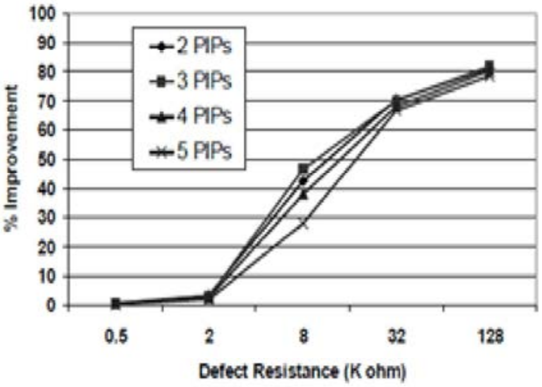

Fig. 7: Improvement ratio for path of unbuffered PIPs

configuration, line segment *(B,C)* is still used, through usage of *(P,B)* and *(C,Q)*. Therefore all the PIPs in the FPGA which are connected to *B* and *C,* must be marked to not be used in the rerouting.

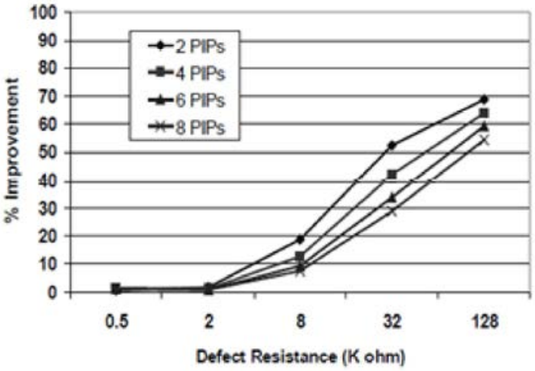

Fig. 8: Improvement ratio for path of buffered PIPs

Modeling Resistive Opens: Figure 4 shows a three-stage inverter chain with a resistive open defect in the middle stage. The delay of the middle stage can be estimated by the following equation, *Delay*=[**Rt** (VDD) + **Rdef**]*C where *Rt* is the transistor turn-on resistance as a function of the supply voltage, *VDD*. *C* is the total capacitance, including wire capacitances and load capacitance of the next stage, seen at this stage [11]. The load capacitance is proportional to the number of fanouts of this stage and input capacitance of each fanout branch. The *delay ratio* is used as the detectability metric, which is the delay of the defective circuit over the delay of the good circuit [12]. Delay ratio can be viewed as a signal to noise ratio - a larger value means higher resolution in detecting the delay fault.

Improvement ratio is defined as:
Improvement Ratio = (Delay Ratio of Circuit with Fanout)/(Delay Ratio of Original Design)

The following graphs show the improvement ratio for delay analysis:

Compared to unbuffered PIPs, each stage in the path is isolated because they are separated by buffers, yielding a slight reduction in improvement ratio as the path length increases compared to that for unbuffered PIPs. The conclusion is that the technique is still almost insensitive to path length, even for isolated stages.

CONCLUSION

In this paper, we presented a two-step diagnosis method for high resolution localization of open faults in FPGA interconnects. The first step, coarse-grain diagnosis, is the byproduct of interconnect testing of FPGA in which only transparent logic and flip-flops are implemented in logic blocks. The second step, fine-grain diagnosis, is performed by removing some resources from a defective WUT and rerouting the WUT without using those resources. Simulations for path delay analysis of both buffered and unbuffered PIPs show that improvement gained is almost insensitive to length of the path. hence all the routing resources in the FPGA can be tested for resistive opens as well as conventional boolean faults without any extra test configurations.

REFERENCES

1. Baker, K., G. Gronthoud, M. Lousberg, I. Schanstra and C. Hawkins, 1999. Defect-based delay testing of Resistive Vias-contacts, proc. of International Test Conference, pp: 467-476.
2. Bauer, T.J. and S.P. Young, 1999. FPGA interconnect structure with highspeed high fanout capability, US Patent US05907248.
3. Dastidar, J. and N. A. Touba, 2001. Improving Diagnostic Resolution of Delay Faults in FPGAs by Exploiting Reconfigurability, Proc. IEEE Symp. on Defect & Fault Tolerance, pp: 215-220.
4. Dastidar, J. and N.A. Touba, 1999. Adaptive Techniques for Improving Delay Fault Diagnosis, Proc. IEEE VLSI Test Symp, pp: 168-172.
5. [Abramovici 00] M. Abramovici and C. Stroud, 2000. BIST-Based Detection and Diagnosis of Multiple Faults in FPGAs, Proc. Int’l Test Conf.,
6. [Das 99] Das, D. and N.A. Touba, 1999. A Low Cost Approach for Detecting, Locating and Avoiding Interconnect Faults in FPGA-Based Reconfigurable Systems, Proc. Int’l. Conf. on VLSI Design.
7. [Hamilton 99] Hamilton, G., G. Gibson, S. Wijesuriya, C. Stroud, 1999. Enhanced BIST-Based Diagnosis of FPGAs via Boundary Scan Access, Proc. VLSI Test Symp., pp: 413-418.
8. Jayalakshmi, V. and N.O. Gunasekar, 2013. Implementation of discrete PWM control scheme on Dynamic Voltage Restorer for the mitigation of voltage sag /swell, 2013 International Conference on Energy Efficient Technologies for Sustainability, ICEETS, pp: 1036-1040.
9. Uma Mageswaran, S. and N.O. Guna Sekhar, 2013. Reactive power contribution of multiple STATCOM using particle swarm optimization, International Journal of Engineering and Technology, 5(1): 122-126.
10. Arumugam, S. and S. Ramareddy, 2012. Simulation comparison of class D/ Class E inverter fed induction heating, Journal of Electrical Engineering, 12(2): 71-76.
11. Nagarajan, C. and M. Madheswaran, 2012. Experimental study and steady state stability analysis of CLL-T series parallel resonant converter with fuzzy controller using state space analysis, Iranian Journal of Electrical and Electronic Engineering, 8(3): 259-267.
12. Ramkumar Prabhu, M., V. Reji and A. Sivabalan, 2012. Improved radiation and bandwidth of triangular and star patch antenna, Research Journal of Applied Sciences, Engineering and Technology, 4(12): 1740-1748.