

## Wireless Cellular Communication Using 100 Nanometers Spintronics Device Based VLSI

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**Abstract:** Rapid progress in the miniaturization of the semiconductor electronic devices leads towards chip features smaller than 100 nanometers in size. This revolution offers opportunities for developing a new generation of device incorporating standard microelectronics with spin-dependent effects arising from the interaction between carrier spin and the magnetic properties of materials. In this paper we attempt to exploit the versatility of burgeoning spin devices in connection with its application in advanced communication systems such as mobile communication as they are motivated by the anticipated low power consumption, higher degree of functionality, increased data processing speed and increased integration densities compared with conventional semiconductor devices. In fact, with “integration” being the buzzword in today’s electronics industry, gone are the days of bulky mobile cellular sets. However mobile communication systems still suffer from several limitations like multi path fading, interference, dependence on weather condition for good reception. Several error correction codes are used to get rid of such errors partially or fully. In the present work such attempt is made to realize a spintronics device based VLSI chips for error correction in wire less cellular communication. Three error correcting algorithms are employed and realized here using spintronic devices to make it power and space efficient.

**Key words:** Spintronics device • VLSI chip • Cellular communication • Error correcting codes • Power and space efficient

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### INTRODUCTION

In computer science and information theory, the issue of error detection and correction has great practical importance. Error detection is the ability to detect errors that are made due to noise or other impairments in course of the transmission from the transmitter to the receiver. Error correction has the additional feature that enables localization of the errors and correcting them. Given the goal of error correction, the idea of error detection may seem to be insufficient. However, error-correction schemes may be computationally intensive, or require excessive redundant data which may be inhibitive for a certain application. Error correction in some applications, can be achieved with only a detection system in tandem with an automatic repeat request scheme to notify the sender that a portion of the data sent was received

incorrectly and will need to be retransmitted, However, where efficiency is important, it is possible to detect and correct errors with far less redundant data.

Spintronics is the generic name for spin based electronic devices, which uses the spin degree of freedom instead of charge for information processing and as such offers opportunities for a new generation of devices combining standard microelectronics with spin-dependent effects that arise from the interaction between spin of the carrier and the magnetic properties of the material. The interest in spintronics devices is motivated by the anticipated low power consumption, higher degree of functionality, increased data processing speed and increased integration densities compared with conventional semiconductor devices [1-2]. Traditional approaches using spin are based on the alignment of a spin (either “up” or “down”) relative to a reference (an

applied magnetic field or magnetization orientation of the ferromagnetic film). Device operations then proceed with some quantity (electrical current) that depends in a predictable way on the degree of alignment. Single spin based logic devices encoded binary bit ‘1’ and ‘0’ into anti parallel spin polarization of single electron confined in quantum dots and placed in a magnetic field [1]. Nearest neighbour exchange spin resulting the single state spin configuration. A three phase clock [3] is applied to flow signal from input to output stage unidirectionally. GMR allows us to make sensors that could sense or ‘read’ extremely tiny magnetized region on a hard drive [1]. GMR read heads are composed of ‘spin valve’, namely, metallic sandwiches at least two ultra-thin ferromagnetic layers separated by a very thin nonmagnetic spacer layer [1]. In the present work such attempt is made to realize a spintronics device based VLSI chips for error correction in wireless cellular communication. Three error correcting code algorithms are employed here using spintronic devices to make it power and space efficient.

**Working Principle:** Operation of the spintronic devices is governed by the fact that (a) any two nearest neighbour electron cells have opposite spin orientation and (b) only nearest neighbour electrons interacts with each other. So it is obvious that if two nearest neighbour of electron in a row have upward orientation (taken as logic ‘1’) then the electron would have downward orientation (taken as logic ‘0’) and vice-versa. But if one of neighbour has upward and another has downward orientation the electron cell (means a quantum dot) can be either upward orientation (i.e. logic ‘1’) or downward oriented (i.e. logic ‘0’). But this does not happen because a weak external DC magnetic field is applied globally through the entire chip, which causes a small Zeeman splitting between ‘up’ and ‘down’ orientation and defines preferred orientation. Let us assume that the external DC field is applied such a way that upward orientation is favoured and so if one neighbour of a cell is upward and another is downward oriented then the cell would be upward oriented [6][7]. Thus according to above mentioned properties of spin polarized single electron cells, a cell will be downward oriented only if both neighbours have upward and downward orientation otherwise the cell will have upward orientation. In single spin logic we can realize the basic gates very easily and then synthesize them. But instead of doing this we choose the other way by simply ensuring that the correct input output relationship are realized through appropriate placement of quantum dots. In order to design single spin logic circuit as long as the exchange

interaction strength  $J$  (energy difference between the triplet and a singlet state in two exchanged quantum dots) is larger than the Zeeman splitting energy, the preferred spin configuration in two exchange couple quantum dots is the singlet state [3].

**Cyclic Redundancy Check Code:** The cyclic redundancy check considers a block of data as the coefficients to a polynomial and then divides by a fixed, predetermined polynomial. The coefficients of the result of the division is taken as the redundant data bits, the CRC. On reception, one can recompute the CRC from the payload bits and compare this with the CRC that was received [8]. A mismatch indicates that an error occurred. A cyclic redundancy check (CRC) is a type of hash function used to produce a checksum—a small, fixed number of bits—against a block of data, such as a packet of network traffic or a block of a computer file. The checksum is used to detect errors after transmission or storage [9]. A CRC is computed and appended before transmission or storage and verified afterwards by the recipient to confirm that no changes occurred on transmission [10]. CRCs are popular because they are simple to implement in binary hardware, are easy to analyze mathematically and are particularly good at detecting common errors caused by noise in transmission channels. A CRC “checksum” is the remainder of a binary division with no bit carry (XOR used instead of subtraction), of the message bit stream, by a predefined (short) bit stream of length  $n$ , which represents the coefficients of a polynomial [4].

**Implementation:** The CRC computation is usually implemented with shift registers and XOR gates, as depicted in Fig. 1. Here  $D_1, D_2, D_3$  and  $D_4$  are four shift register and  $X_1$  and  $X_2$  are two XOR gates. Initially the

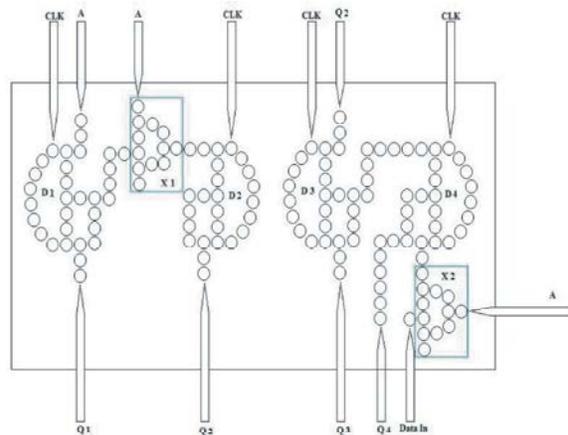


Fig 1: Single spin logic implementation of CRC Encoder

shift registers are reset [11]. Then the data bit stream is shifted through the register and its final state, the remainder, becomes the error check field.

**RS Encoder:** The Reed Solomon codes are a subclass of cyclic codes, being a special case of Bose-Chaudhuri-Hocquenghem (BCH) codes. This code can be easily implemented using linear feedback shift registers (LFSRs) [12]. This cyclic error correcting code takes a fixed length input (k symbols) and produces a fixed length check code (n-k symbols), n being the total number of symbols in the codeword.

A particular cyclic code can be represented by a polynomial divisor, called the generator polynomial. For an (n, k) code, the generator polynomial has the form:

$$G(X) = 1 + \sum_{I=1}^{n-k-1} A_I X^I + X^{n-k}$$

We thus have,

$$X^{n-k} D(X) / G(X) = Q(X) + C(X) / G(X)$$

Where D(X) is the data polynomial, C(X) is the remainder polynomial and it being concatenated properly with D(X) produces the transmitted block,

$$T(X) = X^{n-k} D(X) + C(X)$$

All the summations are, in fact, mod-2 summations, even within the symbols.

RS codes work with M-ary modulation systems. Here data are processed in chunk of m bits ( $M = 2^m$ ) called symbols. A popular value of m is 8 [4]. First and foremost we have to decide on the (n, k) values and then search for the generator polynomial, which will then yield the GF ( $2^m$ ) alphabets. If we consider  $\alpha$  being a primitive element in GF ( $2^m$ ), the generator polynomial of a primitive t-error correcting RS code of length  $2^m-1$  is:

$$G(X) = (X + \alpha)(X + \alpha^2) \dots (X + \alpha^{2t}) \\ = g_0 + g_1 X + g_2 X^2 + \dots + g_{2t-1} X^{2t-1} + X^{2t}$$

From the above expression it's apparent that G(X) has  $\alpha, \alpha^2, \dots, \alpha^{2t}$  as its roots and has coefficients from GF ( $2^m$ ). The code generated using G(X) is an (n, n-2t) cyclic code, which consists of those polynomials of degree n-1 or less with coefficients from GF ( $2^m$ ) that are multiples of G(X) [13].

As RS code is a systematic code, we have the appearance of the transmitted codeword as:  $X = (k | n-k)$ , where k = message bits, n-k = check bits

The code polynomial is generated (as in convolution code style) by long division of G(X) by M(X) the message polynomial. A shift register is used to aid in the division process.

**Implementation:** In the implementation of RS encoder, we have used an 8-ary alphabet, i.e. a 3-bit encoder. The RS coding scheme used is the well-known coding scheme where four multipliers and three adders are used [14]. A shift register is used to aid in the division process to each adder as depicted in Fig. 2. Spin implementation of the multiplier circuit is shown in Fig. 3. At the end of each block of message bits, the shift register is reset to contain the symbol "000." As soon as the complete message has entered the circuit (and also the communication channel), the n-k parity check symbols are in the register. The incoming of message symbols are temporarily stopped during this manoeuvre [5].

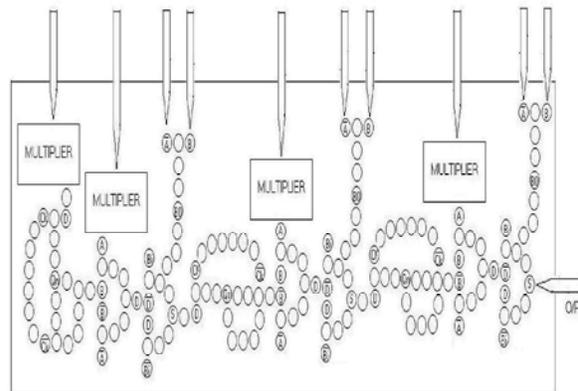


Fig 2: Single spin logic implementation of RS Encoder

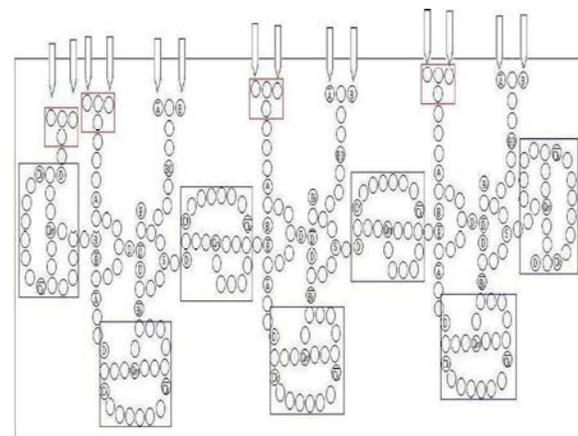


Fig 3: Single spin logic implementation of Multiplier

**Convolution Encoder:** Convolution codes differ from block codes in that the encoder contains memory and the n encoder outputs at any given time unit depend not only on the k inputs at that time but also on L previous input blocks. An (n, k, L) convolution code can be implemented with a k-input, n-output linear sequential circuit with input memory L. Typically n and k are small integers with k<n, but the memory order L must be made large to achieve low error probabilities [15].

For encoding, the message bits (m<sub>k</sub>'s) are first loaded serially into a shift register with tap gains (g<sub>s</sub>'s). The message bits in the register are combined by mod-2 addition to form the encoded bit

$$X_j = m_{j-1} \oplus \dots \oplus m_{j-1} g_1 \oplus m_j g_0 = \sum_{i=0}^L m_{j-i} g_i \pmod{2}$$

where m<sub>j</sub> is the j<sup>th</sup> message bit

The problem of constructing good convolution codes for use with the Viterbi algorithm can be calculated by a computer search as soon as the desired code rate has been selected. That code is generally selected which gives the largest free distance d<sub>free</sub>, which in turn helps in easy identification and correction of the symbols in error. However, the use of catastrophic codes should be avoided at all costs. Catastrophic errors occur when a finite number of channel errors cause an infinite number of decoding errors, even if subsequent symbols are correct.

**Implementation:** The implementation of convolution encoding is carried out using an encoder. The shift register employed has a length one more than that of the memory of the encoder. The input gets in at the LSB position. At each clock pulse, the register is shifted once to the left and the input is stored in the LSB. The output data is produced according to the logic presented above. The depicted Encoder (in Fig. 4) has a four stage shift register, (S<sub>1</sub>, S<sub>2</sub>, S<sub>3</sub> and S<sub>4</sub>) the outputs of which are connected to a set of three exclusive OR gates (X<sub>1</sub>, X<sub>2</sub> and X<sub>3</sub>).

### CONCLUSION

Here we have tried to integrate error correcting modules (can be used in typical mobile sets) of a typical mobile transceiver system into a semi-custom VLSI solution using 'single spin logic'. Incorporation of spin based devices will surely reduce the system size,

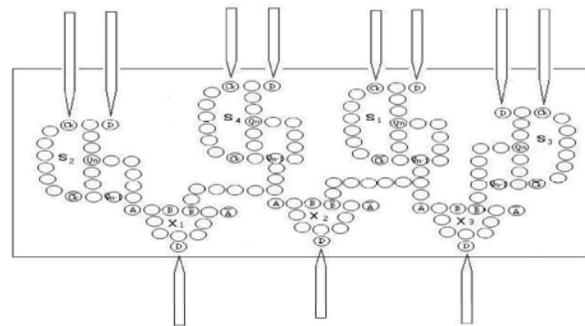


Fig 4: Single spin logic implementation of Convolution Encoder

increase the speed of operation and reduce the power consumption thereby enhancing the battery life. Since this circuit is made up of quantum dot and consequently system implementation is easier using 'single electron spin' rather than building quantum logic gates.

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