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Resonant Clock Generation

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Abstract: Proliferations of portable devices and increasing design complexity have made low power consumption one of the major factors guiding digital design. The clock distribution and generation circuitry forms a critical component of current synchronous digital system and is known to consume large amount the power budget of the current processor. *This* paper describes the importance of the sinusoidal clock in low power clock circuits and synchronous resonance clock generator for clock generation. The frequency range is 830MHz. In this paper we are going to analyze the synchronous PCG (power clock generator). Experimental results show that the 2N synchronous clock generator is less sensitive to capacitance imbalance than the 2N2P clock generator. The circuit performance is evaluated by changing the capacitance values and simulated in Tanner EDA tool.

Key words: PCG (power clock generator · Circuit performance

INTRODUCTION

One of the most important concerns in VLSI design is to achieve low power with optimum performance. For conventional CMOS circuits, the dominant source of power dissipations due to the charging and discharging of the node capacitances. The energy dissipated is given by

$$E = \frac{CV_{dd}^2}{2}$$

This is mostly converted to thermal energy. There are a number of circuit techniques that are often used by circuit designers to reduce this energy dissipation, like reducing the voltage swing, minimizing the switching activities or decreasing the node capacitances. Adiabatic switching utilizes a pulsed power supply to charge the node capacitance and then recover a portion of the energy stored in the capacitance by reversing the current source direction, allowing the charges to be transferred back into the power supply.

Thus, energy is recycled instead of dissipated as heat during evaluation. Charge recycling, on the other hand, minimizes the power by reusing a portion of charges stored in the node capacitance. With this charge-recycling technique, the power saving can be as much as 50% of the normal power dissipation per transfer. Moreover for maximum efficiency, we require sinusoidal or symmetric power clock wave. We can generate this wave by using the resonant LC-based oscillation.

Sinusoidal Clock Signal: There are two types of power dissipation in CMOS circuits: dynamic and static. Static power dissipation is related to the logical states of the circuits rather than switching activities. In CMOS logic, leakage current is the only source of static power dissipation. In conventional CMOS circuits the dynamic power dissipation is due to charging and discharging of capacitance. A higher operating frequency leads to more frequent switching activities in the circuit and results in increased power dissipation. The capacitance forms due to parasitic effects of interconnection wires and transistors. Such parasitic capacitance cannot be avoided and it has significant impact on the power dissipation of the circuits. The power dissipation on these circuits is given by the equation proposed in [1].

$$p = C_L V^2 F$$

Few assumptions are made in our derivations, they are:

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- The capacitance is constant LC
- The voltage V is constant
- The capacitance is fully charged and discharged.

We are going to violate one of the assumptions. We will no longer restrict ourselves to circuits where the supply voltage is a constant. We introduce a logic family in which the supply voltage is varied with the logical operation.

This circuit technique is commonly referred as adiabatic because in an ideal situation it does not consume power. The supply voltage in adiabatic circuits, in addition to providing the power to the circuit behaves as the clock and for this reason it is called as power clock. One of the main concerns in the adiabatic logic circuit is the power clock generation. In this supply voltage is desired to be ramping voltage, since it can be approximated to sinusoidal voltage that can be easily generated by resonance circuits. The voltage and power for sine wave is determined by [8].

$$V(t) = V_m \sin \omega t$$

$$I = \frac{V}{Z}$$

$$Z = \sqrt{\left(R^2 + X_c^2\right)}$$

$$P = VI\cos\varphi$$

$$\cos\varphi = \frac{R}{Z}$$

Here we are going to charge and discharge the capacitance slowly, that is the voltage in capacitor will follows the power-clock voltage. Fig.1 and Fig.2 represent the power dissipation in RC load driven by normal square clock and sinusoidal clock.

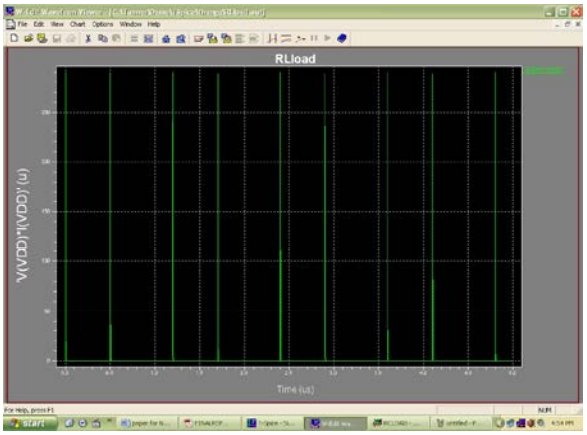

Fig 1: power dissipation in square clock circuits

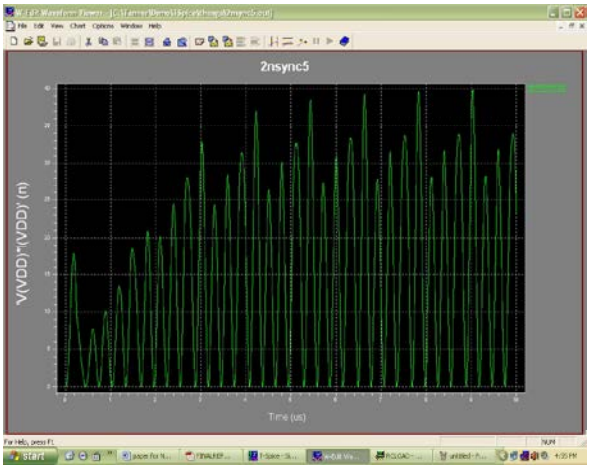

Fig 2: power dissipation in sinusoidal clock circuits

From the above simulation results we come to know that power dissipation in square clock is in microwatts that of Sinusoidal clock power dissipation is in nanowatts. Thus by using the sinusoidal clock we can reduce the considerable amount of power dissipation.

Power Clock Generator: In conventional dynamic digital circuit's power and clock lines are separate. In adiabatic circuit's power and clock lines are mixed into a single power clock line which has both the functions of powering and timing the circuit. A DC to AC converter named power clock generator is needed for the generation of the power clock signal [2]. Power clock generators usually consume the main fraction of the total energy consumed by the adiabatic system and degrade the energy savings obtained due to the energy recovery property of the adiabatic logic.

The design of power clock generator therefore is an important part of the whole adiabatic system design. Inefficient power clock generations have become an obstacle to the adiabatic module integration into a VLSI system are strongly desired. The clock generator designed should have good conversion efficiency. The conversion efficiency is defined as the ratio of the dissipated energy in the adiabatic core and the total energy delivered from the DC supply.

Two methods have been developed for power clock generation: stepwise charging [3] and resonant charging [3] where the latter is simpler, more efficient and commonly used. The LC resonant circuit, which performs like a colpitts type oscillator, is suitable for a power clock generator. Inductor used may be on chip or off chip according to our needs. The *C* component is

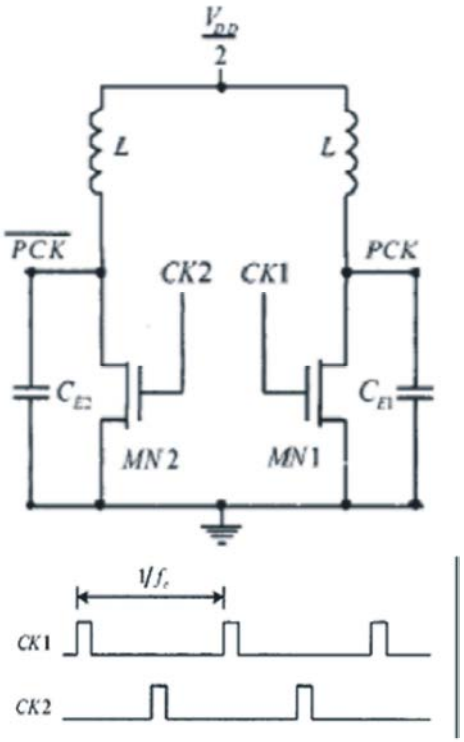

Fig 3: 2NSynchronous clock generation

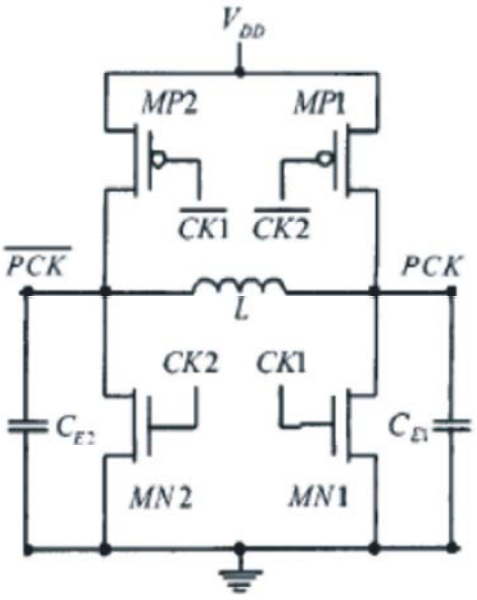

Fig 4: 2N2P synchronous clock generator

the distributed capacitance of the power clock line and it's connected logic circuits all over the chip [4, 5]. The LC product determines the oscillation frequency of the power clock generator. In order to have a stable frequency of oscillation, the equivalent on chip capacitance should be constant and data independent which is achieved in the adiabatic logic circuits due to their differential nature.

Synchronous Power Clock Generation: Circuit diagram of 2N and 2N2P synchronous clock generation is shown in the Fig.2and Fig.3 Synchronous clock generation is free from the problems associated with asynchronous PCGs however, they require external control signals. 2N requires two non-overlapping clocks as shown in Figure 3, whereas 2N2P needs two additional clocks, which are complement of the two used for 2N.

The simulated waveform of the two-phase clock signal is shown in the figure 5.

Simulation Results: From the simulation results we come to know that 2N synchronous clock generation is less sensitive to capacitance variation than the 2N2P clock generation. In 2N synchronous clock generation the capacitance variation in one phase will not affect the other phase clock but in 2N2P clock generation variation in one phase capacitance will affect both the clock phases.

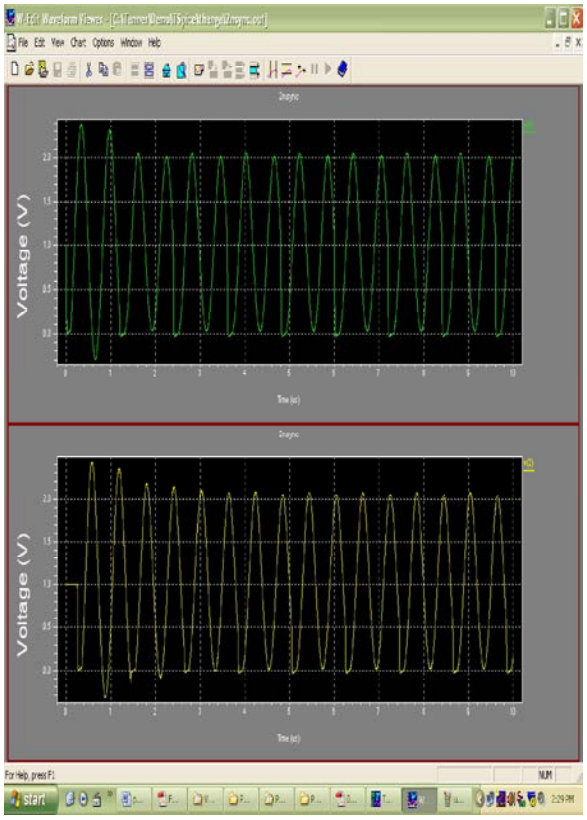

Fig 5: simulation waveform of a two-2N synchronous

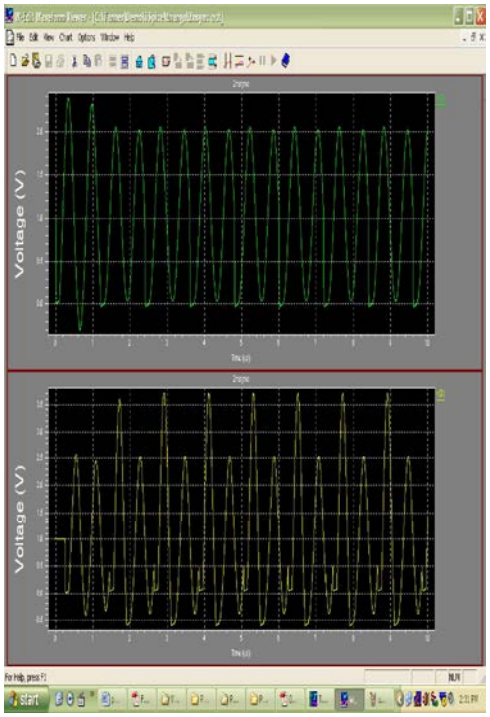

Fig 6: Two phase clock with capacitance imbalance in 2N synchronous clock circuit

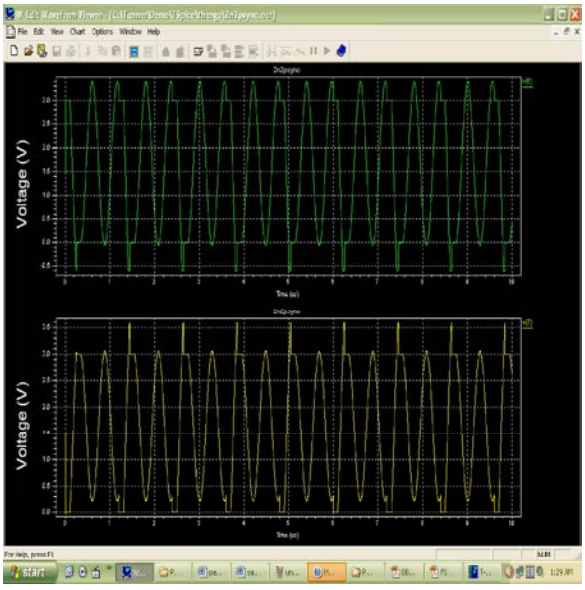

Fig 7: Two phase clock with capacitance imbalance in 2N2P synchronous clock circuit

CONCLUSION

In this paper we compared the synchronous clock generators and reported the results and we saw the importance of the sinusoidal clock in low power clock circuits. Simulations are performed at the schematic levels using a standard *0.35µm* technology. The performance is evaluated at the frequency of 830MHZ. From the simulation results, to drive circuits with large capacitance variation the 2N clock generation more efficient than the 2N2P synchronous clock generator.

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