

Optimizing 2:1 MUX for Low Power Design Using Adiabatic Logic

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Abstract: Increasing demands to improve system performance fueled the necessity of low-power design methodology. Historically, the system performance had been synonymous with circuit speed and processing power. But recently, area and time are not the only parameters to be considered while deciding the system performance. Power consumption is yet another metric. Adiabatic logic, which works on the principle of Energy Recovery, is proving to be an emerging low power approach in low power design. This paper compares conventional CMOS based design of 2:1 Mux with the designs based on the adiabatic logic styles viz. PAL and CAL. All the circuits are designed using cell based design approach and 180nm device size in Cadence. The outcome of this research work will provide guidelines for designing Mux for low-power and ultra-low power applications.

Key words: Adiabatic • Energy • Recovery • PAL • CAL

INTRODUCTION

The three contributory factors to the total power dissipation in CMOS are a) static power dissipation due to leakage current flowing through reverse biased p-n junctions and subthreshold current b) dynamic power dissipation due to charging and discharging of load capacitor during the time the output is switching and c) the short circuit current power dissipation during switching due to n-channel and p-channel transistors of the CMOS structure conducting in saturation for a short time during switching. The contribution due to dynamic power dissipation is the highest and is about 70% while that due to static power dissipation is the lowest and is about 10%. The remaining contribution to the total power dissipation is due to short circuit current dissipation. Hence to meet the objective of low power CMOS design, it becomes imperative to tackle the solutions to reduce the dynamic power dissipation primarily and then apply solutions to reduce it further due to other two reasons.

The charging and discharging of a load capacitor C_L for a conventional CMOS circuit is represented in Fig. 1. It is seen that C_L charges to V_{DD} through F while discharges to ground through F'. During charging an energy $= (1/2) C_L V_{DD}^2$ is lost in the pull up circuit while during discharging energy $= (1/2) C_L V_{DD}^2$ (which was stored in the capacitor) is lost to the ground.

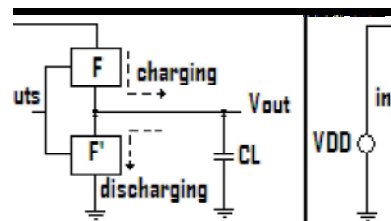


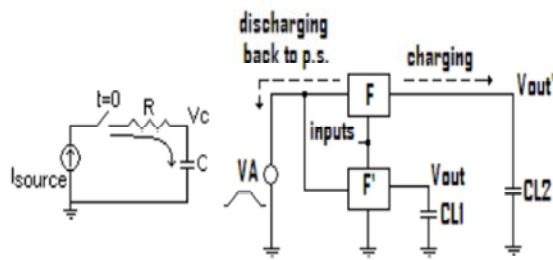
Fig. 1: Conventional CMOS.

Thus in one cycle of charge and discharge, energy $C_L V_{DD}^2$ is dissipated. If the output is switching at frequency f and the switching activity is then the dynamic power dissipation is given by,

$$P_{\text{dynamic}} = C_L V_{DD}^2 f \quad (1)$$

Thus the dynamic power dissipation depends on the load capacitor, supply voltage, frequency of switching and the switching activity. The quadratic dependence of dynamic power dissipation on supply voltage offers an attractive solution to reduce it by a factor of S^2 with supply voltage scaling down by a factor of S .

Unfortunately, supply voltage reduction has a lower bound determined by performance requirements and compatibility issues. As supply voltage is reduced, the circuit delays increase exponentially. It can be proved analytically that the power-delay product is optimized for



a: Adiabatic Switching b: Charge Flow

Fig. 2: Adiabatic Switching

power supply voltage equal to $2V_t$. This tends to limit the range of voltage supplies to a minimum of about $2V_t$. [1] Once the supply has been fixed, it remains to tactfully minimize the physical capacitance and activity at that operating voltage.

A considerable amount of energy saving can be obtained if the energy which is generally lost to the ground during discharging period in a conventional CMOS logic is returned back to the supply itself. If recycling of the energy drawn from the supply is done then the energy efficiency of the logic circuits can be increased. Adiabatic logic design offers this possibility.

Adiabatic Switching: A typical adiabatic switching circuit is as shown in Fig. 2a. Here, the load capacitance is charged by a constant current source, which corresponds to a linear voltage ramp. The main difference between the conventional CMOS circuits and the adiabatic circuits is that in adiabatic circuit the load capacitor is charged by a constant current source while in conventional CMOS circuit, it is charged by a constant voltage source. In the figure below, let R be the on-state resistance of pull-up network of the circuit.

Assuming $V_c(t)=0$ at $t=0$

$$V_c(t) = \frac{1}{C} I_{source} t$$

Where,

$$I_{source} = C \frac{V_c(t)}{t}$$

Energy dissipated in the resistor R from $t=0$ to $t=T$ can be found as

$$\begin{aligned} E_{diss} &= R \int_0^T I_{source}^2 dt \\ &= I_{source}^2 RT \\ &= \frac{RC}{T} C V_c^2(T) \end{aligned} \quad (2)$$

From this Equation it Is Observed That:

- If charging time is greater than $2RC$ then the dissipated energy is smaller than that for conventional CMOS circuit.
- Dissipated energy is inversely proportional to T , which means that dissipated energy can be made arbitrarily smaller by increasing the charging time.
- Dissipated energy is proportional to R in contrast to conventional CMOS case wherein dissipated energy depends on load capacitor and voltage swing.
- As charging resistance decreases, the energy dissipated decreases.

Fig. 2b depicts the charge flow in adiabatic circuit. Pull-up circuit drives the true output of the adiabatic gate while pull-down circuit drives the complementary output node. Both the networks in adiabatic charge up as well as charge down the output capacitor. At the end of the cycle, the energy flows back into the power supply. The important component in this circuit is the pulsed power supply with ramped voltage instead of a DC supply in conventional logic [2].

Alternatively, a stepwise supply voltage can replace the ramped power supply where the output of a power supply varies in small steps during charging and discharging of a capacitor. The energy dissipated is proportional to average voltage drop traversed by the charge and it can be proved analytically that the total energy dissipated is inversely proportional to the total number of steps from logic 0 to logic 1 as explained in the section below.

Implementation of Adiabatic Logic

Pass-Transistor Adiabatic Logic: 2:1 Mux using Pass-Transistor Adiabatic Logic (PAL) [3] is designed in ICFB tool of Cadence. PAL uses single-phase AC power-clock for adiabatic operation. When AC voltage is rising the load capacitor is adiabatically charged and when it is decreasing the load capacitor is adiabatically discharged into the power-clock supply.

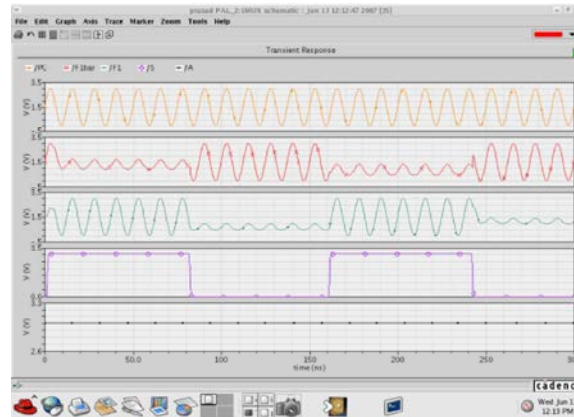
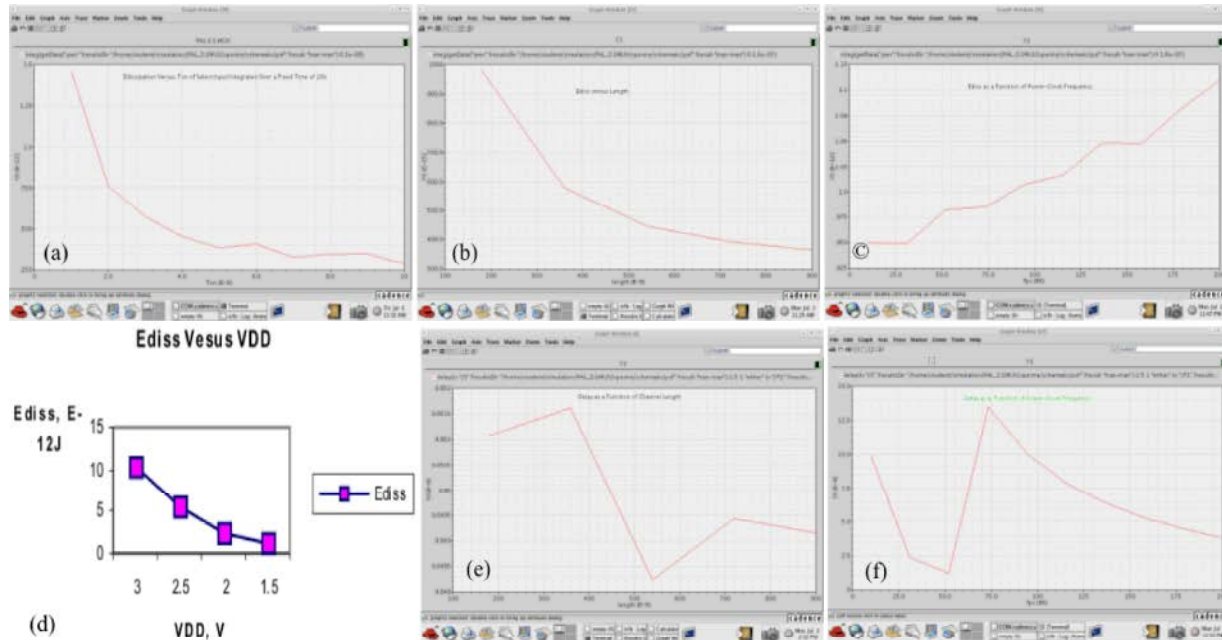


Fig. 3: Input and output waveforms PAL2:1 MUX



a. Ediss versus Ton of select
b. Ediss versus length
c. Ediss versus PC frequency
d. Ediss versus VDD
e. Delay versus length
f. Delay versus PC frequency

Fig. 4: Analysis of PAL 2:1 MUX

Each transistor has channel length of 180nm. Fig 3 shows the input-output waveforms, which is measured using Spectre.

The circuit is tested for Energy Dissipation by varying VDD, frequency of 'select' signal, channel length and frequency of single-phase power-clock supply. Delay is also measured for above parameters.

Fig 4a confirms the relationship between energy dissipated and frequency of operation as given in equation 1. The input signals A and B were held constant and the Ton of the input signal 'select' was varied. As the channel length increases, the drain current

through transistors decreases therefore the energy dissipation also decreases. This is shown in fig 4b. The inverse relationship between charging (and discharging) time of load capacitor, which in turn depends on the Power-clock (PC) frequency and energy dissipated, is verified in fig 4c. The quadratic relationship between power dissipation and VDD is depicted in fig 4d. Analysis of dependence of delay on channel length and Power-clock frequency, fig 4e and 4f, show that the PAL 2:1 MUX can be optimized at the channel length of 540nm and Power-clock frequency of 52.5MHz.

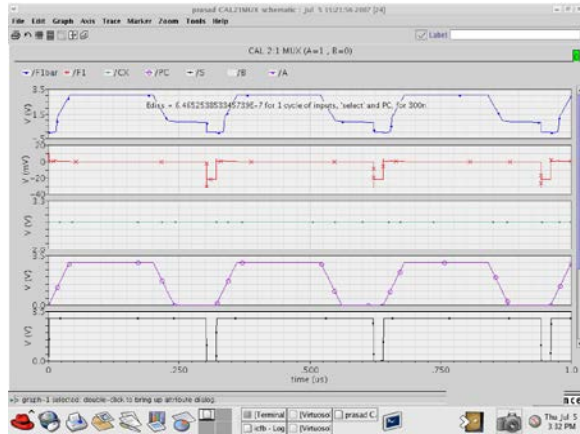


Fig. 5: Input and output waveforms CAL2:1 MUX

Clocked CMOS Adiabatic Logic: The design and simulation results of a Clocked Adiabatic Logic (CAL) [4] are described in this section. CAL is a dual-rail logic that operates on a single-phase ac power-clock. It can be also operated on a dc supply in non-adiabatic operation. Again, all transistors have 180nm channel length and schematic is designed and tested in ICFB tool of Cadence.

CAL uses ramped or pulsed Power-clock supply and hence the load capacitor is adiabatically charged when the PC is ramping up and it is adiabatically discharged when it is ramping down. As analyzed in the previous section, The circuit is tested for Energy Dissipation by varying VDD, frequency of 'select' signal, channel length and frequency of single-phase power-clock supply. Delay is also measured for above parameters.

There are other adiabatic logic families viz. Split-Charge Recovery Logic [5], PAL-2N [6]. PAL-2N dissipates more energy than PAL so it is not considered here.

Conventional Cmos Design of 2:1 Mux: Finally, a conventional CMOS design of 2:1 MUX is functionally simulated and tested in ICFB tool of Cadence using 180nm size transistors. The experimental evaluation of the circuit is done under the same input conditions as are applied in PAL and CAL evaluations.

RESULTS AND DISCUSSIONS

CAL gives the lowest energy dissipation for all device sizes. Fig 6a. The dependence of the energy dissipation on channel length is predominant in PAL and CAL. For channel lengths above 360nm, the energy dissipation of CMOS is the highest.

The quadratic relationship between the energy dissipated and VDD is observed in PAL and CMOS, CAL gives the lowest energy dissipation at VDD equal to 2V. Fig 6b.

In adiabatic designs, the system frequency is decided by the frequency of the Power-clock. In this view, CAL consumes more energy when operated above 60 MHz whereas the energy consumed by PAL slowly increases with increase in the Power-clock frequency. Fig 6c.

The relationship between frequencies of input (select signal) and the energy dissipation is linear as per equation 1. The same was observed up to 20MHz and

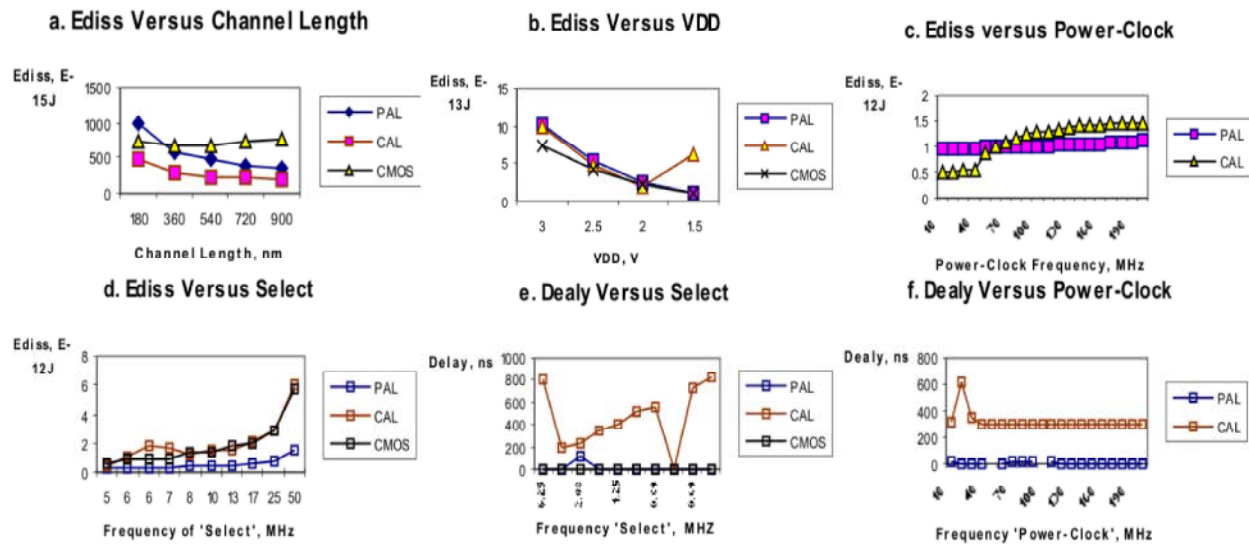


Fig. 6: Analysis of 2:1 MUX

increasing frequencies beyond this threshold show non-linear nature. PAL consumes lowest energy at all frequencies of the select signal whereas energy consumed by CAL and CMOS is almost same. Fig 6d.

Delay analysis shows that it is the lowest in conventional CMOS, which is expected as it contains very few transistors and does not use pulsed power supply. The delay of PAL circuit is the lowest when it is operated at frequencies below 1.5MHz as seen in fig 6e. The effect of the frequency of Power-clock on delay is more in CAL and the worst delay in CAL is 200 times that in PAL as observed in Fig 6.

CONCLUSION

With the energy-recovery adiabatic switching, the circuit energies are conserved within the system rather than dissipated as heat. Depending upon the system requirements and application, this approach may be used to design ultra low power under certain conditions. These conditions are obviously defined by frequency constraints, device sizes and silicon area overhead.

From the experimental evaluations it can be concluded that PAL design is suitable for designing 2:1 MUX for ultra-low power applications at high frequencies above 70MHz. To keep its energy dissipation lower than conventional CMOS, the device channel length should be at least 360nm. Higher delay is the only disadvantage of PAL as compared to CMOS.

CAL design gives optimized energy-delay product at lower frequencies. Energy dissipation of CAL is lower than that of CMOS for VDD=2V and the input frequencies above 16.7MHz. CAL dissipates the lowest energy for any device channel length compared to PAL and CMOS. Therefore, by selecting channel length of 180nm we can reduce the silicon area.

To optimize the design of 2:1 MUX for silicon area, CMOS offers the lowest transistor count of 9. PAL consumes 10 transistors in addition to silicon overhead of power-clock supply. CAL requires 14 transistors in addition to number of transistors required to generate ramped voltage supply. Table 1 epitomizes the conditions for achieving the lowest energy dissipation

Table 1: Conditions for low Edissipation.

	PAL	CAL	CMOS
Frequency of PC	>70M	<70M	NA
Channel Length	>360n	Any	<360n
VDD	<2.25	2	Any
Frequency of select	Any	<25M	<25M

Table 2: Conditions for low delay.

	PAL	CAL	CMOS
Frequency of PC	Any	>40M	NA
Frequency of select	Any	0.7<f<5M	<25M

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