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A Very Low Power IR-UWB Transmitter with Digitally Data Rate Control

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Abstract: In this paper, a very low power and low complexity all digital impulse radio ultra wideband (IR-UWB) transmitter is presented. The pulse repeating frequency (PRF) of the transmitted signal is controlled digitally, which complies with federal commission committee (FCC) regulations. In order to control the transmitted power the amplitude of transmitted signals is reduced by increasing the PRF. The transmitter can be used with both binary phase shift keying (BPSK) and pulse position modulation (PPM) schemes for modulation. We also propose a new fourth order derivative of Gaussian pulse generator circuit. The proposed signal used as impulse transmitted signal. This transmitter was designed in a 0.18 µm CMOS technology, the core chip size was only 0.025 mm^2. Simulated results showed that the transmitter consumed 7.2~18 pJ/pulse to achieved 50~400 MHz PRF. The output amplitude pulse yielded 60~350 mV peak to peak under a supply voltage of 1.8 V.

Key words: IR-UWB transmitter · Digitally PRF control · Gaussian pulse · BPSK and PPM

INTRODUCTION

UWB communication systems are classified into three categories; direct sequence spread spectrum (DS-SS), multi-band OFDM (MB-OFDM) and IR-UWB. The MB-OFDM and DS-SS UWB schemes increase the complexity, power and cost of UWB circuits. In addition, the carrier-based transceiver approaches require frequency mixers and power amplifiers which are generally difficult for full CMOS implementation.

IR-UWB technology is an appropriate solution for high speed wireless communication systems; moreover it is a promising technology from the view point of a low power, low complexity and low cost system [1]. In order to regulate the use of UWB systems, the FCC has allocated frequency spectrum from 3.1 GHz to 10.6 GHz and the average output power has been limited to-41.3 dBm/MHz [2].

IR-UWB utilizes the transmission of the short duration pulses without using carrier. According to the modulation scheme, a train of pulses is generated which is passed to the antenna. Several modulation techniques have been proposed for IR-UWB signals, such as pulse position modulation (PPM), binary phase-shift keying (BPSK) and on-off keying (OOK). The pulse generator is a key component in the IR-UWB systems because it determines the frequency characteristic of the transmitter so that satisfies FCC effective isotropic radiated power (EIRP) spectrum mask. The IR-UWB transmitter generates a pulse such as a Gaussian monocycle pulse or an nth derivative of the Gaussian pulse to satisfy the FCC regulation [3]. Ref [4] presented an all-digital and low power IR-UWB transmitter in a 65 nm CMOS process. This transmitter uses standard cells in the design procedure and the reported PRF is 50 MHz. BPSK scheme is applied for modulation of a high speed IR-UWB transmitter in [5]. The data rate of this transmitter is 750 Mb/s. Ref. [6] presented a high speed IR-Transmitter in a 180 nm CMOS process; however, it has high power consumption and area. Similar transmitters are presented in [7-9]. Some of them use a single scheme for modulation or use a structure with high complexity. Most of the reported IR-UWB transmitters were designed for a special PRF, thus; their data transmission rate is constant.

In this paper, an all-digital IR-UWB transmitter is presented that utilizes standard cells in a 180 nm CMOS

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process. The amplitude of the transmitted signal is digitally controlled so that data can be sent with different rates. Moreover, having the ability to change the output signal amplitude, it can satisfy the FCC spectrum mask easily. Therefore, no need to use any external band pass filter. The transmitter has very simple architecture. Consequently, the power consumption and chip area are decreased. This new transmitter can use both BPSK and PPM schemes for modulation. The PRF can be changed from 50 to 400 MHz. We proposed the novel positive and the negative 4th order derivatives of Gaussian pulse so that fully complied with FCC UWB power mask.

The Organization of this Paper Is as Follows: Section 2 presents the Gaussian pulse generator circuits for the new IR-UWB system. Section 3 describes the proposed transmitter architecture. The simulation results are given in section 4. Finally, conclusion is presented in section 5.

Gaussian Pulse Generator Circuit: Typically, derivatives of Gaussian pulses are used for indoor IR-UWB communication systems because of mathematical convenience and ease of implementation. The circuits that generate the first and the second order of Gaussian pulse derivatives have simpler scheme compared to higher order derivatives. However, additional filtering circuits are needed to satisfy FCC regulations of EIRP mask. In [10] the Gaussian pulse was designed based on Digital to Analog Converter (DAC) structure, in which the reference voltages are obtained by piecewise constant approximation of the pulse shapes. It has been reported that the 4th and 5th derivative of the Gaussian pulse has the most effective pulse shape which satisfies the FCC regulation without any filtering [11]. A 5th derivative of Gaussian pulse generator is proposed in [12-13].

The equation of the 4th order derivative of Gaussian pulse for IR-UWB system can be written as:

$$G(t) = \frac{A}{\sqrt{2\pi}\sigma}\exp\frac{-t^2}{2\sigma^2},\ G^4(t) = \frac{d^4G(t)}{dt^4} \quad (1)$$

Where the parameter A is for signal power adjustment and σ is a shape factor which are chosen to meet the limitation set by the FCC.

Positive 4th Derivative of Gaussian Pulse Circuit: Fig. 1(a) shows the positive 4th derivative of Gaussian pulse satisfying the FCC limitation. It consists of two blocks: a digital triangular pulse generator and an output stage driving a 50 Ω load.

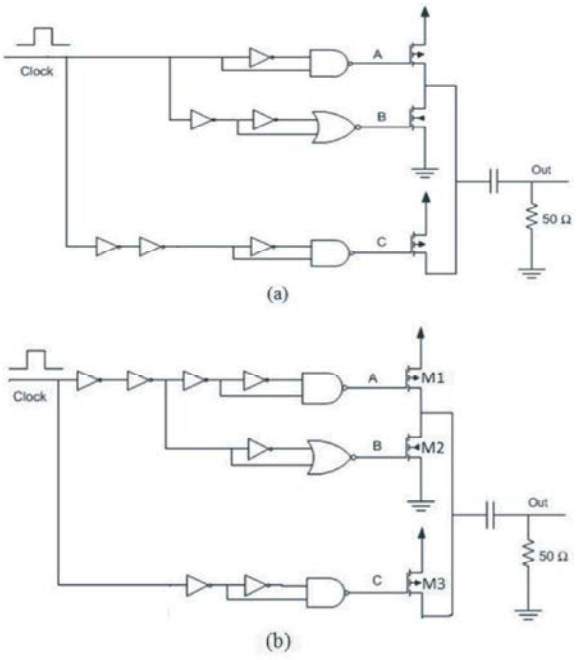

Fig. 1: (a) The proposed positive 4th derivative of Gaussian pulse circuit and (b) The proposed negative 4th derivative of Gaussian pulse circuit.

The input signal is a square pulse train and then digital triangular pulse generator provides the input signal to the pulse shaping circuit. The outputs of NAND and NOR gates are low and high at any given time, respectively. The voltage variations on nodes A and C take the shape of a triangular pulse from VDD to the ground and voltage variations on node B is built up to a triangular pulse from the ground to VDD. The NOR gate generates a positive-peak triangular pulse and the negative-peak triangular pulse is constructed by the NAND gates. Each triangular pulse is designed to have the same peak-to-peak amplitude. To organize four phase signals correctly, the delay times of the four pulses are determined by changing the size and the number of the inverters. In the output stage, the four triangular pulses generated in the previous block are combined successively. The output current magnitudeis controlled by output transistor (M1–M3) sizes. Power consumption is minimized by turning on only one MOS transistor in the output stage during each phase [12]. The signal produced by this circuit is called a positive signal.

Negative 4th Derivative of Gaussian Pulse Circuit: Fig. 1(b) presents the negative 4th derivative of Gaussian pulse. The signal at nodes C, B and A are applied to the shaping circuit, respectively. As a result, the output of

this negative signal has 180 degrees phase difference than the positive circuit.

Transmitter Architecture: Two new transmitter structures that employ BPSK and PPM schemes for modulation are presented in this section. Then, the total architecture for the transmitter is presented.

BPSK Transmitter Architecture: The transmitted signal of BPSK-UWB system can be written as:

$$S_{BPSK}(t) = \sum_{j=-\infty}^{\infty} b_j G(t - jT_f) \quad (2)$$

Where $b_j \in \{-1,1\}$ is mapping values of data bits, T_f is frame duration and G(t) is impulse signal.

A block diagram of the proposed BPSK IR-UWB transmitter is shown in Fig. 2. The BPSK transmitter consists of the positive (Fig. 1(a)) and the negative (Fig. 1(b)) circuits, two switches and a D-FF. In the proposed structure, if one switch is on, the other one is off and vice versa. The clock signal passes through the switch and then applied to the pulse generator. Switching timing is controlled by the input data. If the input data is '1', SW1 is on and SW2 is off. Now, the positive Gaussian pulse appears at the 50 Ω antenna output. Conversely, if the input data is '0', SW1 is off and SW2 is on. The negative Gaussian pulse is generated at the 50 Ω antenna output.

Fig. 2(b) shows the circuit of these switches. The switches consist of PMOS and NMOS transistors as transmission gate. The width ratio of the PMOS to NMOS is designed to 2.5:1.

PPM Transmitter Architecture: The transmitted signal of PPM-UWB system can be written as:

$$S_{BPSK}(t) = \sum_{j=-\infty}^{\infty} G(t - jT_f - \Delta b_j) \quad (3)$$

Where $b_j \in \{0,1\}$ is data bits, T_f is frame duration, Δ is modulation index and G(t) is impulse signal.

A block diagram of the proposed PPM-UWB transmitter is shown in Fig. 3(a). The positive 4th derivative of Gaussian pulse is employed in this structure. When SW2 is on and SW1 is off, the clock goes through a delay circuit and then applied to the pulse generator circuit; consequently the output pulse is generated at the output node with delay as Δ.

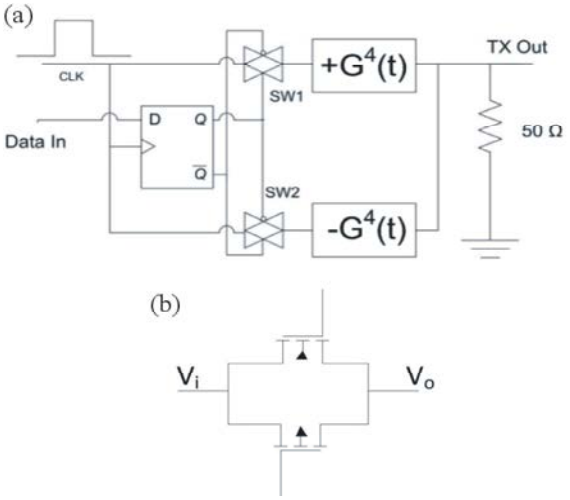

Fig. 2: (a) The proposed BPSK transmitter architecture (b) Transmission gate as switch.

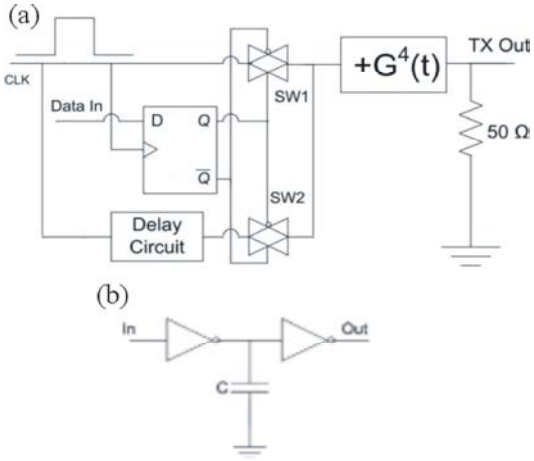

Fig. 3: (a) The proposed PPM transmitter architecture (b) Delay circuit.

Fig. 3(b) shows the delay generator circuit. The circuit uses two inverter gates and a capacitor.

Total Transmitter Architecture: The proposed transmitter structure consists of two parts: the amplitude control circuit and the circuit selection modulation type. Since the maximum power of transmitted signal is 41.3 dBm/MHz when the data transmission rate increases, the amplitude of the output transmitter must be reduced. Fig. 4 shows the transmitter architecture. By changing the equivalent resistance (R) that connected to the output of transmitter, the amplitude of transmitted signal can be controlled. When the 50 Ω antenna resistance is paralleled with any one of R1, R2 or R3, then the equivalent resistance is decreased and consequently the signal amplitude is reduced.

Table 1: The situation of M1, M2, M3 and value of R, at different PRF.

M1	*M2*	*M3*	*R1-R2-R3 (Ω)*	*R (Ω)*	*PRF (MHz)*
OFF	OFF	OFF	---	50	50
ON	OFF	OFF	R1=116	35	100
OFF	ON	OFF	R2=28.125	18	200
OFF	OFF	ON	R3=8.14	7	400

The M1, M2 and M3 transistors were used to select any of resistors R1, R2 or R3, respectively. Table 1 shows the transistor situation, R and the transmitted PRF.

Modulation selecting circuit consists of two switches: SW3 and SW4. When the signal mode is '0', the input data is modulated in BPSK form and when the signal mode is '1' the data is modulated in PPM scheme. In BPSK modulation state SW4 is on and SW3 is off and convertibly in PPM scheme the SW3 is on and SW4 is off.

RESULT

The proposed transmitter was simulated using 0.18µm CMOS standard cells with a supply voltage of 1.8 V. Fig. 5(a) shows the output waveform of the positive and the negative 4th derivative of Gaussian pulse. The two output pulses have precisely 180 degrees phase difference. The spectrum of output generator signal is shown in Fig. 5(b) which complies with FCC regulations. The center frequency of spectrum is about 5.4 GHz.

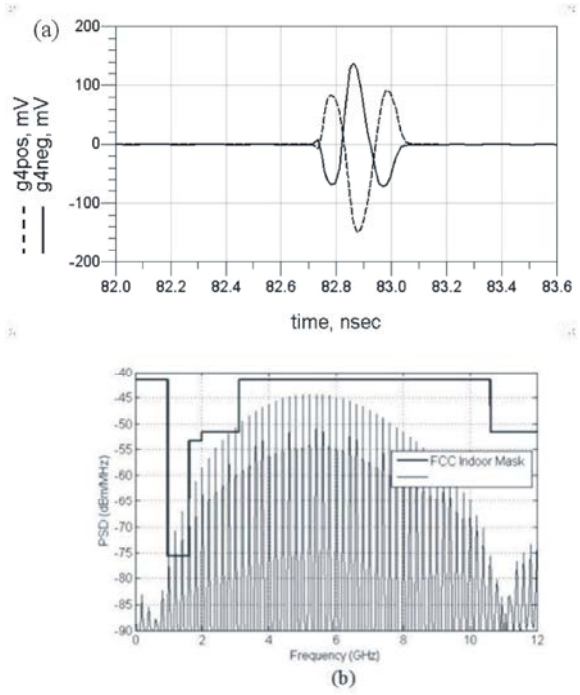

Fig. 5: (a) Waveform of transmitted signal (b) Spectrum of transmitted signal.

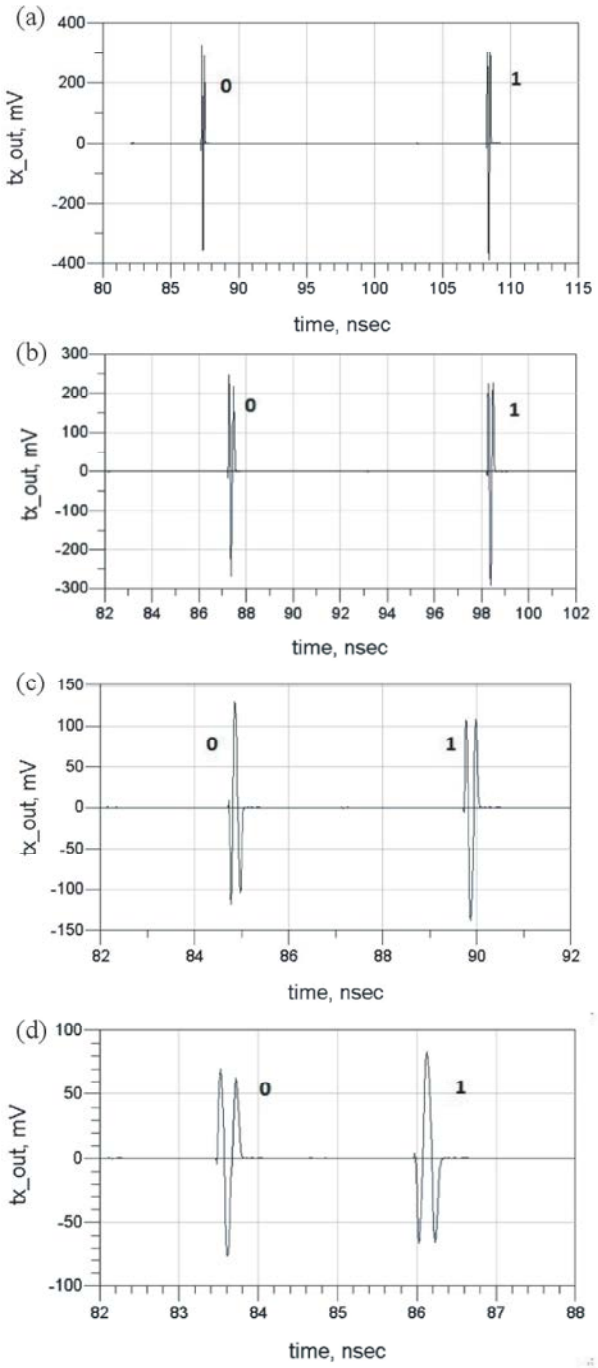

Fig. 6: Output of the modulated signal at: (a) 50, (b) 100, (c) 200 and (d) 400 MHz PRF.

Table 2: Simulation Results Comparison with prior works.

	Ref.[4]	Ref.[5]	Ref.[6]	Ref.[7]	Ref.[8]	Ref.[9]	This work
Supply Voltage (V)	0.9	1.8 to 2.2	-	1	1	1	1.8
PRF (MHz)	0 to 50	750	560	0 to 15.6	16.7	0 to 15.6	50 to 400
Energy Consumption (pJ/pulse)	8 to 16	12	75	17	47	40	7.2 to 18
Size (mm^2)	0.032	0.045	0.11	0.07	0.08	0.07	0.025
Center frequency (GHz)	3.1 to 5	8	3 to 5	2.1 to 5.7	3.1 to 5	3.1-10.6	3.1-10.6
Modulation	PPM+DB+ BPSK	BPSK	BPSK+ PPM	BPSK+ PPM	PPM+DB+ BPSK	BPSK+ PPM	BPSK+ PPM
Output Amplitude (mV)	~91 to 126	~70	~200	~200	~700	~600	~60 to 350
Technology	65 nm CMOS	180 nm CMOS	180 nm CMOS	90 nm CMOS	90 nm CMOS	90 nm CMOS	180 nm CMOS

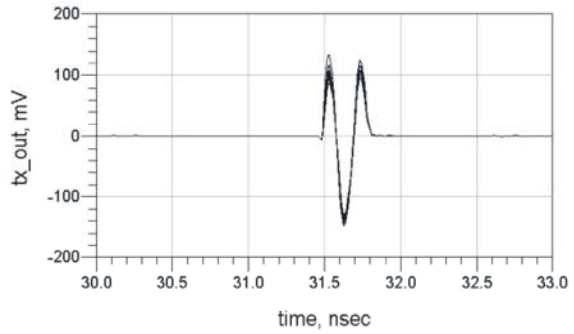

Fig. 7: Monte Carlo simulation results for 5 present variation in transistors size.

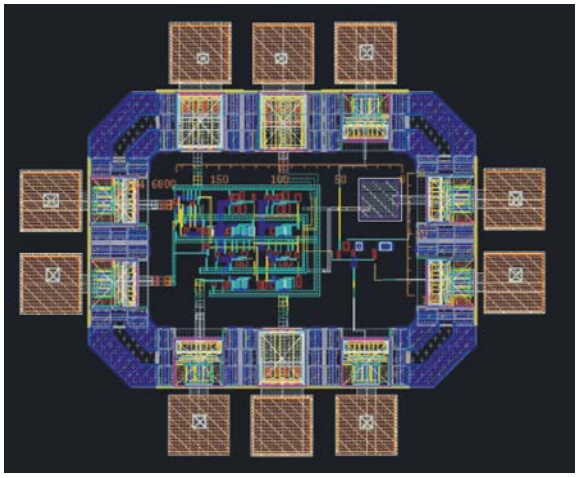

Fig. 9: Layout of the proposed transmitter

The output modulated signal at various PRF can be seen in Fig. 6. The amplitude of transmitted signals is reduced by increasing the PRF. Signals are modulated in BPSK scheme in Fig. 6 (a) and Fig.6 (b). Fig. 6(c) and Fig.6 (d) shows the waveforms of PPM modulation for Δ=1 nSec.

The Monte Carlo simulation results are shown in Fig. 7. When we change the size of transistor, the variation of the output pulse is acceptable.

Figure 9 shows the layout of the proposed transmitter. The layout is performed with a 0.18µm CMOS technology using standard cells. It shows that this design occupies the smallest circuit size of 0.025 mm^2.

Table 2 summarizes the key transmitter specifications for the reported state of the art in the similar transmitter circuits. The lowest reported power dissipation is only 7.2~18 pJ/pulse at 50~400 MHz PRF while covering the 3.1-10.6 GHz UWB spectrum.

CONCLUSION

A very low power and low complexity all-digital IR-UWB transmitter is proposed in this paper. This new transmitter was designed and simulated in 0.18µm CMOS using standard cells. The pulse-repeating frequency (PRF) of the transmitted signal was controlled digitally, which complied with FCC regulations. The transmitter generated BPSK and PPM modulated pulses at 5.4 GHz center frequency. We also proposed a new positive and the negative 4^{th} order derivative of Gaussian pulse were used in transmitter architecture. The post-layout simulation results showed that the core chip size is only 0.025 mm^2 and the output amplitude pulse is 60~350 mV peak to peak under a supply voltage of 1.8 V. The transmitter operated in the 3.1~10.6 GHz UWB band and transmitter consumed 7.2~18 pJ/pulse to achieve data rate of 50~400 Mb/s.

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