Guest Editorial of WASJ Special Issue
(Recent Trends in VLSI Design)

VLSI has a governing role to play in the field of technology and applications. The aggressive growth of transistors for emerging technological needs have created a void. To fill these voids of VLSI, newer and interdisciplinary methodologies are required. In past few decades, we have witnessed technological advancement towards the same path; whether it is System-on-Chip (SoC), Network-on-Chip (NoC), Field Programmable Gate Array (FPGA) or application of well-established algorithms of computer science (e.g. Genetic evolutionary algorithm), they have taken technology to a new level. Newer EDA tools, technologies and supporting hardware are required for further progression of this trend. On the other hand, observing the trend of scaling (Moore's law) that can be understood that one day scaling will reach at its fundamental limitation.

The aim of this special issue is to present and identify most significant, recent and novel developments in VLSI trends, Digital/Analog circuits, EDA tools, and Optimization algorithms. We received several paper submissions from IEEE World Congress on ICT, Dec 11-14, Mumbai, India, which were all peer-reviewed by 15 professional reviewers. Finally, twelve papers were accepted for publication in this special issue. Among these, six belong to the digital VLSI design, one belongs to analog VLSI design, three belongs to reconfigurable logic and two belong to the multi-core-related research area.

The topics of the submitted papers in the VLSI design include modeling of Flip-Flop, Phased-Locked Loop, Filters, optimization of transistor width and Neuro-Fuzzy on chip learning. The reconfigurable research area includes overview system level design, RTL code generation, architecture synthesis, and secure applications. The first paper proposes a four squared-layer topology for Networks-on-Chips. The proposed topology has a significant effect on the most important parameters of a network such as latency and power consumption. Authors have compared with existing topology and results of comparisons show that proposed topology perform better than mesh and Spidergon topologies.

In second paper, authors have presented a very interesting survey on low-power techniques in Network-on-Chip. Author have presented a discussion that local orthodox techniques for power saving are not sufficient to address the power issue to reduce the power dissipation in the interconnection network. The paper also presents various mathematical models to reduce the power.

Third paper presents stabilization and tracking systems to maintain the orientation of optical sensor payloads. To overcome many problems in tracking system, Authors have proposed a choquet fuzzy integral based control algorithm.

In the fourth paper, authors have presented a new static master-slave flip flop configuration based on a regenerative feedback loop strategy using a single clocked pass transistor. Authors have realized the flip flop is realized using only eleven transistors.

The fifth paper presents a novel design for charge pump. The proposed charge pump circuit has simple symmetric structure and provides more stable operation while reducing spurious jump phenomenon. Authors have tested functionality of charge pump at operating frequency of 1000 MHz.

The sixth paper presents a current differencing buffered amplifier as an active element for analog signal processing. The proposed filter uses a single current differencing buffered amplifier (CDBA) and a total of five/six passive components.

In seventh paper authors have presented design of CDMA Transceiver. Authors have used pure digital BPSK modulation technique to implement the CDMA Transceiver.

In eighth paper authors have presented design of DSP based FPGA board. To obtain optimum performance authors have interfaced 16-bit MSPS ADC with Vertex-4SX FPGA device.

In ninth paper authors have presented comparative analysis of SET D Flip-Flops based on their performance ad power dissipation.

In tenth paper authors have presented a Neuro-Fuzzy integrated system using on-line learning ability of neural network. Authors have realized activation and membership functions for NFIS have been using differential amplifier and operational transconductance amplifier (OTA) respectively.

In eleventh paper, authors have presented a secure application of VLSI Design. Authors have presented layout implementation of secure hash algorithm-1(SHA-1) which is an area efficient chip with respect to simple parallel architecture of secure hash algorithm-1. Authors have achieved 426 MHz operating frequency for SHA-1 implemented at 180 nm TSMC library.

The twelfth paper presents very interesting approach for optimization of transistor width using Logical Effort theory. Authors have utilized feature of SPICE net list and TCL for automation.

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We would like to thank the authors for their wonderful work; without their contributions, this special issue would not be possible. Also, we would like to extend our sincere thanks to the members of the Editorial review Board for their stringent and high-quality reviews. Last but not the least; we are grateful to the Editor-in-Chief and the production staff of *World Applied Science Journal.* Their help was invaluable for the preparation of this special issue.

Guest Editors

Mohammad Ayoub khan is working with Center for Development of Advanced Computing (Ministry of Communication and IT), Govt. of India with interests in Radio Frequency Identification, microcircuit design, and signal processing, NFC, front end VLSI(Electronic Design Automation, Circuit optimization, Timing Analysis), Placement and Routing in Network-on-Chip etc. He has more than seven years' experience in his research area. He has published more than 50 papers in the reputed journals and international IEEE conferences. He is contributing to the research community by various volunteer activities. He has served as Conference chair in various reputed IEEE/Springer international conferences. He is member of professional bodies of IEEE, ACM, ISTE and EURASIP society. He is also member of technical committee at various journals of IEEE, Springer and Elsevier. Recently, he has also co-authored/edited three books. He may be reached at ayoub@ieee.org.

Abdul Quaiyum Ansari is working with the Department of Electrical Engineering at Jamia Millia Islamia (A Central University by an Act of Parliament), New Delhi. He has also served as Professor and Head, Department of Computer Science, and as Dean, Faculty of Management Studies and Information Technology at Jamia Hamdard (Hamdard University), New Delhi. Professor Ansari did his B. Tech. (Electrical, Low Current) from AMU, Aligarh, and received the M. Tech. (IEC) and Ph. D. degrees from IIT Delhi and JMI, New Delhi respectively. His researches are in the areas of Computer Networks, Networks-on-Chip, Image Processing and Fuzzy Logic. He has published about eighty research papers in International and National Journals and proceedings of conferences. Prof. Ansari is a Fellow of IETE, IE (I), and National Telematics Forum (NTF). He is a Senior Member of IEEE (USA) and Computer Society of India and Life Member of ISTE, ISCA, and National Association of Computer Educators and Trainers (NACET). He is also presently the Chairman of the Delhi Chapter of the IEEE-Computational Intelligence Society. He can be reached at aqansari@ieee.org.

Ajith Abraham received Ph.D. degree from Monash University, Melbourne Australia and a Master of Science Degree from Nanyang technological University, Singapore. His research and development experience includes over 17 years in the Industry and Academia spanning different continents in Australia, America, Asia and Europe. He works in a multi-disciplinary environment involving computational intelligence, network security, sensor networks, e-commerce, Web intelligence, Web services, computational grids, data mining and applied to various real world problems. He has authored/co-authored over 350 refereed journal/conference papers and book chapters and some of the papers have also won best paper awards at international conferences and also received several citations. Some of the articles are available in the ScienceDirect Top 25 hottest articles -- http://top25.sciencedirect.com/index.php?cat_id=6&subject_area_id=7. He is actively involved in the Hybrid Intelligent Systems (HIS); Intelligent Systems Design and Applications (ISDA) and Information Assurance and Security (IAS) series of International conferences. He is the General Co-chair of the Tenth International Conference on Computer Modeling and Simulation, (UKSIM'08), Cambridge, UK; Second Asia International Conference on Modeling & Simulation (AMS 2008), Malaysia; Eight International Conference on Intelligent Systems Design and Applications (ISDA'08), Taiwan, Fourth International Symposium on Information Assurance and Security (IAS'07), Italy; Eighth International Conference on Hybrid Intelligent Systems (HIS'08), Spain; Fifth IEEE International Conference on Soft Computing as Transdisciplinary Science and Technology (CSTST '08), Cergy Pontoise, France and the Program Chair/Co-chair of Third International Conference on Digital Information Management (ICDIM'08), UK and Second European Conference on Data Mining (ECDM 2008), Netherlands. He is a senior member of IEEE, IEEE Computer Society, IEE (UK), ACM etc. More information please visit at: http://www.softcomputing.net